Timing Window Wiper : A New Scheme for Reducing Refresh Power of DRAM

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Ho Hyun Shin, Hyeokjun Seo, Byunghoon Lee, Jeongbin Kim and *Eui-Young Chung*

Yonsei University, Republic of Korea

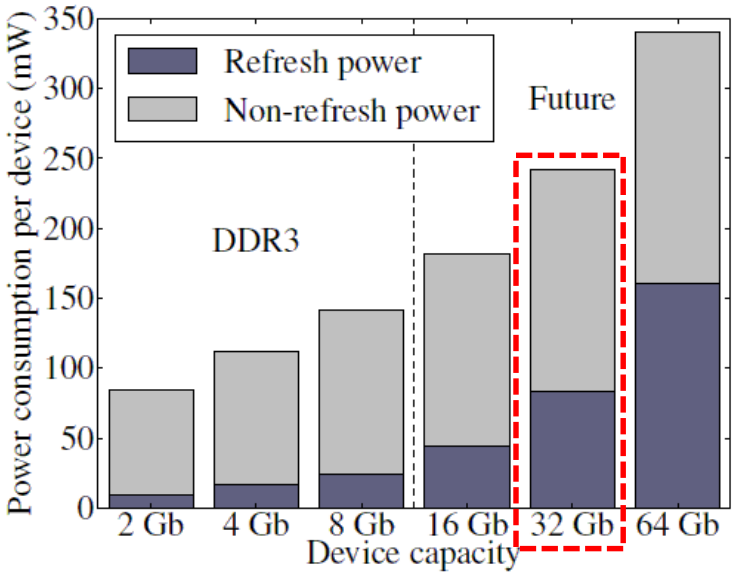
Power Breakdown for DRAMs

Table 1. Power consumption breakdown for an IBM p670.

IBM p670 server	Processors	Memory	I/O and other	Processor and memory fans	I/O component fans	Total watts
Small configuration (watts)	384	318	90	676	144	1,614
Large configuration (watts)	840	1,223	90	676	144	2,972

Memory power accounts for 40% of the total system power.

* C. Lefurgy, K. Rajamani, F. Rawson, W. Felter, M. Kistler, and T. Keller, “Energy management for commercial servers, “Computer, vol. 36, pp. 39-48, Dec. 2003.



Refresh power accounts for up to 35% of total DRAM power in high capacity DRAMs

* J. Liu, B. Jaiyen, R. Veras, and O. Mutlu, “RAIDR: Retention-aware intelligent DRAM refresh," in 2012 39th Annual International Symposium on Computer Architecture (ISCA), pp. 112, June 2012.

Previous Works

■ Row Selective

SRA, Smart Refresh, ESKIMO

**** Key idea***

The DRAM controller has a tag table for all row addresses and prevents pre-activated or unnecessary row from refresh.

(+) *Pros*

1) Simple to implement

(-) *Cons*

1) Large register size
2) Limited effect on refresh power reduction

■ Retention Time Aware

RAIDR, VRA, Flikker, RAPID

**** Key idea***

Adjust refresh period of each row based upon its retention characteristics with OS management.

(+) *Pros*

1) Effective to reduce the refresh power

(-) *Cons*

1) High design complexity

Proposed Scheme

■ Proposed Scheme

Timing Window Wiper(TWW)

**** Key idea***

It captures the row and bank addresses of active commands within a timing window and eliminates the refresh operation of the captured rows within the pre-defined timing window.

(+) *Pros*

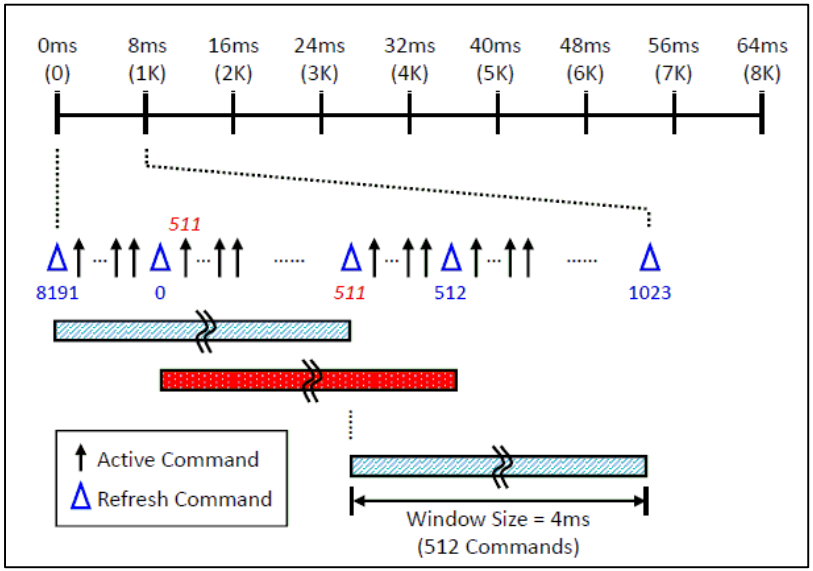
1) Simple to implement

2) Appropriate level of register size

(-) *Cons*

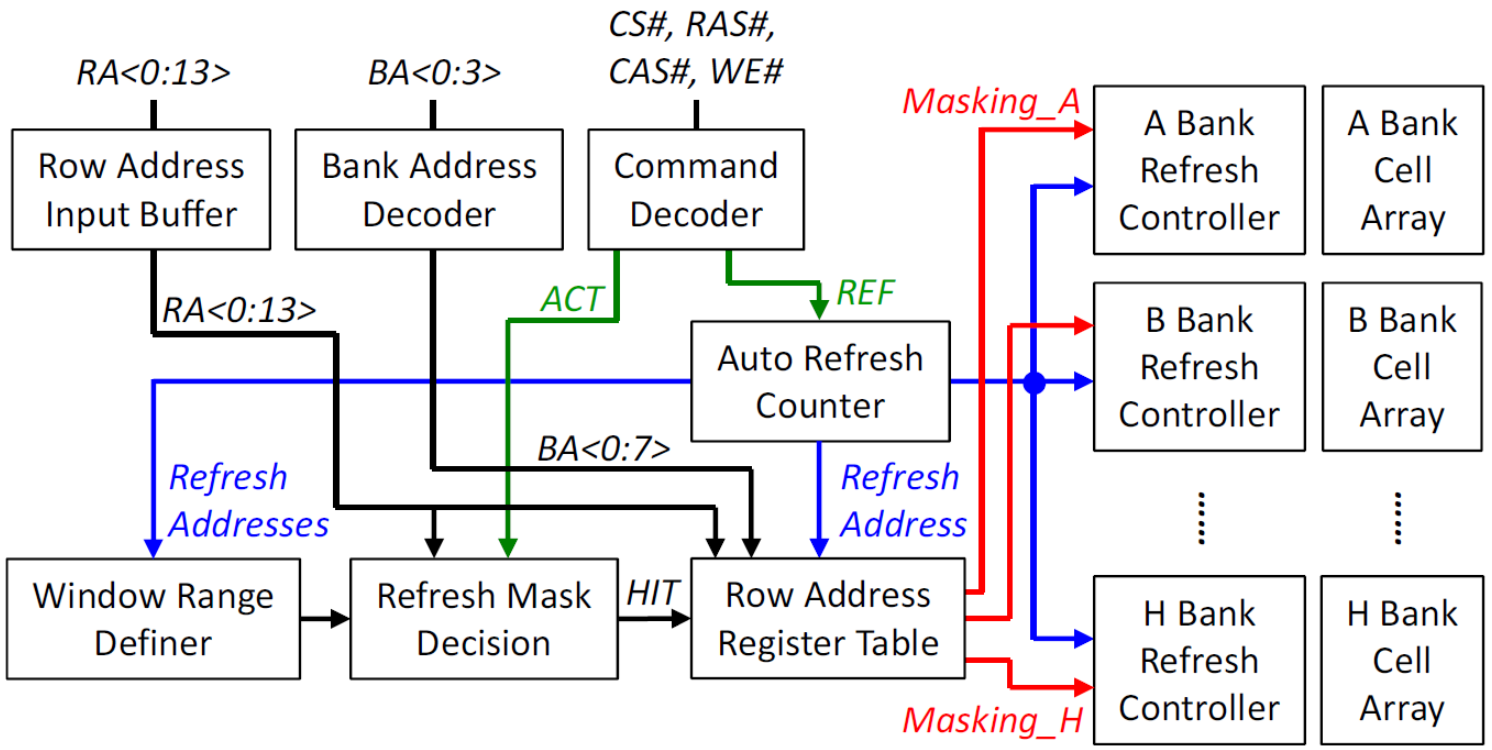
1) Limited effect on refresh power reduction

■ Rationale of TWW



Timing Window Wiper(1)

Overall architecture of TWW in a DRAM device



Timing Window Wiper(2)

TWW Management Algorithm

Algorithm 1 Pseudo code of TWW scheme

INPUT : CMD, BA, RA
// Issued command, bank address and row address

```
WS ← 4096 // Window size (for 32 ms)
RC ← 0 // Refresh address generated by the counter
EntryPt ← 0 // Entry pointer of the register table
while CMD do
    if (CMD = "ACT") then
        // When active command is issued
        if (RA > RC and RA ≤ RC + WS) then
            // If the RA is belonging to the window range
            EntryPt ← SearchRA(RA)
            if (EntryPt.ValidBit = 1) then
                UpdateBA(EntryPt, BA)
            else
                EntryPt ← LowestVacantEntry()
                StoreRA(EntryPt, BA)
                UpdateBA(EntryPt, BA)
                EntryPt.ValidBit = 1
            end if
        end if
    else if CMD = "REF") then
        // When refresh command is issued
        EntryPt ← SearchRA(RA)
        // Find the RA corresponding to the RC
        if (EntryPt ≠ NONE) then
            MaskedBank ← GenerateMaskSignal(EntryPt)
            ClearEntry(EntryPt)
            RC++
        end if
    end if
end while
```

Row Address Register Table (RART)

	Valid	Row Address Bit Table													Bank Address Table							
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	A	B	C	D	E	F	G	H
Entry 1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⋮																						
Entry N	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

RART size = {1 + RA + (BA X REF)} X N

RA : the number of row address bits

BA : the number of banks

REF : the number of simultaneous refresh rows in a bank

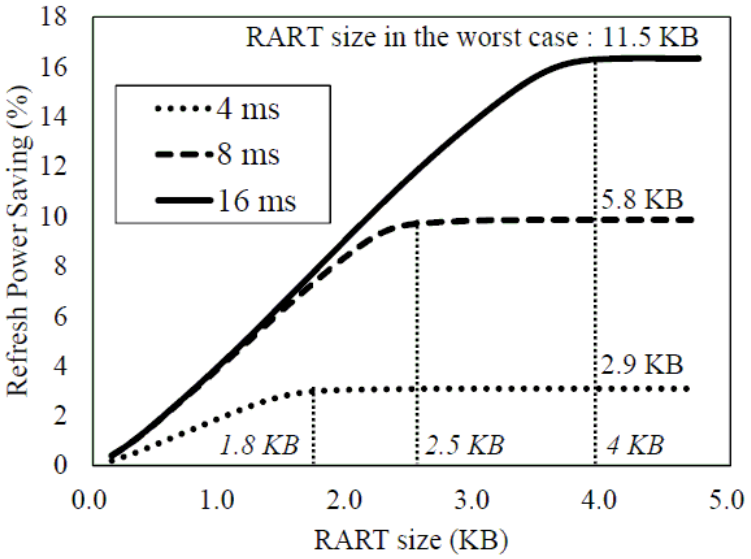
N : the number of entries (= refresh commands in a timing window)

Ex) Capacity = 4GB & Window Size = 32 ms

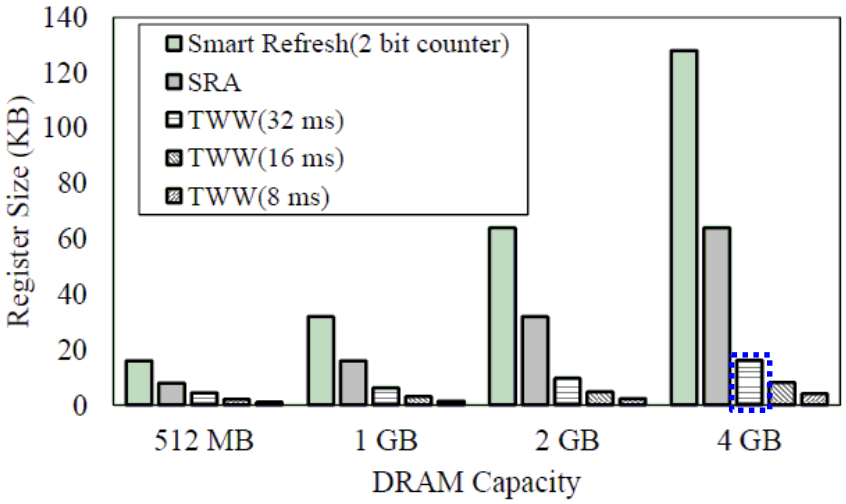
→ {1 + 16 + (8 X 8)} X 4096 = 40.5KB (Worst Case)

Timing Window Wiper(3)

■ Exploration of the RART size



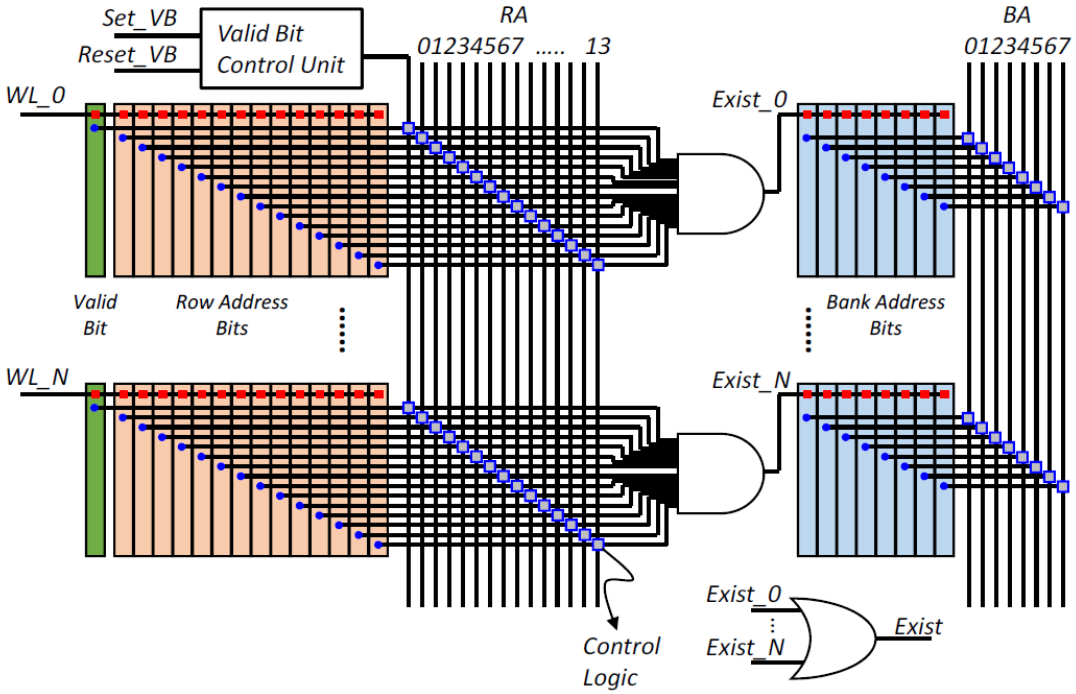
40% of the worst case size is enough

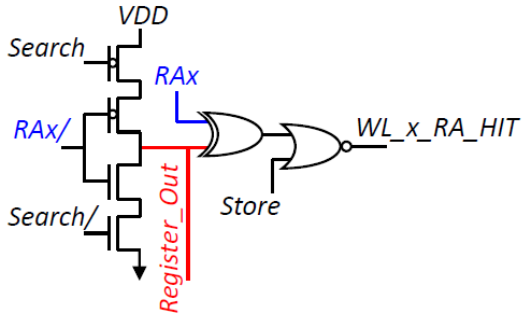


40.5 KB (worst case) → 16.2 KB

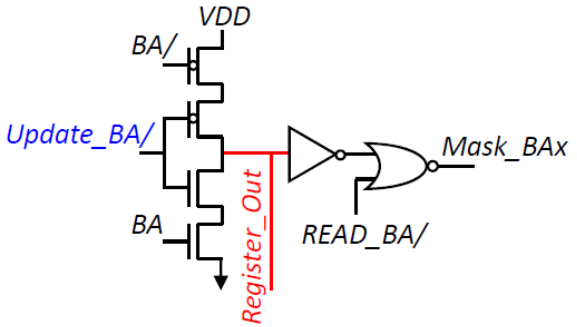
Timing Window Wiper(4)

Control Logic of RART





(a) Control logic circuit for the row address register



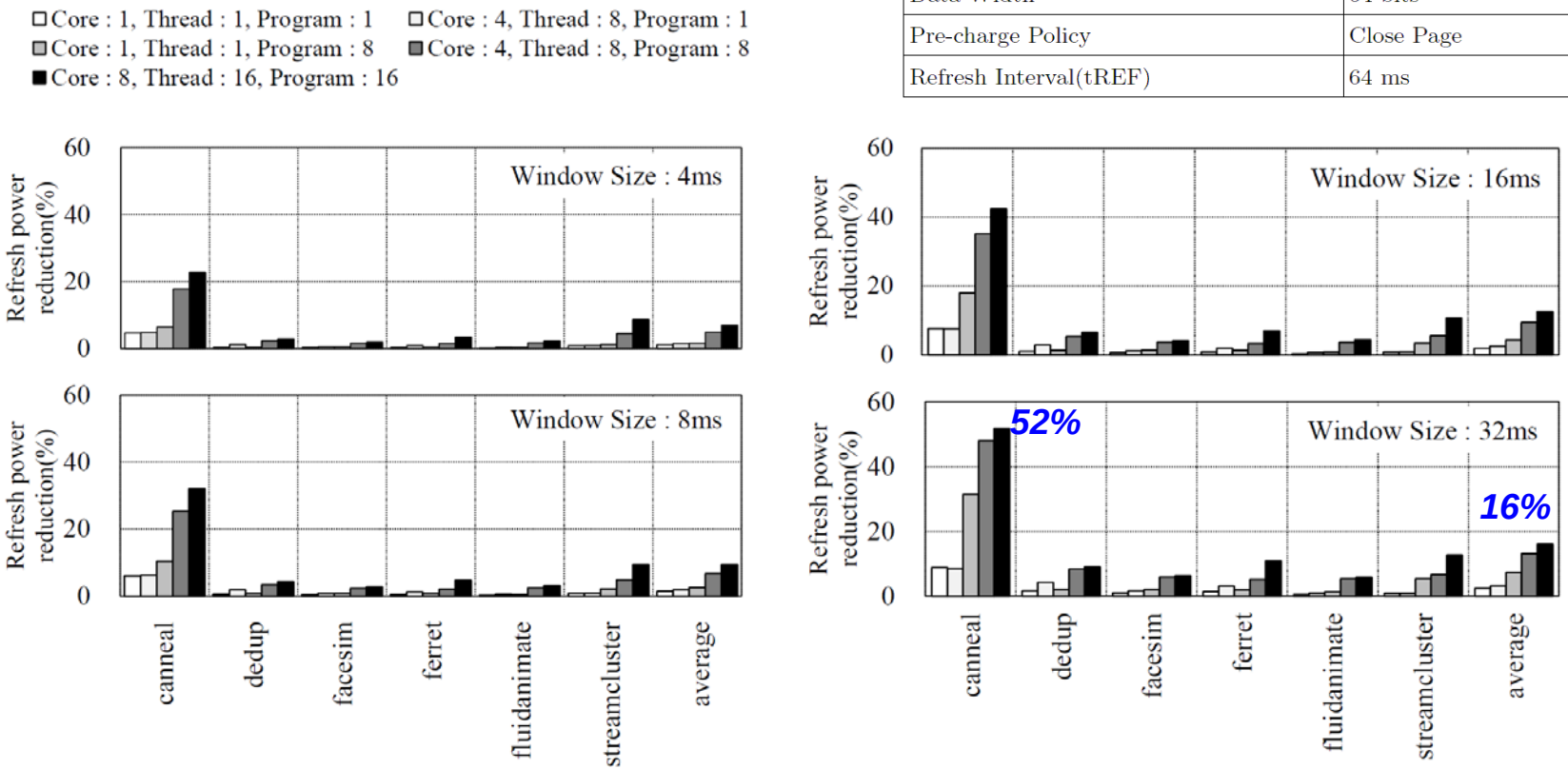
(b) Control logic circuit for the bank address register

Experiment Result

Experiment Result

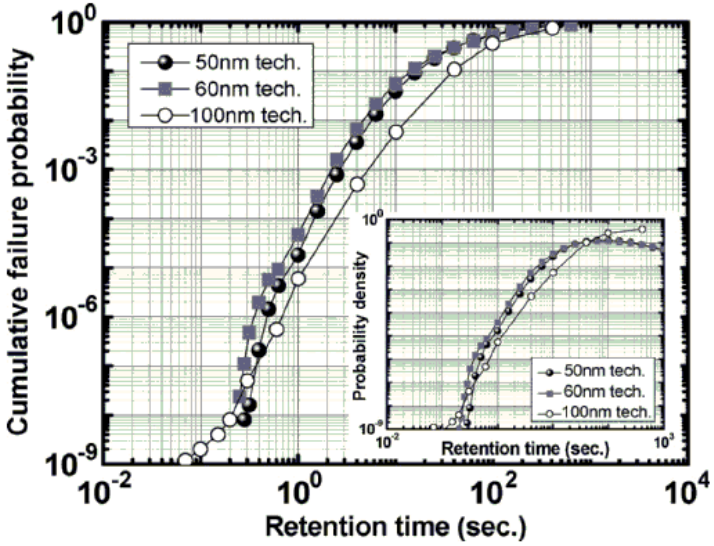
System Configurations for Experiments

CPU Type/Frequency	Alpha/2 GHz
DRAM Type/Capacity/Frequency	DDR3/1 GB/667 MHz
Number of Banks/Ranks/Rows/Columns	8/1/16384/8102
Data Width	64 bits
Pre-charge Policy	Close Page
Refresh Interval(tREF)	64 ms



Risk Management

■ Risk Management



- *TWW increases the DRAM retention time to 64 ms + window size.*
- *The number of cells (tREF < 100 ms) : dozens of bits for 1Gb devices. (see Fig.)*
- *Exploit e-fuse for storing the risky rows*

* K. Kim and J. Lee, “A New Investigation of Data Retention Time in Truly Nanoscaled DRAMs," IEEE Electron Device Letters, vol. 30, pp. 846-848, Aug. 2009.

Conclusion

Conclusion

[Performance]

TWW can reduce the average refresh power by up to 16%.
(Register Size = 6.2KB)

[Compatibility]

TWW can be implemented without modifying the DRAM controller or the OS.

Q & A