Guiding Template-aware Routing Considering Redundant Via Insertion for Directed Self-Assembly

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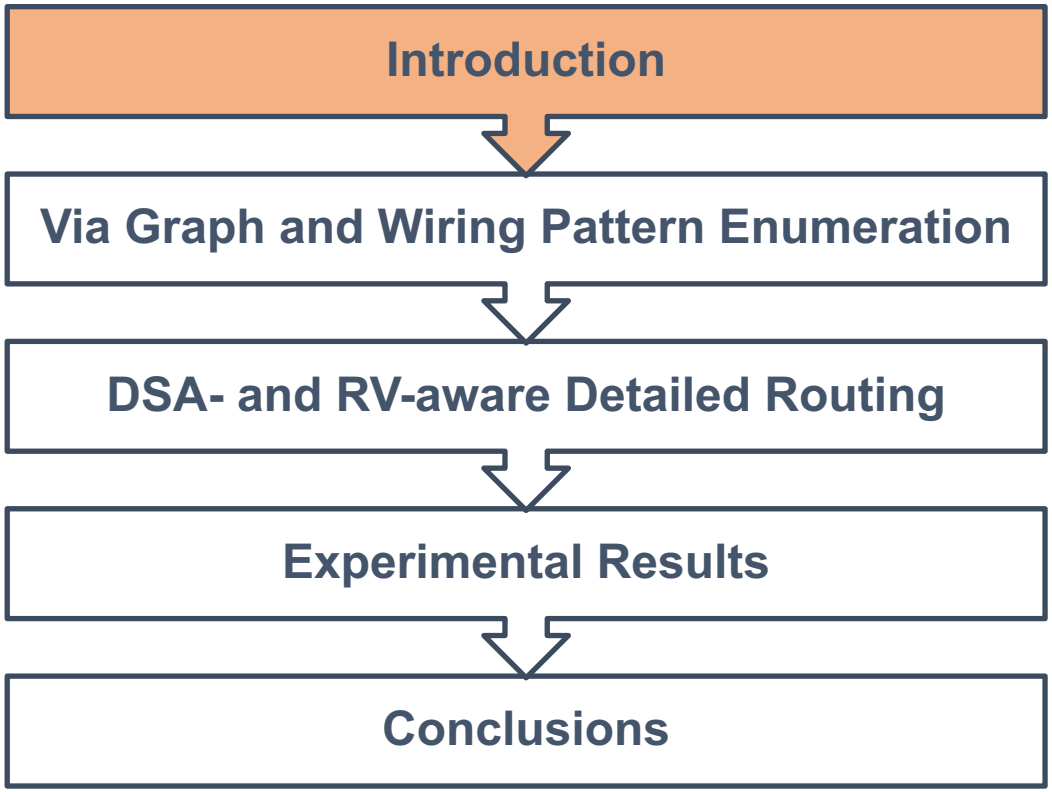
Outline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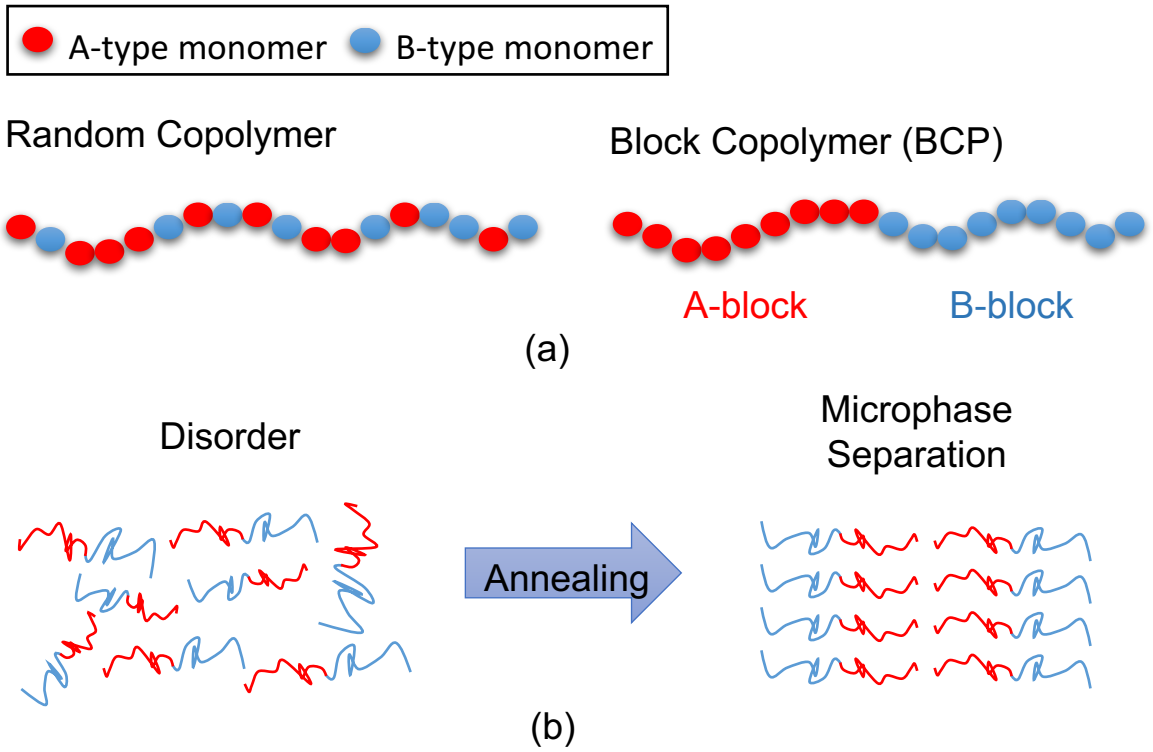
Via Graph and Wiring Pattern Enumeration
DSA- and RV-aware Detailed Routing
Experimental Results
Conclusions

Block Copolymer Directed Self-Assembly

- Block copolymer directed self-assembly (DSA) is one of Next Generation Lithography (NGL) technologies
  - Common material: PS-b-PMMA (polystyrene-block-polymethyl methacrylate)



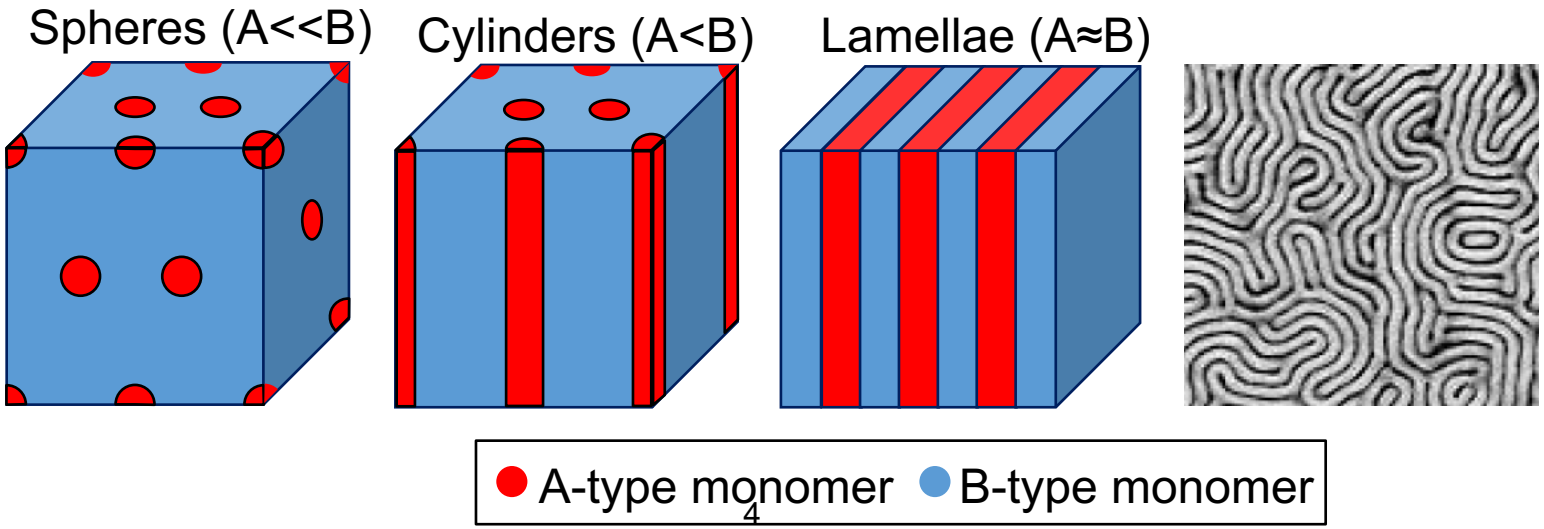
Different DSA Morphologies

- Different proportions of block components form different DSA morphologies

  (a) Spherical (A << B)

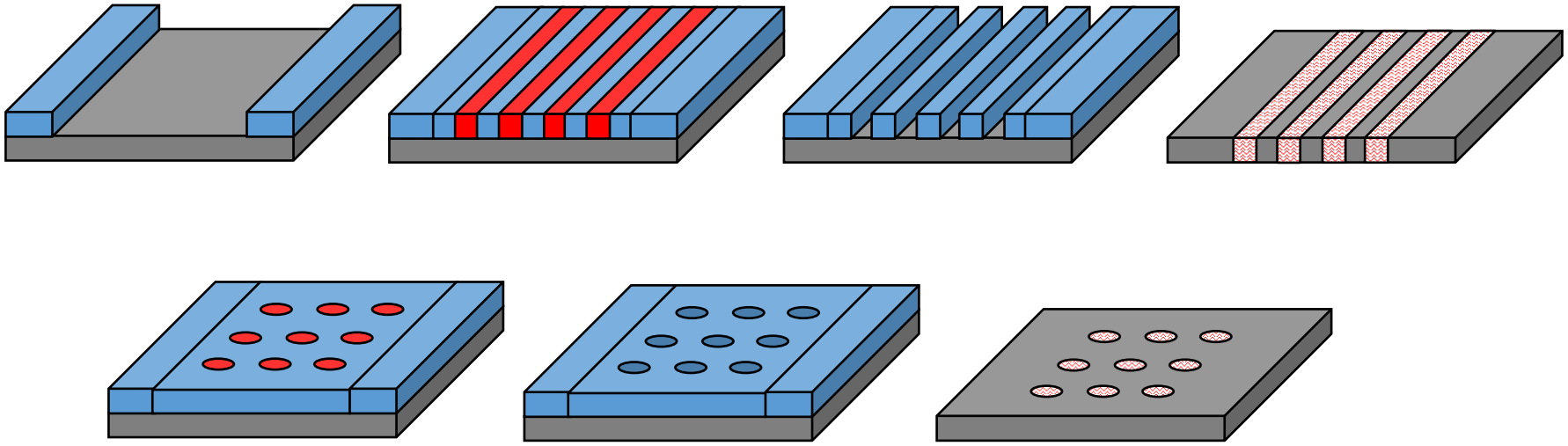
  (b) Cylinders (A < B)

  (c) Lamellae (A ≈ B)



Guiding Templates in DSA

- Guiding patterns are used to provide additional driving forces to turn random fingerprints into highly orientated and aligned patterns



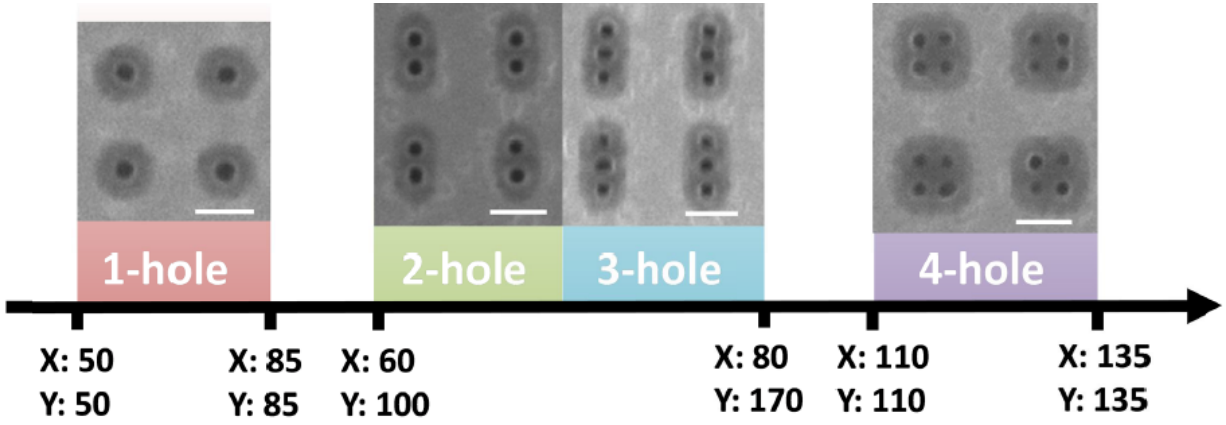
DSA Template Design Strategies

(1) Surround each via with a guiding template

- Require higher lithographic resolution for template fabrication

(2) Design larger templates for closely positioned vias

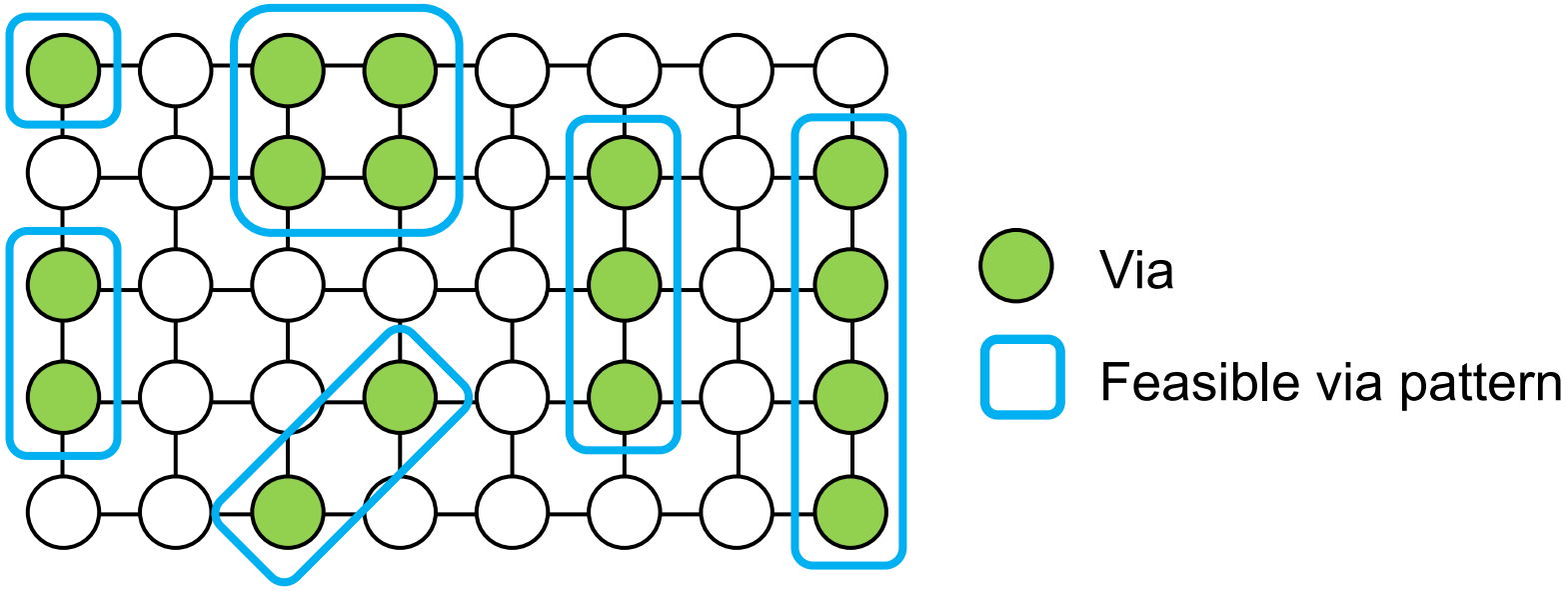
- Relax the resolution requirement but the pitch of DSA holes must match the contact pitch in the layout



An axis showing the range of template sizes for generating DSA patterns from 1 hole to 4 holes
X: template width, Y: template length (nm) [Yi et al., SPIE'13]

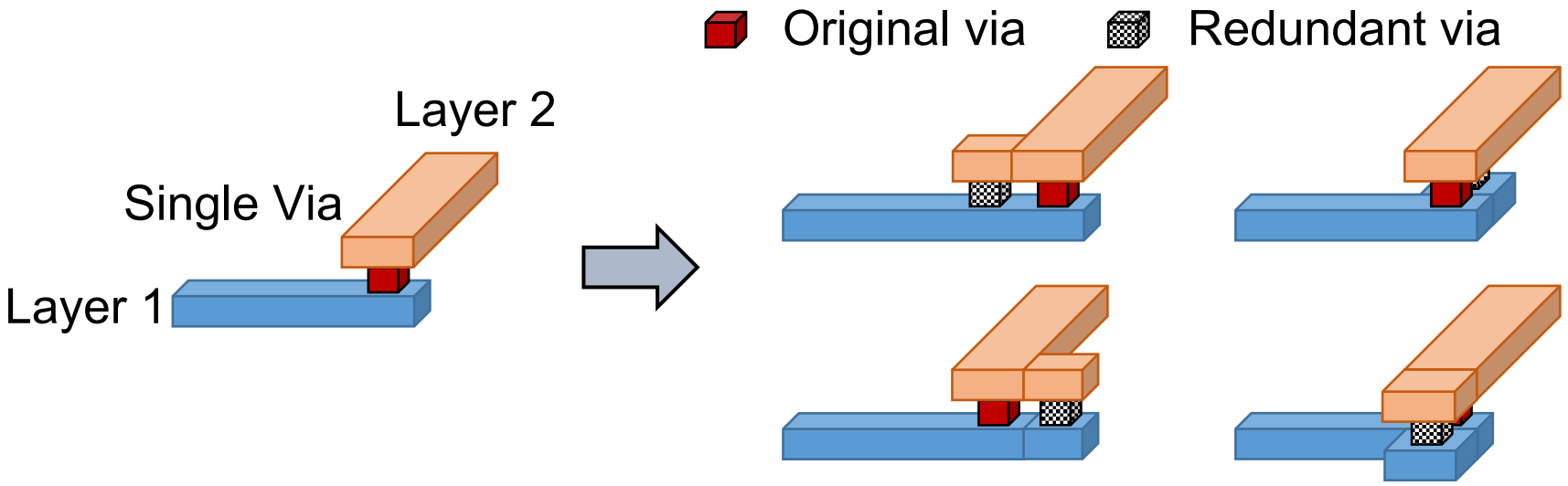
DSA Feasible Via Patterns

- Not every via pattern can be well generated with guiding templates
- We consider six types of DSA feasible via patterns, which are highly oriented and aligned



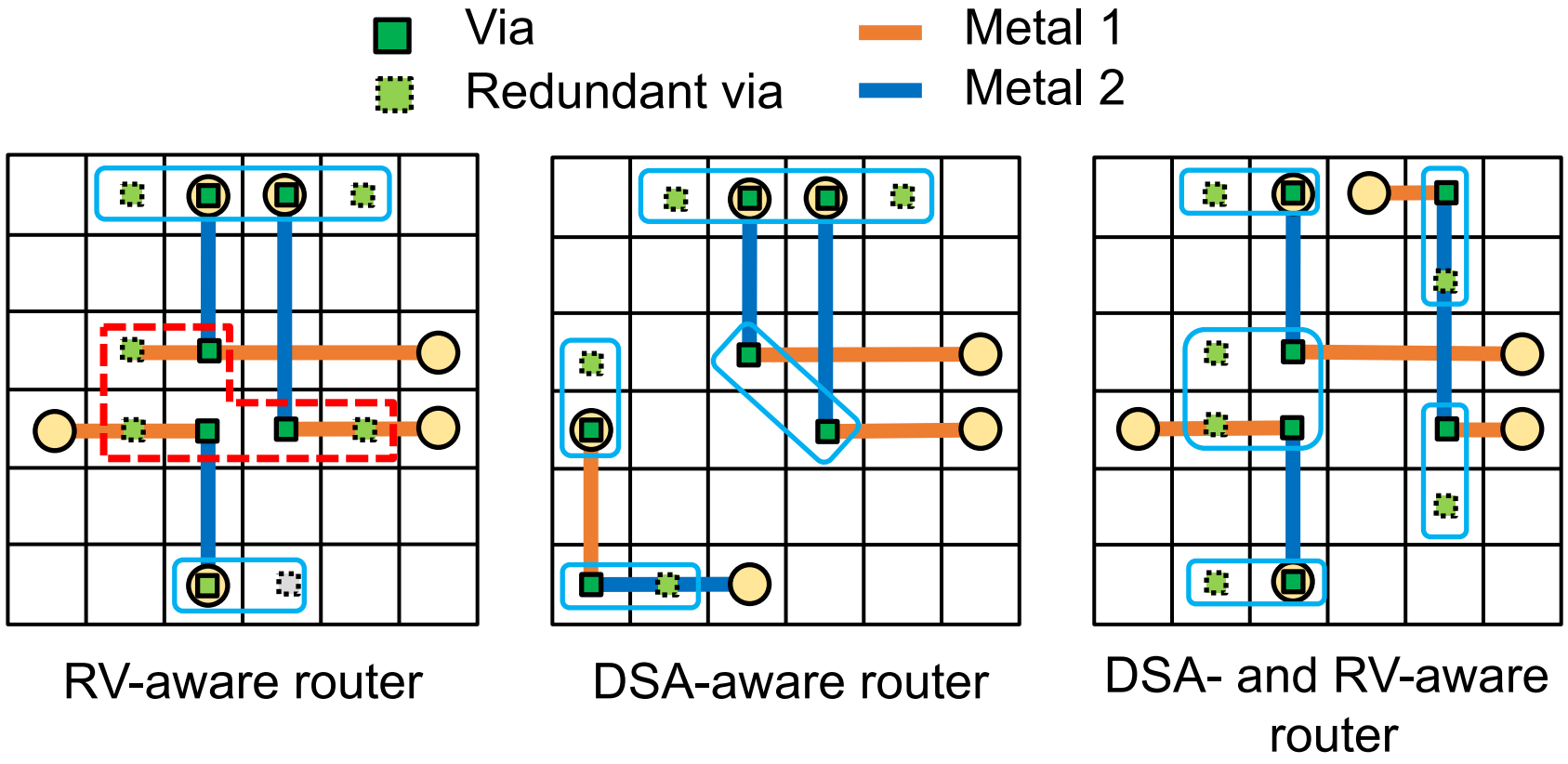
Redundant Via (RV) Insertion

- RV insertion has become a necessary step
  - Improve yield and circuit reliability
  - Serve as the back up of an original via
- Inserting an RV has to avoid any short circuit problem and design rule violation
- An original via has at most 4 RV candidates



DSA- and RV-aware Routing

- Routing by only considering either DSA or RV is not sufficient
- A DSA- and RV-aware router is desirable



Contributions

- *The first work of detailed routing considering DSA via manufacturability and RV insertion*
  - Propose ***a sophisticated routing graph*** model to avoid generating undesired wiring patterns
  - Propose ***a trunk assignment method*** for better via planning
  - Propose several rip-up and rerouting techniques for via layout optimization
  - Experimental results demonstrate the effectiveness and the practicality of our method

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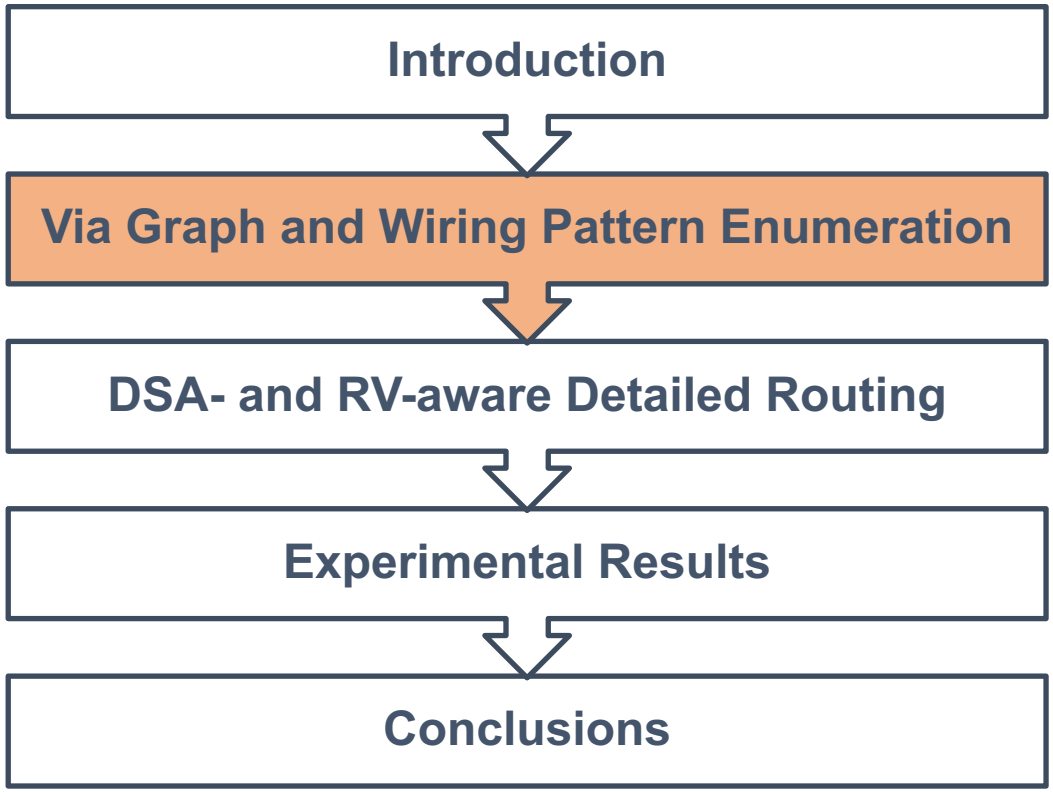
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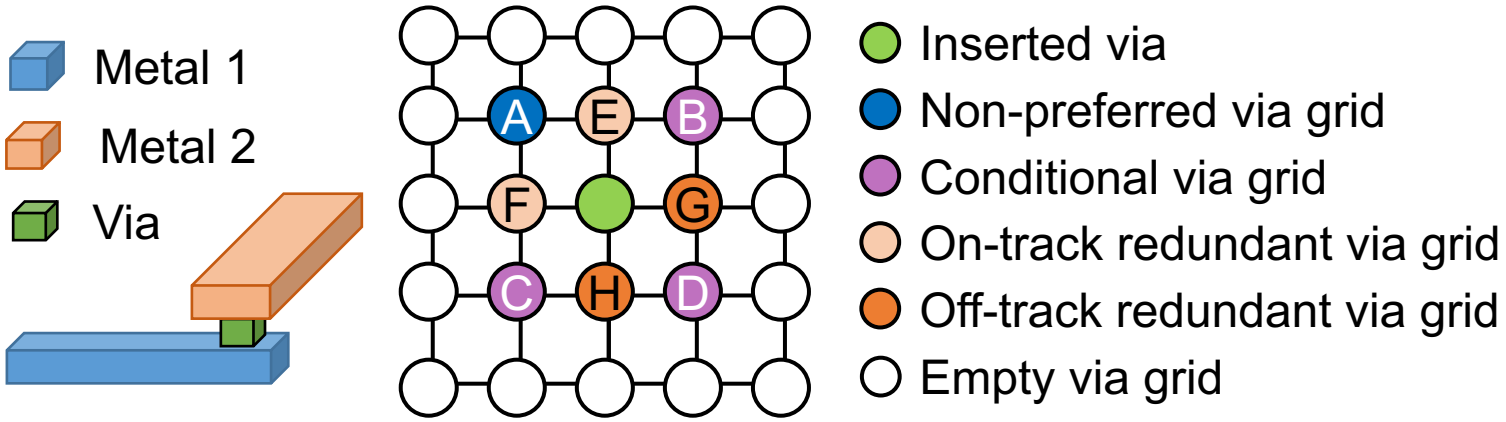
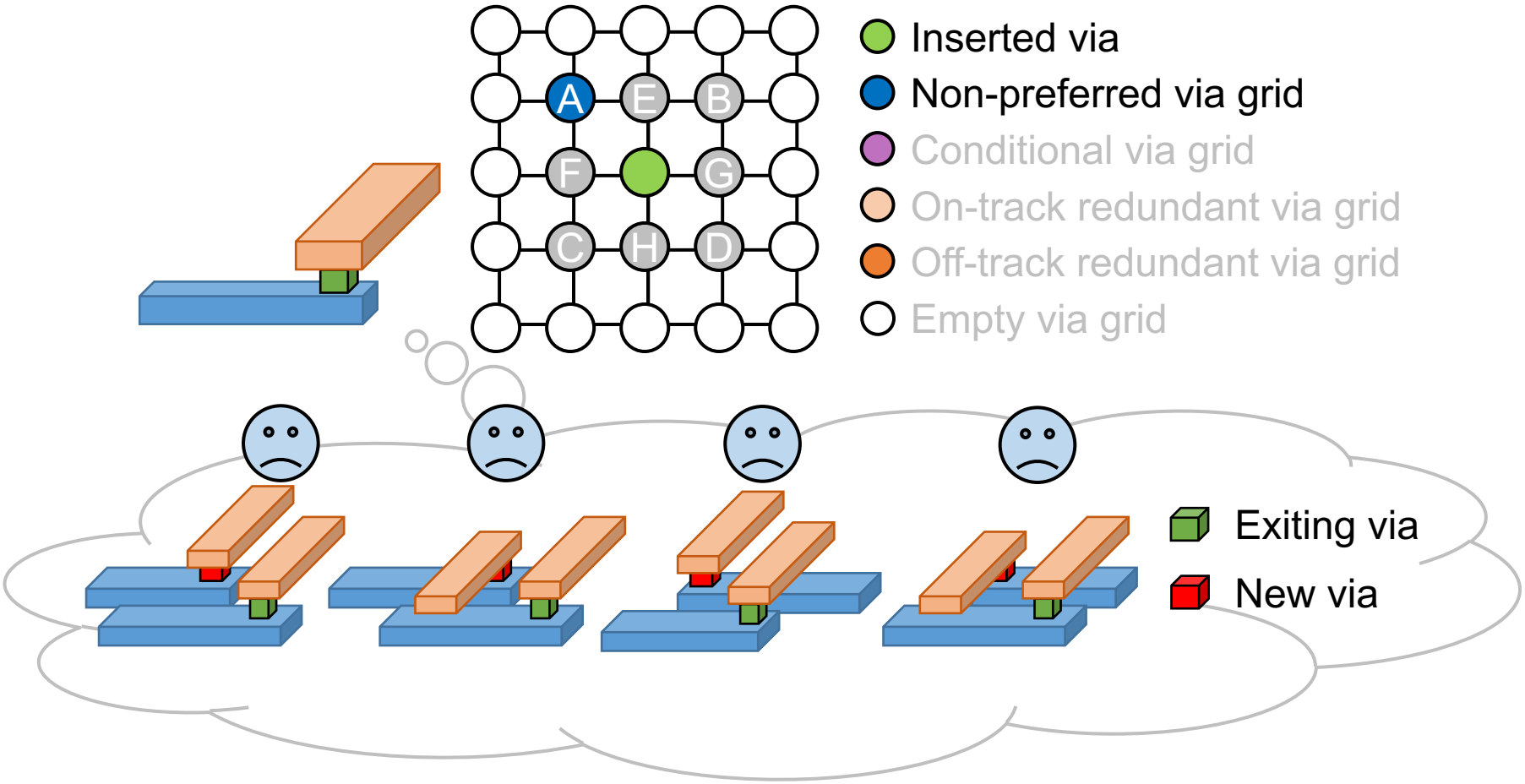
Via Graph

- One-dimensional routing is assumed
  - A via is required to connect a horizontal wire segment and a vertical wire segment in adjacent layers
- Four directions of a wire segment connection: top-left, top-right, bottom-left, bottom-right
- A via graph is used to indicate different via statuses



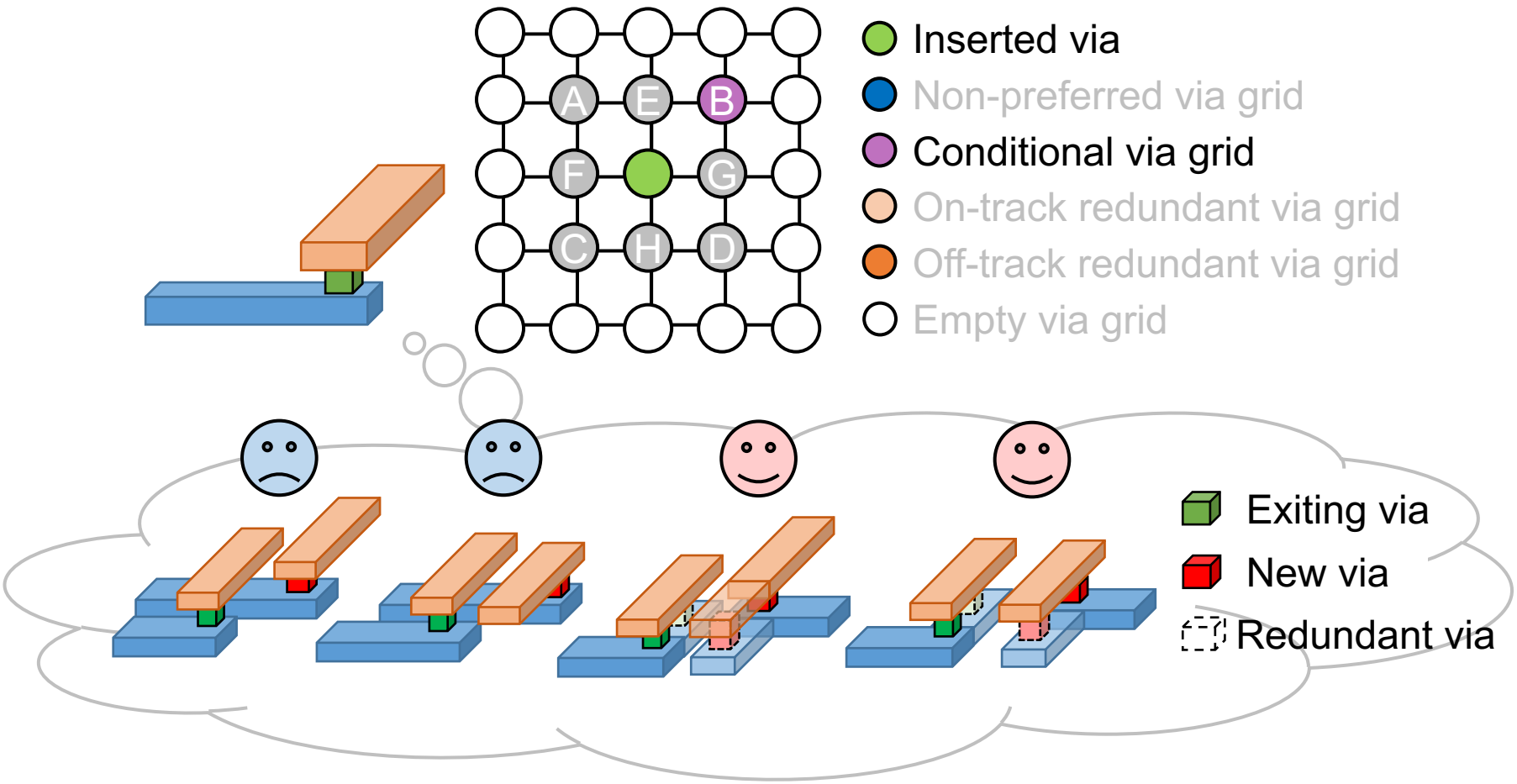
Non-Preferred Via Grid

- Non-preferred via grid: a new via inserted at a non-preferred via grid results in two dead vias, regardless of connection directions



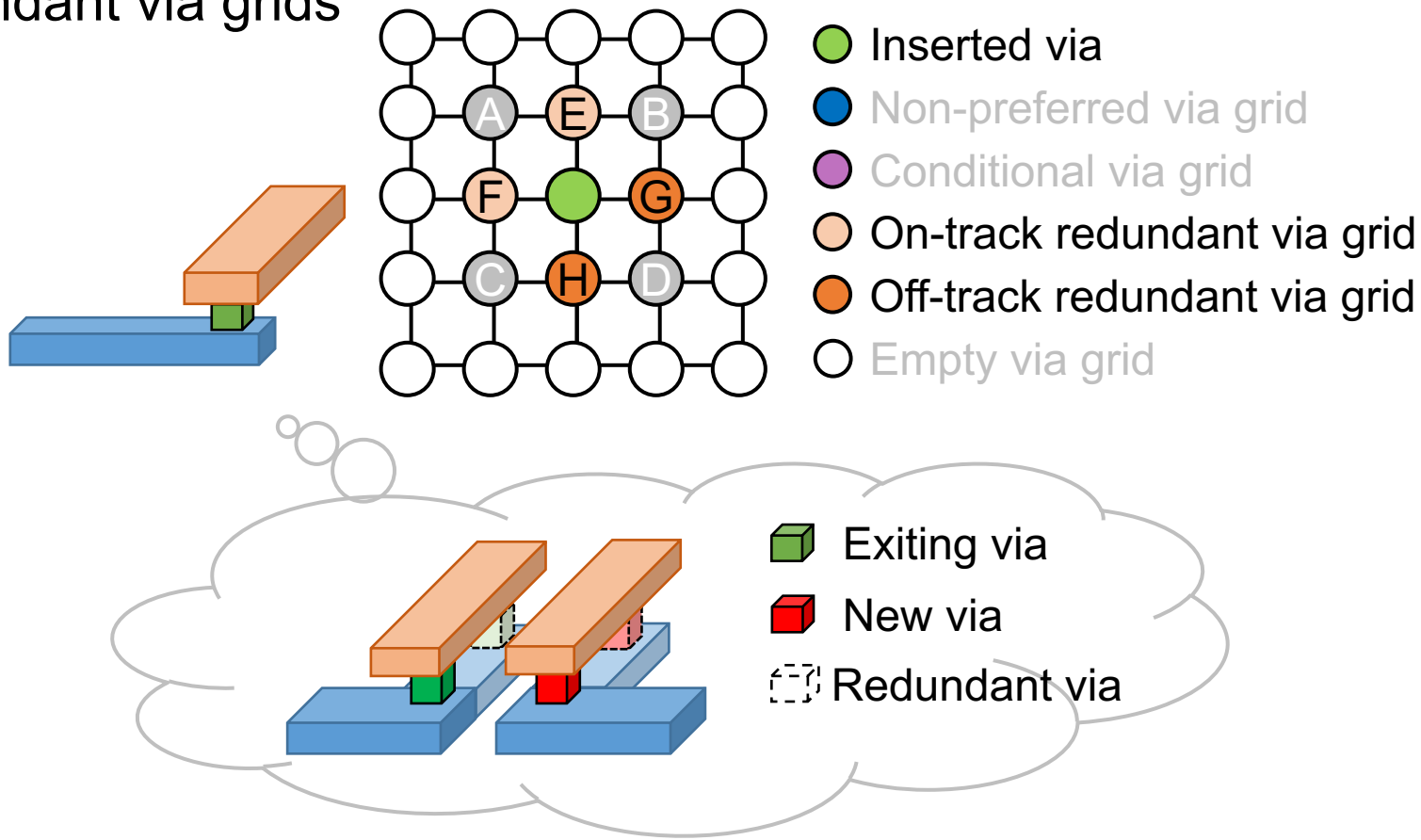
Conditional Via Grid

- Conditional via grid: whether a new via should be inserted depends on the direction of a wire connection



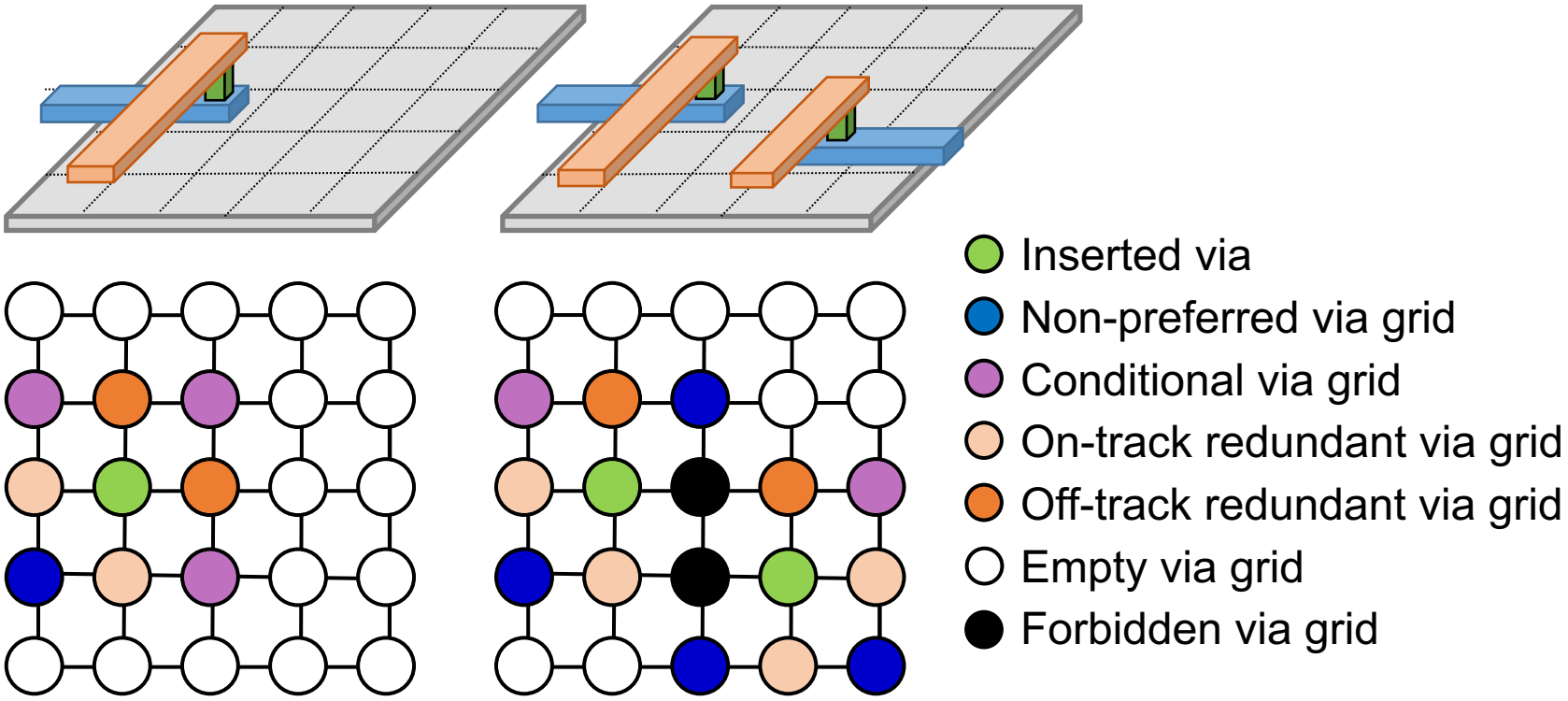
On-/Off-Track Via Grid

- On-track via grid: no via of other connections can be inserted
- Off-track via grid: all the connection directions are favorable
- Additional cost should be added to wire routing upon/below redundant via grids



Via Graph Update

- The via graph is updated after routing each net
- Forbidden via grid: no via can be inserted to guarantee via manufacturability



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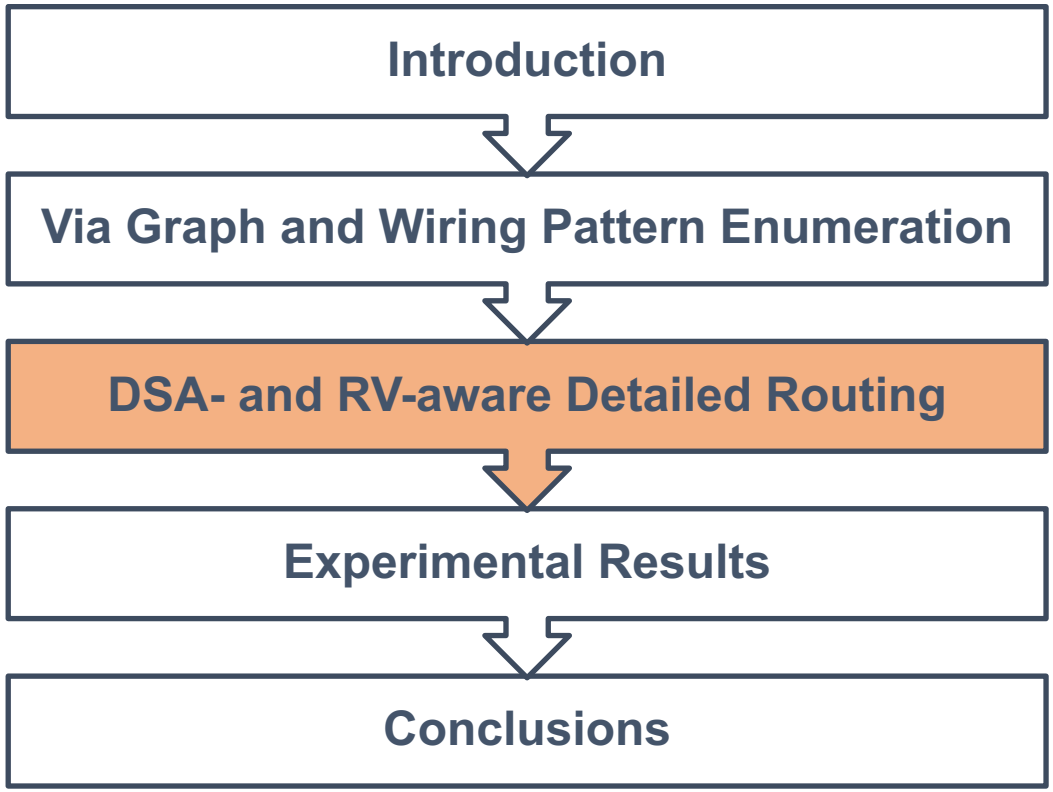
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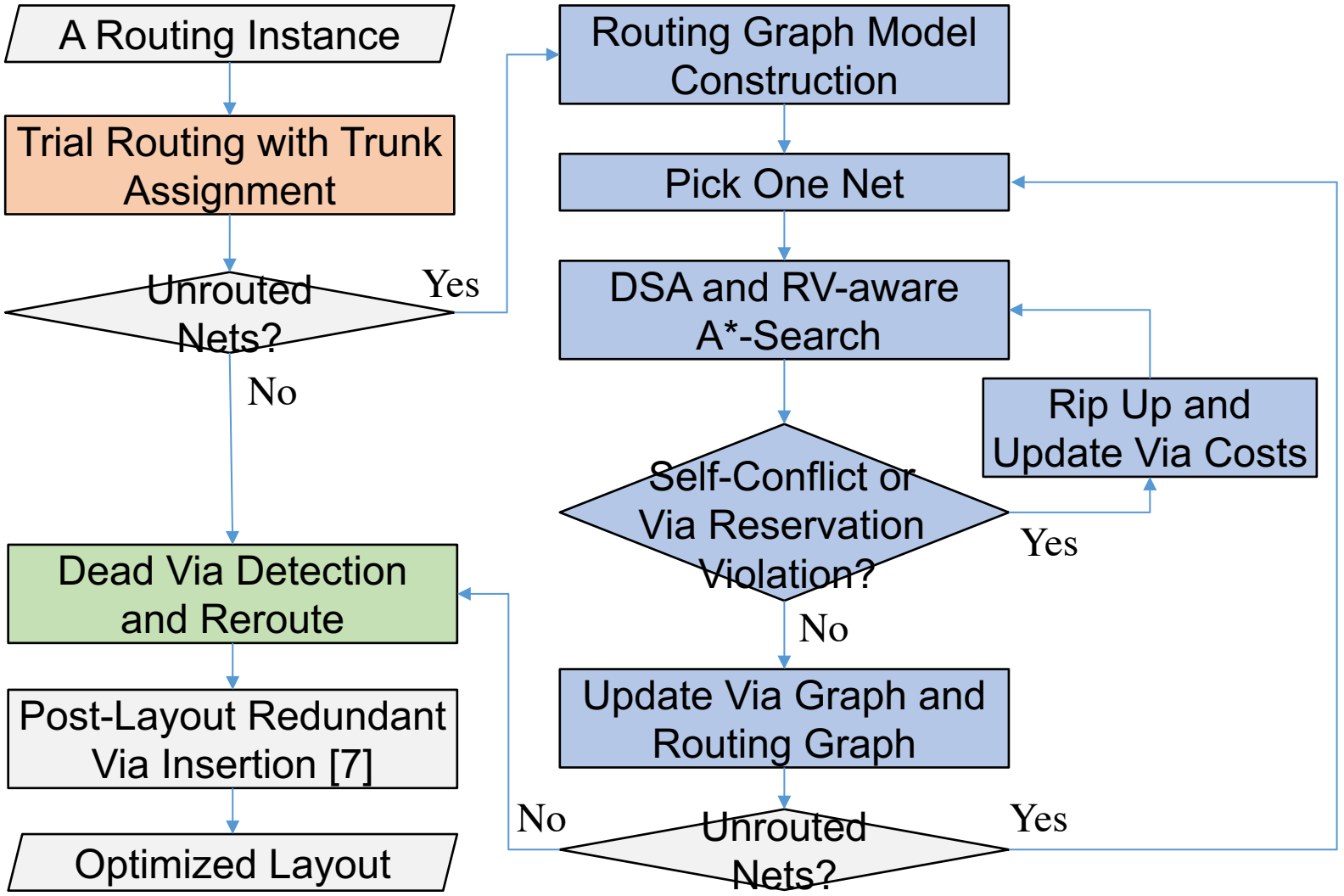

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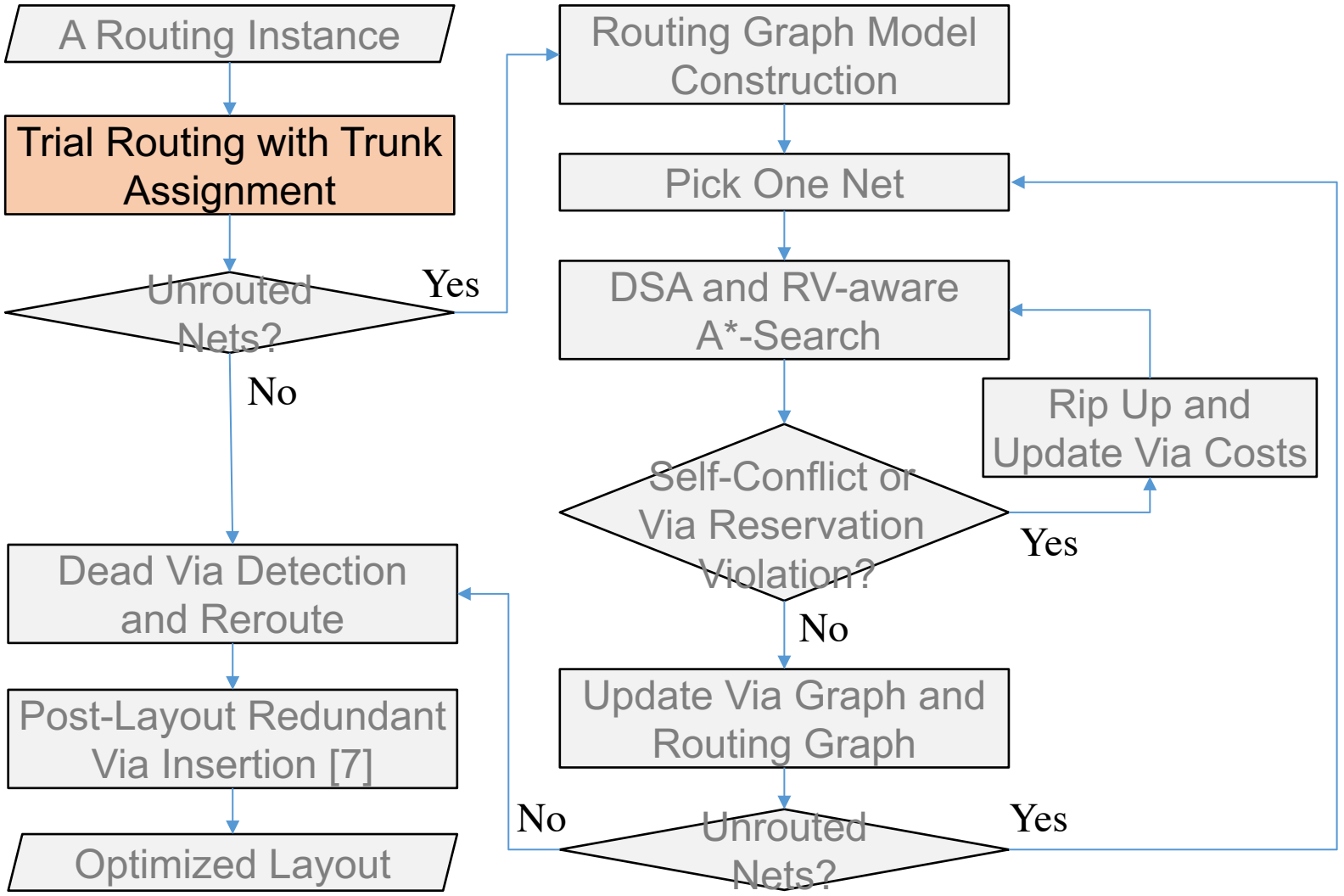
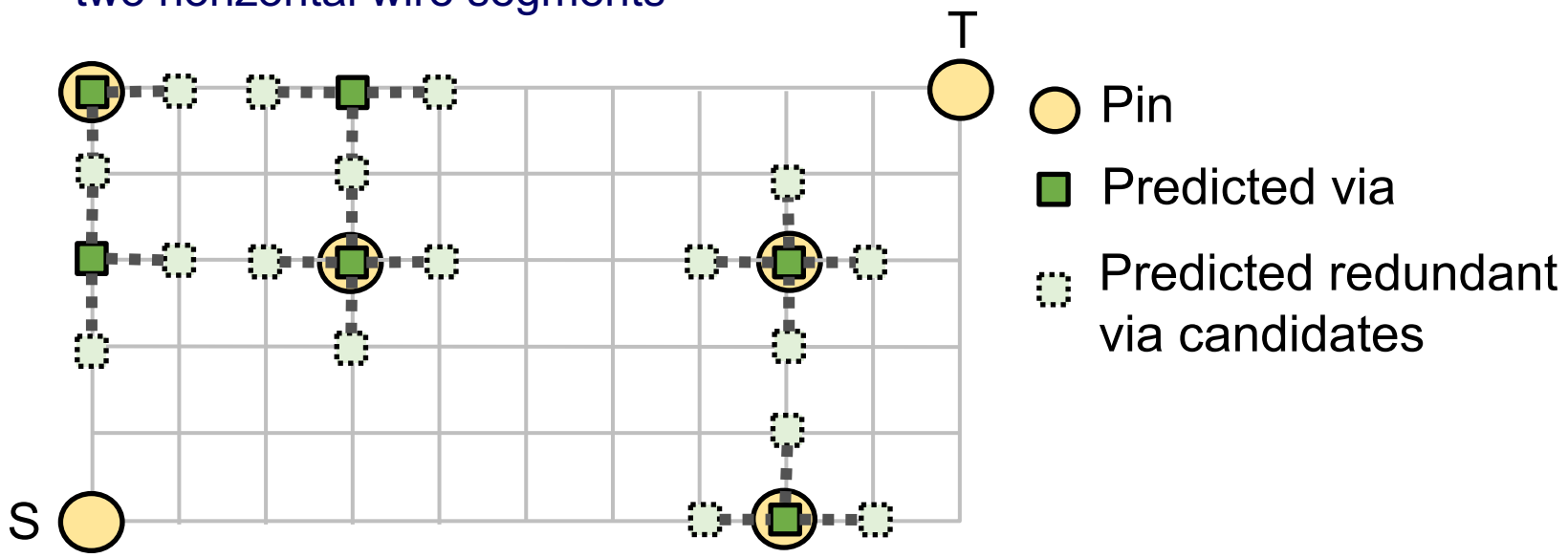


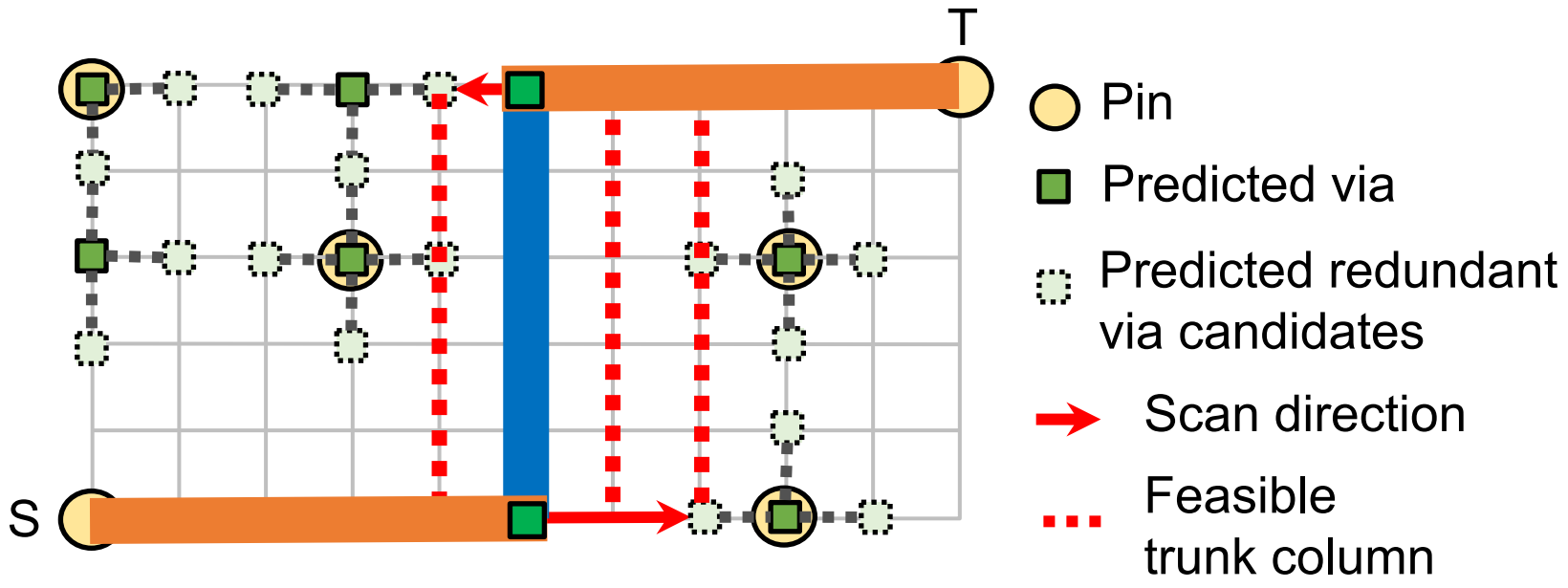
Trunk Assignment

- Assume each net has the highest probability to be in L-shaped such that wirelength and vias are minimized
  $\Longrightarrow$ *Via and RV positions can be predicted*
- Try to route each net in L-shape and Z-shape
  - Only consider a Z-shaped route composed of one vertical ***(trunk)*** and two horizontal wire segments



Trunk Assignment (cont'd)

- Scan the columns from *S*/*T* to the right/left and stop as a predicted via is encountered
- Some feasible trunk columns exist if two scan lines are vertically overlapped
- A route sacrificing the least predicted RV candidates is chosen



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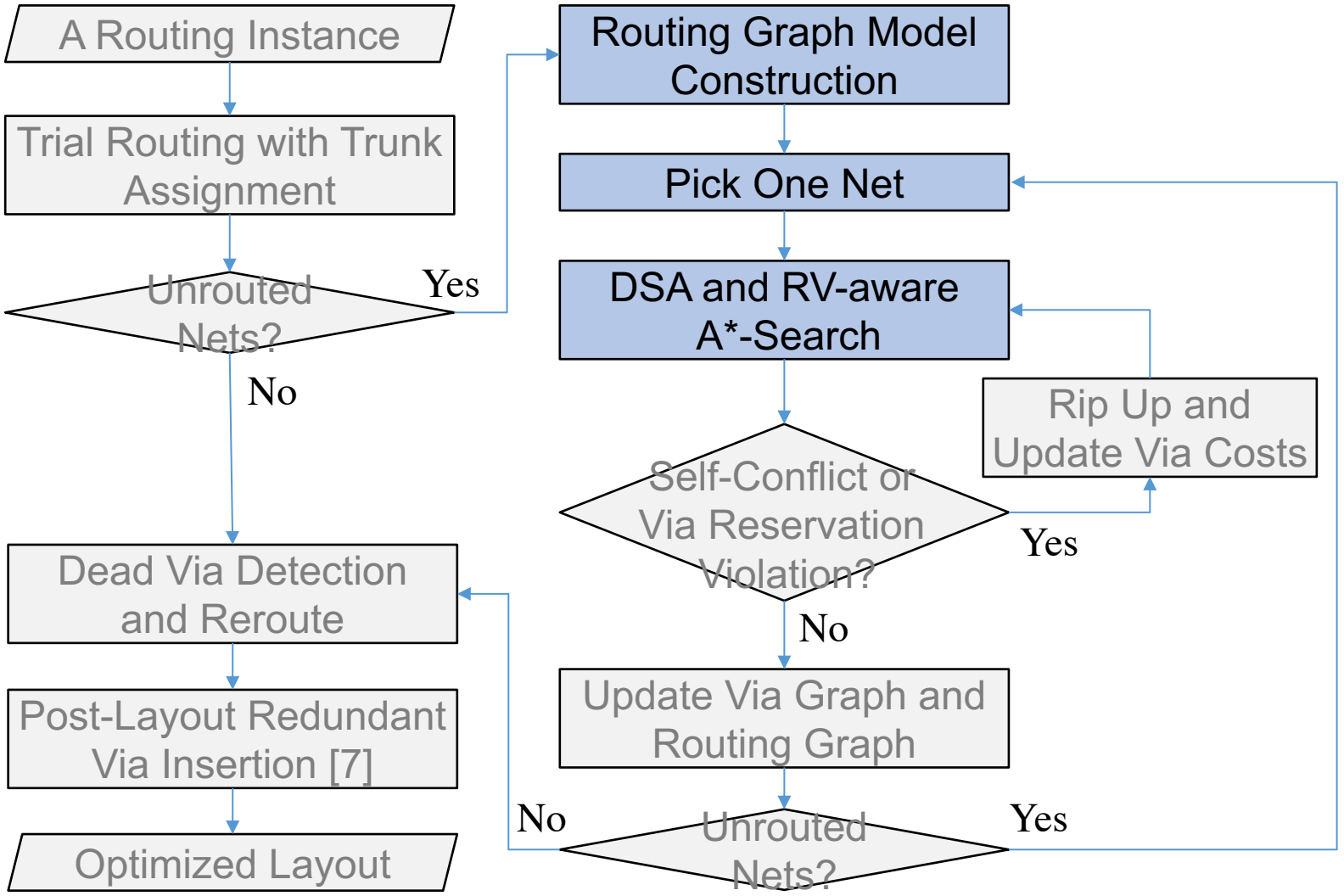
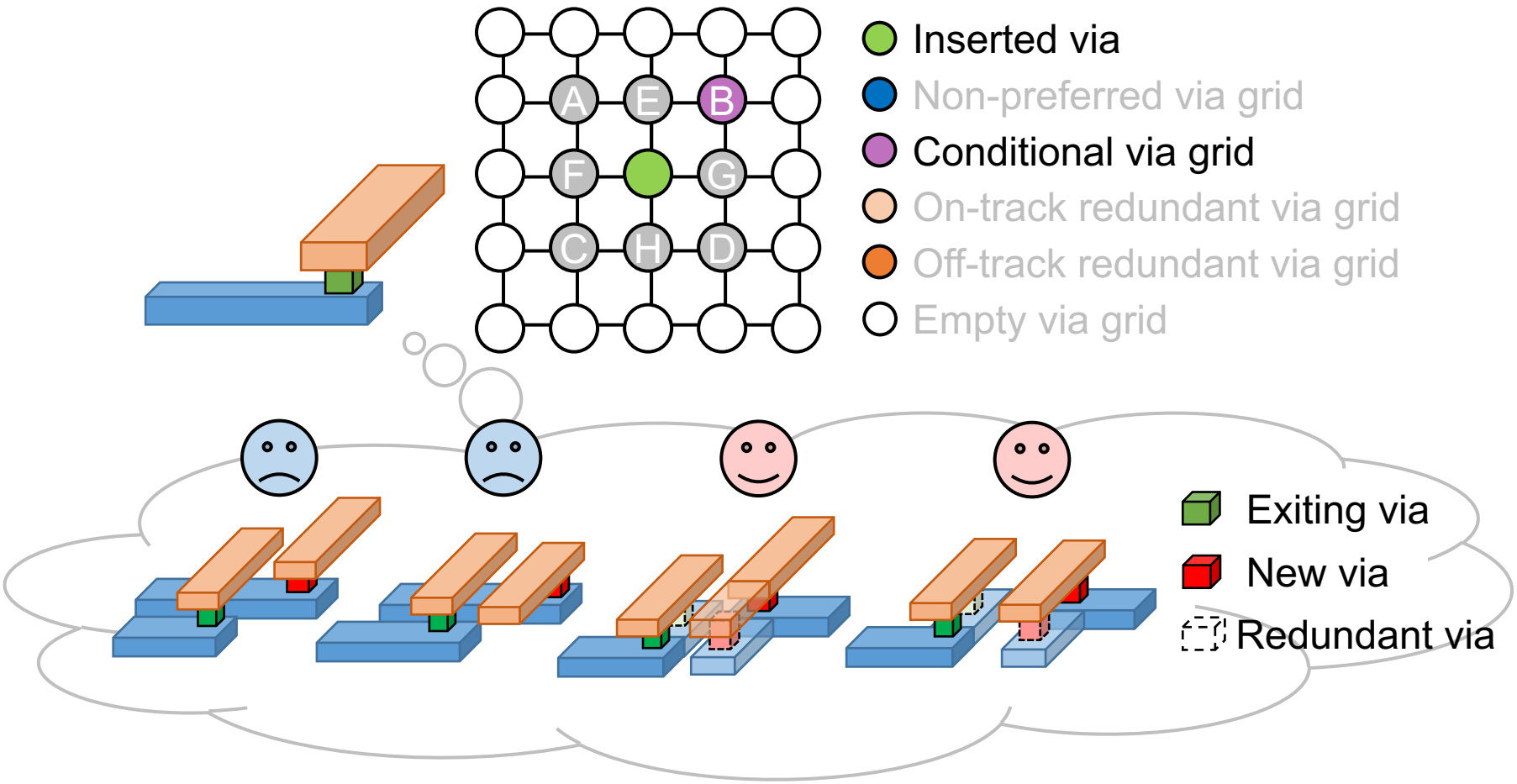


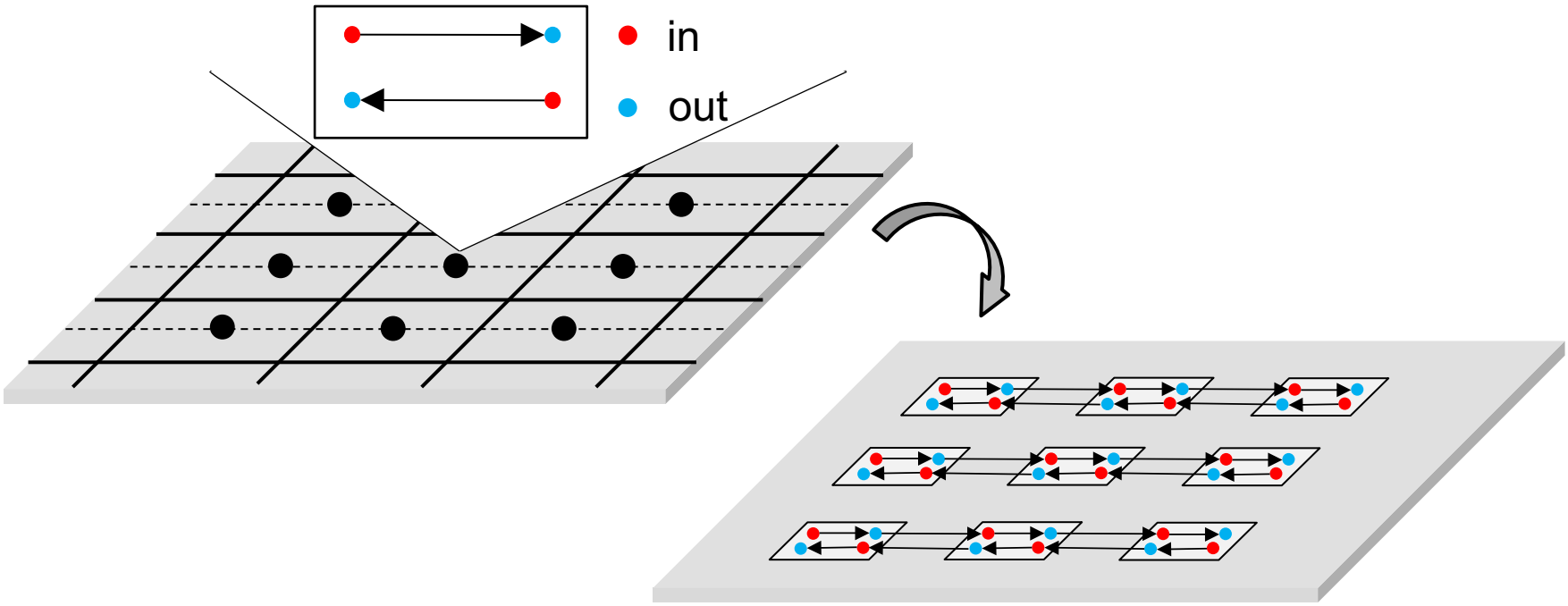
Insufficiency of Via Graphs

- A via graph only indicates via statuses but cannot distinguish differentiate different wire connection directions



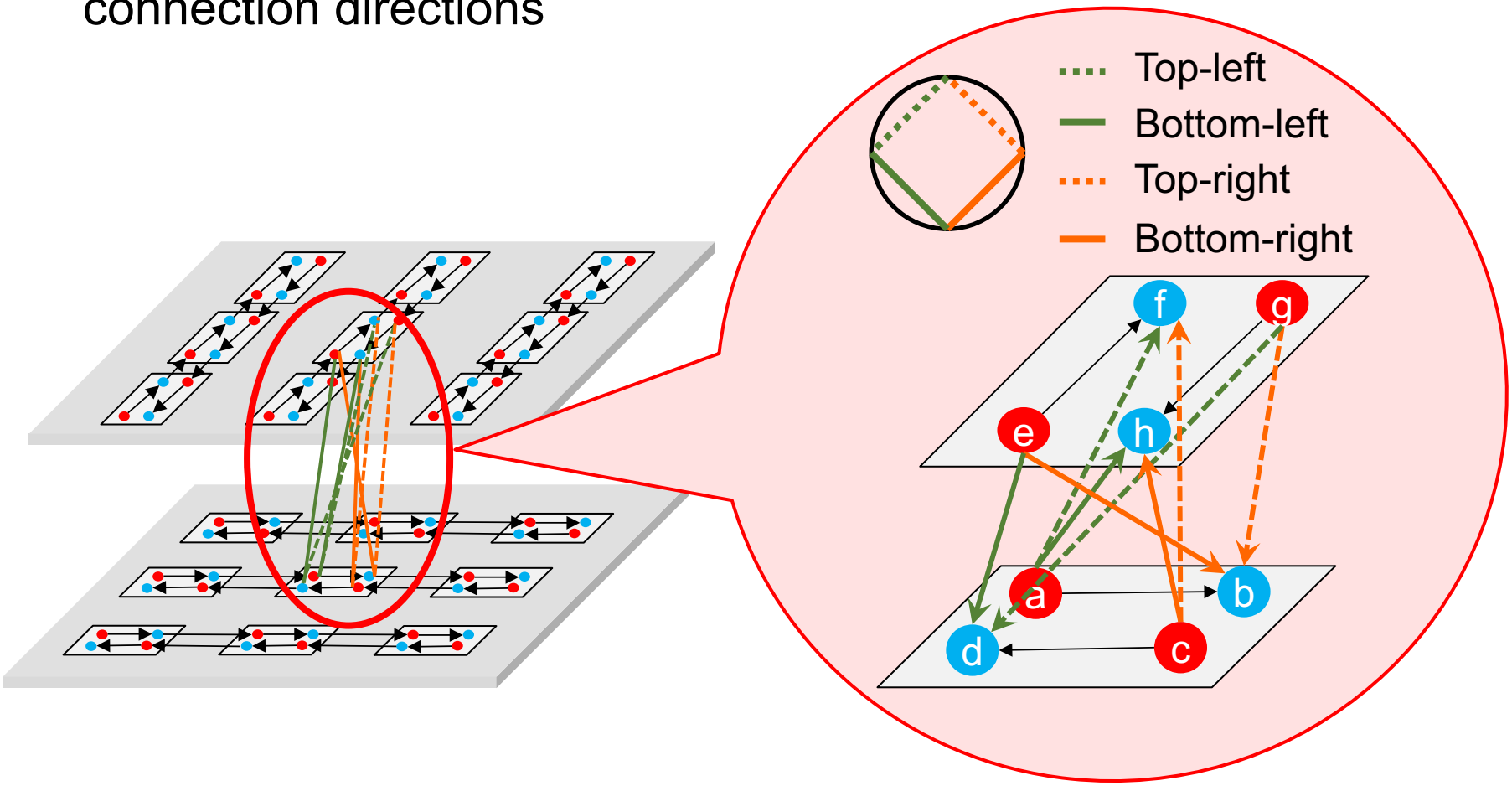
Routing Grid Model

- A novel routing graph model is proposed
- The model for each routing grid
  - Two in-vertices and two out-vertices
  - Directed edges pointed from in-vertices to out-vertices



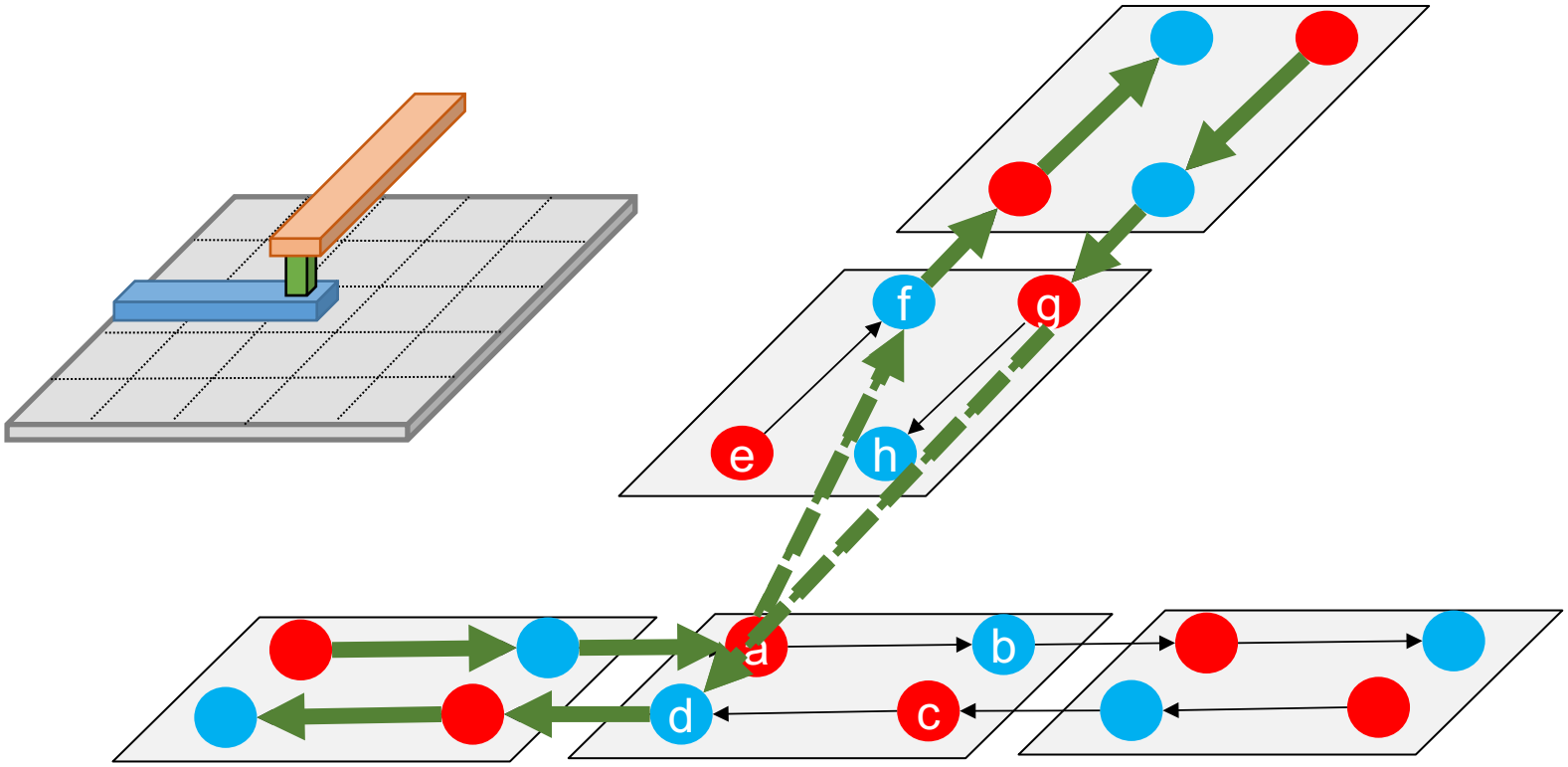
Overall Routing Graph Model

- The grid models are connected across different layers
- Four types of cross-layer connections represent four connection directions



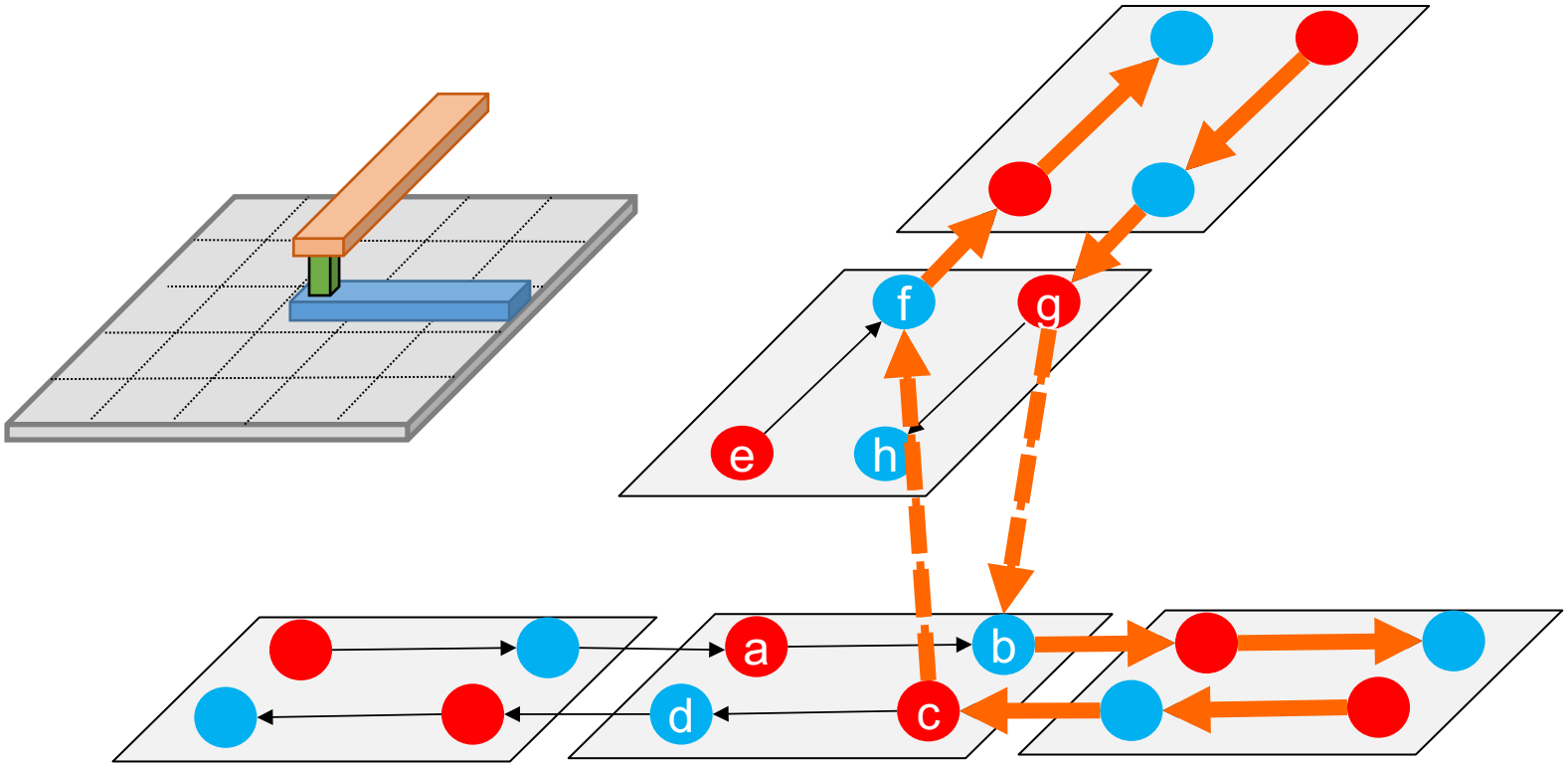
Propagation Example

- A propagation example for a top-left connection



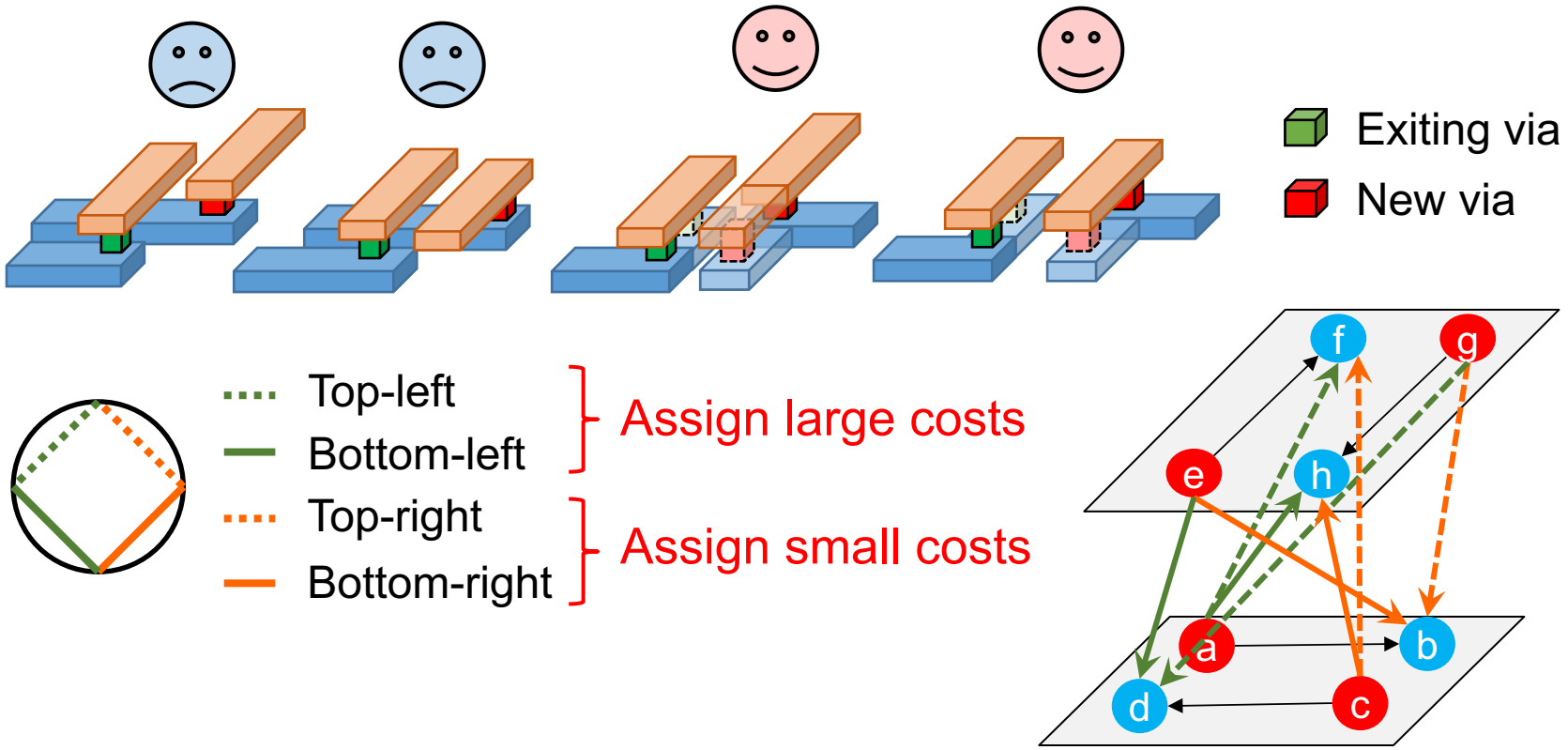
Propagation Example (cont'd)

- A propagation example for a top-right connection



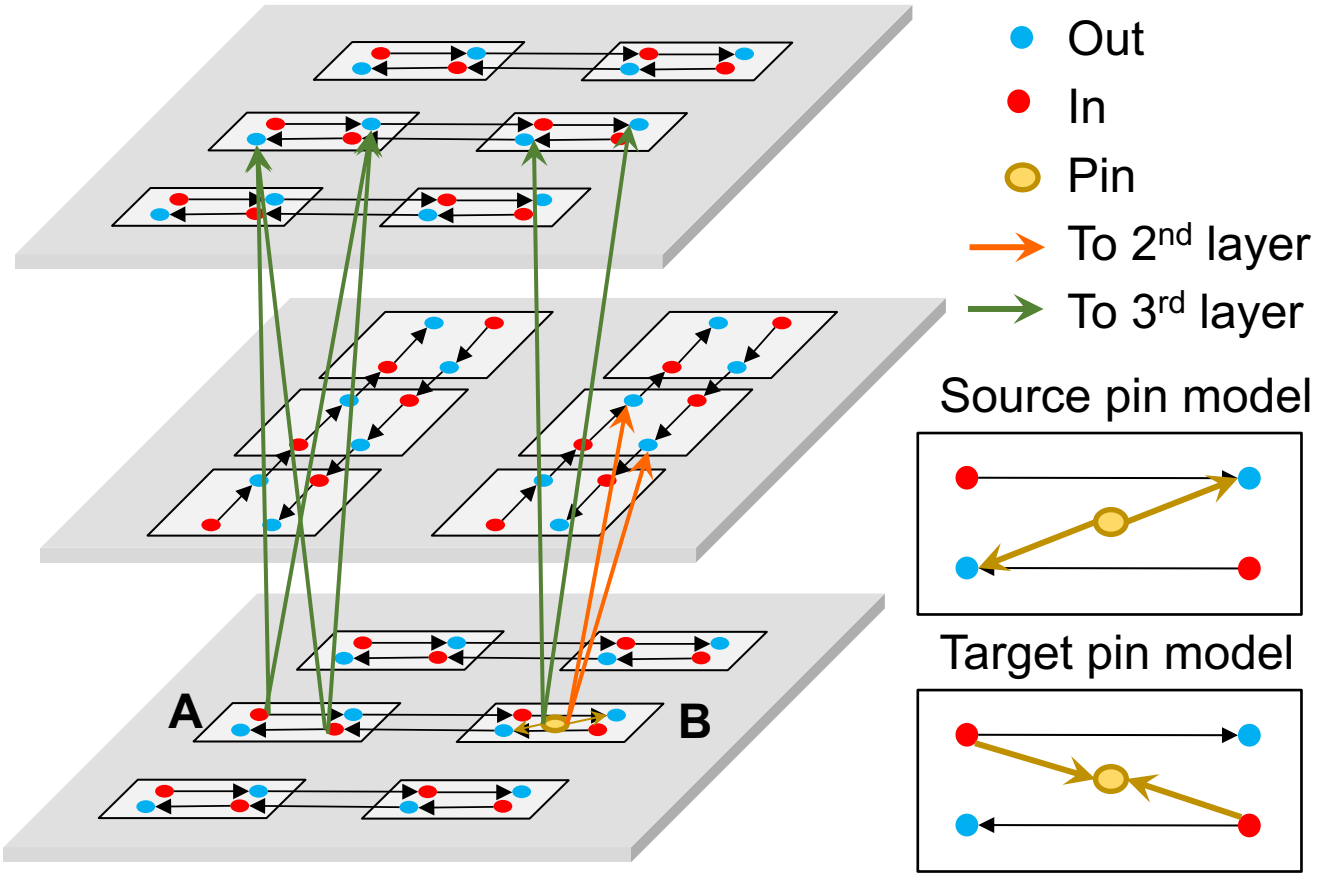
Edge Cost Assignment

- Large costs can be directly assigned on the cross-layer edges to discourage non-preferred connection directions



Extended Graph Model

- Stack vias can be simply modeled
- Source and target pin models are used



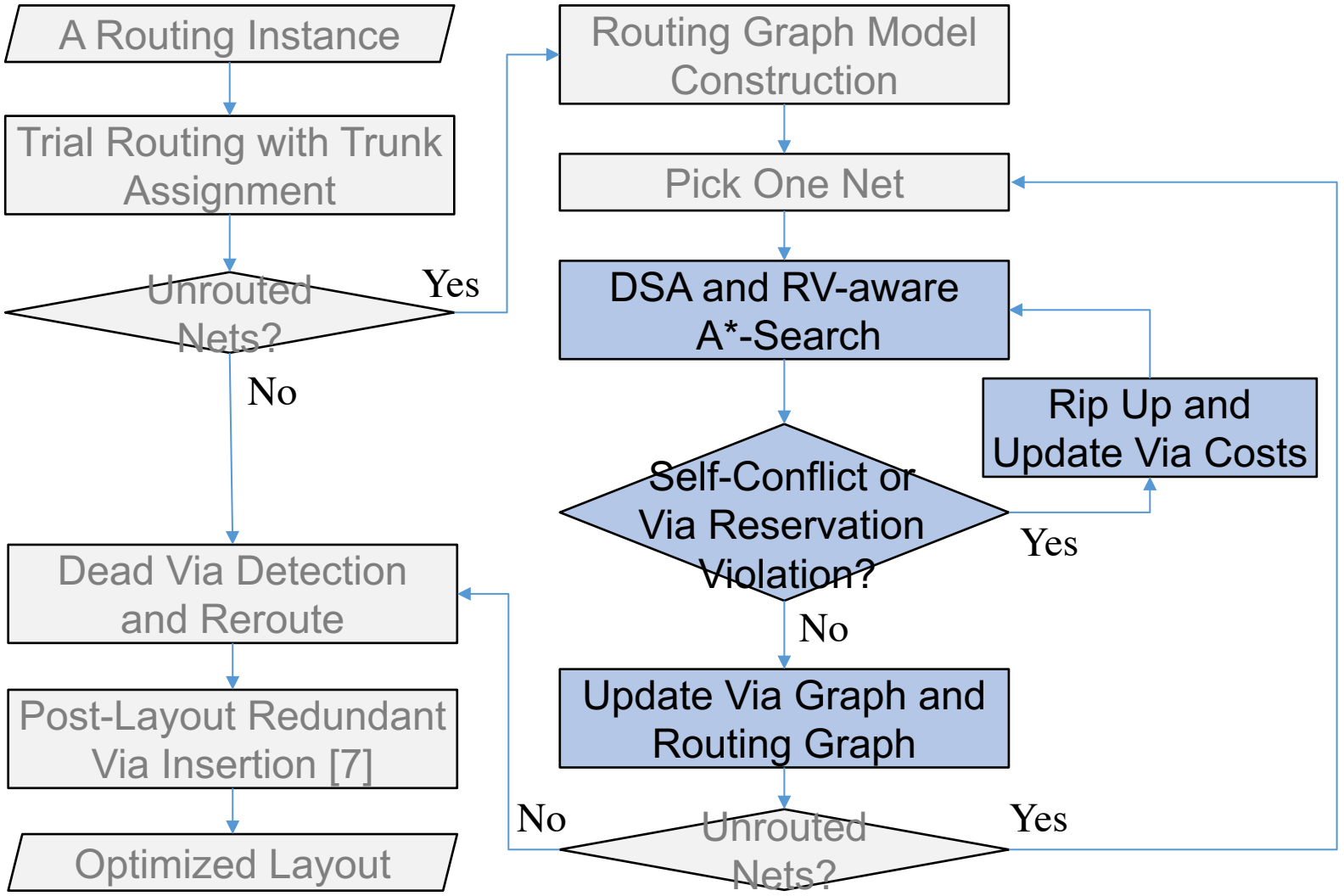
DSA- and RV-aware A*-Search

- The routing cost of a routing path p:

$$cost(p) = \alpha \times WL + \beta \times NCC + \hat{\beta} \times CC + \gamma \times NPC + \delta \times V$$

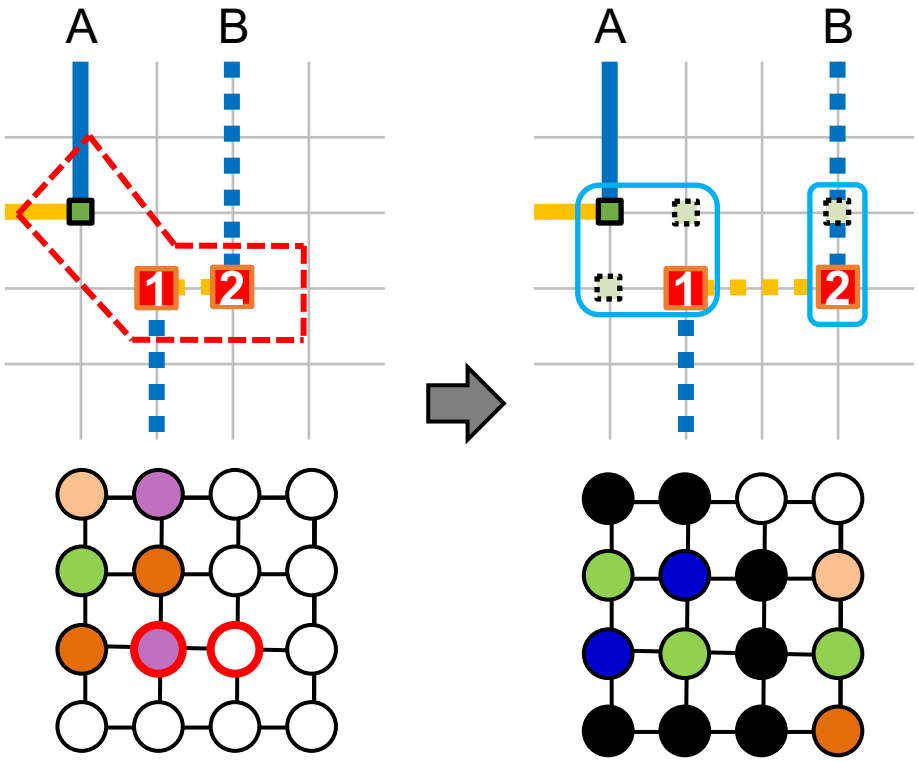
  - WL: wirelength
  - NCC: # non-critical RV candidates eliminated by p
  - CC: # critical RV candidates eliminated by p
  - NPC: # non-preferred connection edges
  - V: # vias
  - $\hat{\beta} \gg \beta$, $\gamma \gg \delta$, to maximize RV insertion rates

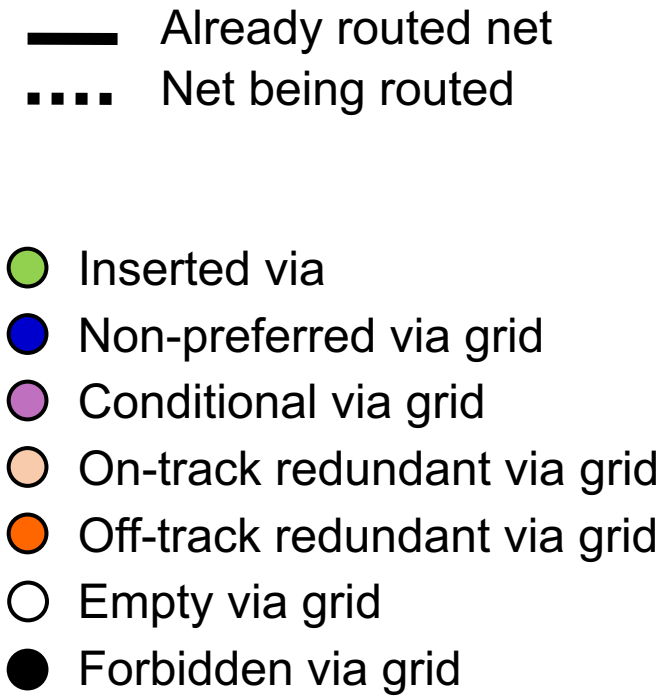
Overall Flow



Self-Conflict Removal

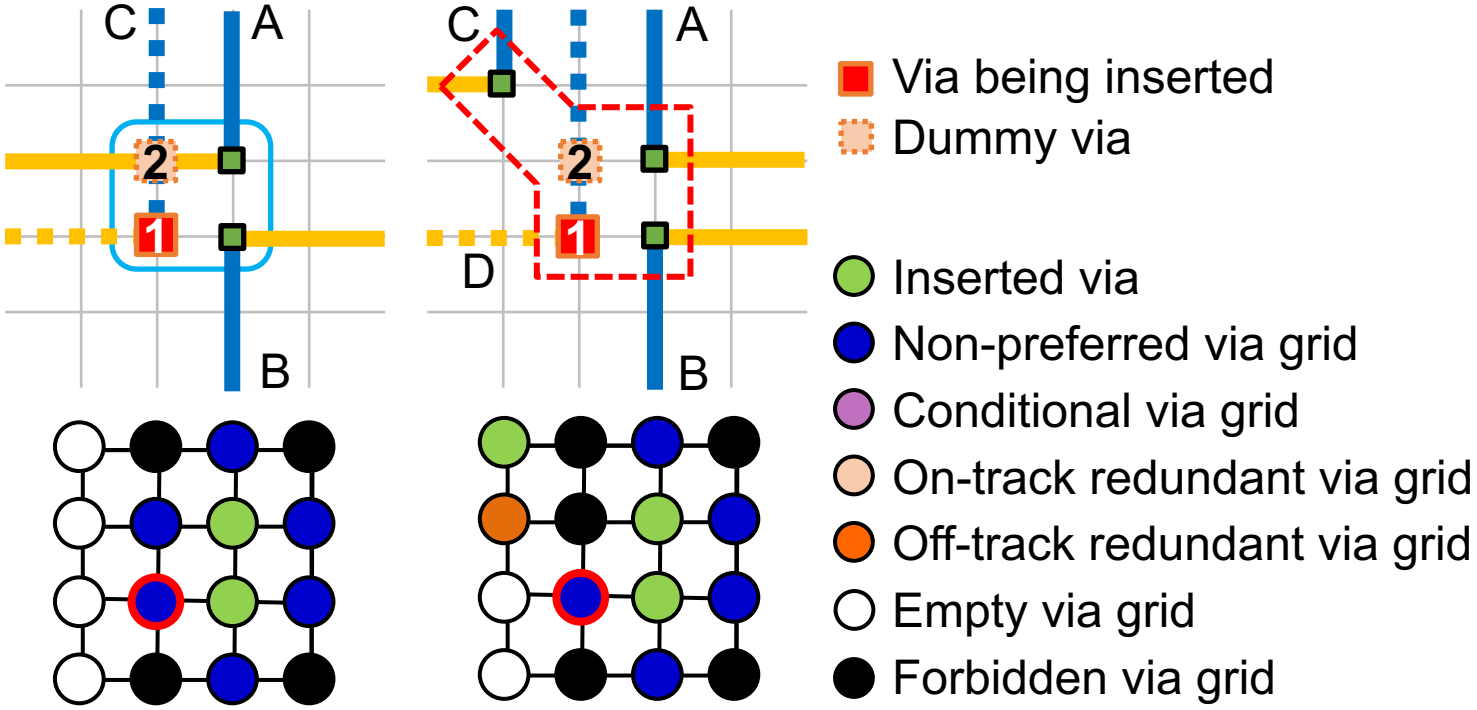
- Infeasible via patterns caused by multiple vias of a net being routed may not be detected
- Increase via costs at specific grids and reroute





Via Reservation Violation

- A dummy via is required to make an infeasible L-shaped 3-via pattern become a feasible squared 4-via pattern
- Short circuits or infeasible via patterns could be generated



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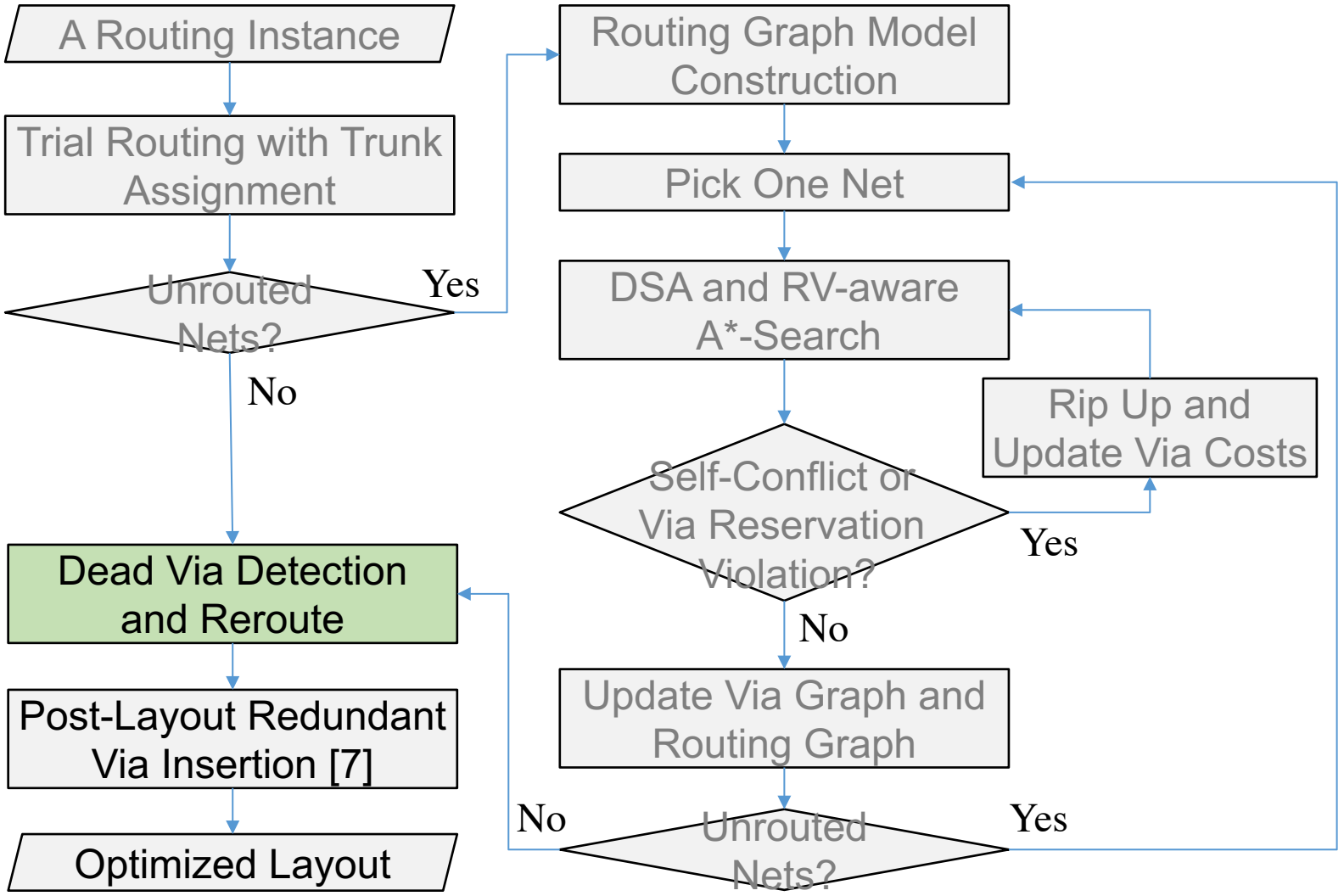

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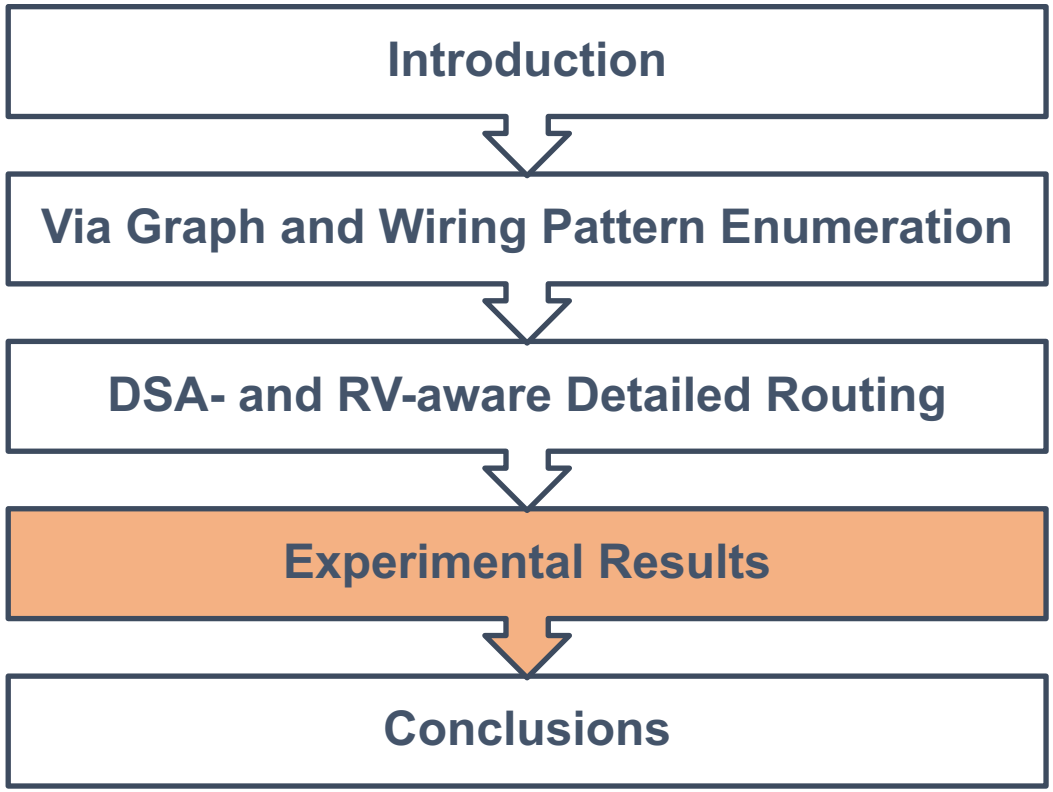
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Experimental Settings

- Platform
  - 2.0 GHz Linux machine with 56 GB memory
  - C++ programming language
- Three routers are implemented based on A*-search
  - Conventional router
  - DSA-aware router [Du et al, SPIE'14]
  - Our DSA- and RV-aware router
- An optimal ILP-based DSA-aware post-routing RV insertion algorithm is implemented [Fang et al, ICCAD'15]

Experimental results

- Compared to the conventional router
  - 47% RV insertion rate improvement
  - The convention router generates many unmanfuacturable vias

Circuit	Conventional A*-Search					Ours				
	WL	# V	RV	# UV	CPU	WL	# V	RV	# UV	CPU
Test0.5k	103	1036	46%	87	<1	108	1040	96%	0	<1
Test1k	219	2092	51%	280	<1	229	2140	96%	0	<!
Test3k	736	6512	54%	772	7	762	6582	95%	0	18
Test5k	1107	10592	52%	1303	13	1154	10782	95%	0	41
Test7k	1792	15268	54%	1824	22	1856	15520	96%	0	69
Test10k	2412	21538	52%	2383	34	2514	21800	96%	0	105
Comp.	0.96	0.99	0.53	-	0.34	1.00	1.00	1.00	-	1.00

  - WL: wirelength in um
  - # V: # vias
  - RV: RV insertion rate
  - # UN: # unmanufacturable vias
  - CPU: runtime

Experimental results (cont'd)

- Compared to the DSA-aware router
  - 39% RV insertion rate improvement
  - 5% WL overhead and 1% increase in # vias

Circuit	DSA-aware Router [Du et al.]					Ours				
	WL	# V	RV	# UV	CPU	WL	# V	RV	# UV	CPU
Test0.5k	102	1040	51%	0	<1	108	1040	96%	0	<1
Test1k	218	2118	59%	0	<1	229	2140	96%	0	<1
Test3k	727	6496	61%	0	14	762	6582	95%	0	18
Test5k	1102	10658	60%	0	28	1154	10782	95%	0	41
Test7k	1783	15374	62%	0	46	1856	15520	96%	0	69
Test10k	2396	21646	59%	0	72	2514	21800	96%	0	105
Comp.	0.95	0.99	0.61	-	0.70	1.00	1.00	1.00	-	1.00

  - WL: wirelength in um
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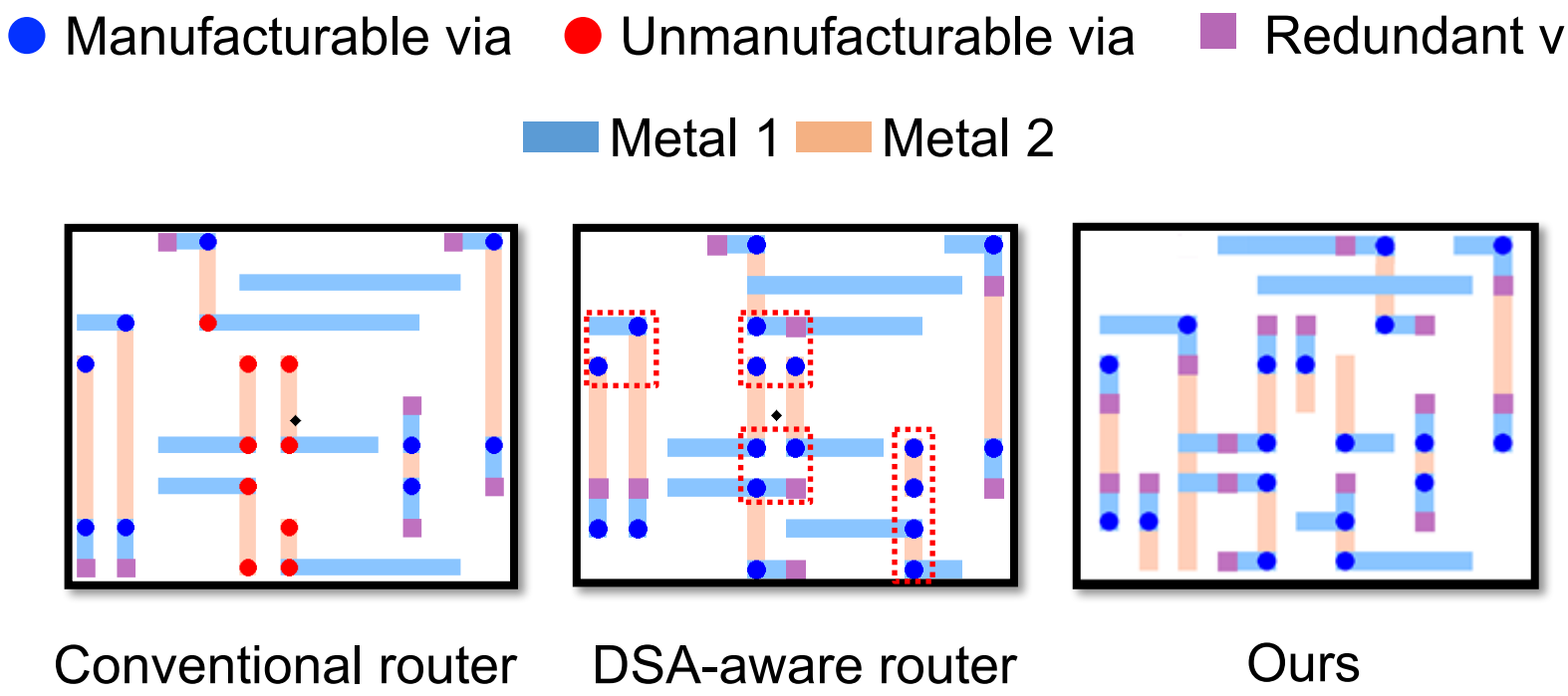
Example Layout



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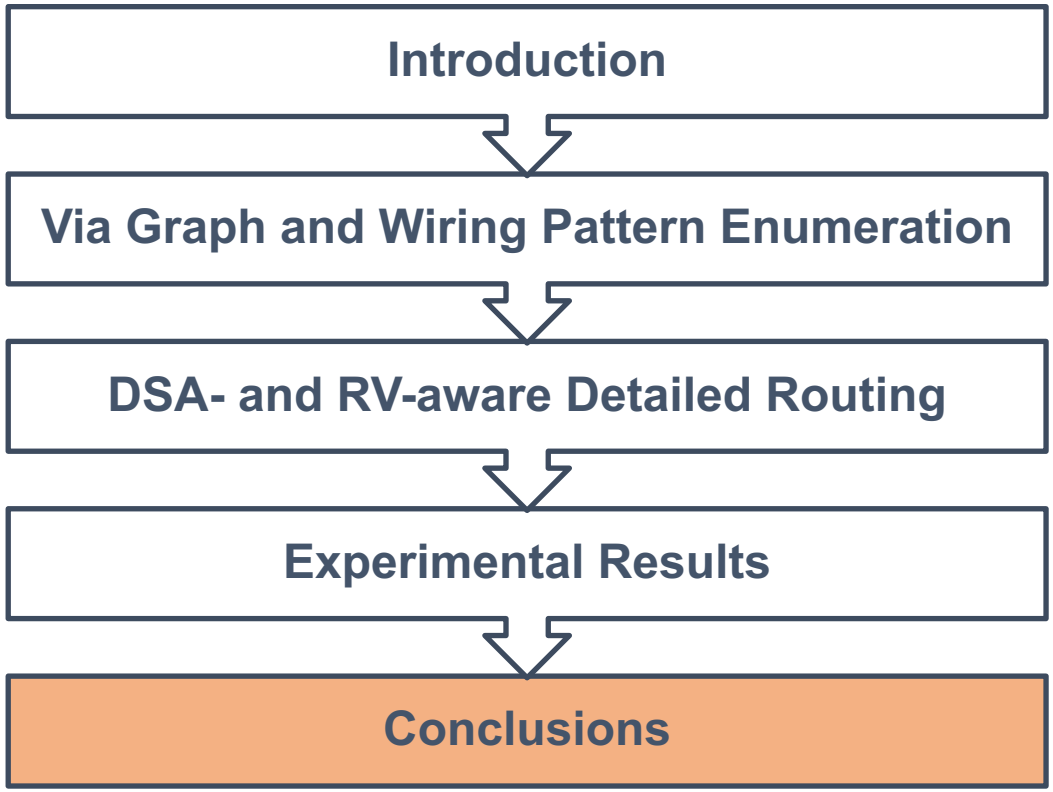
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Conclusions

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- A sophisticated routing graph model is proposed that is able to distinguish different wire connection directions
- Trunk assignment and rip-up/rerouting techniques are proposed for better via planning
- Experimental results validate the effectiveness of the proposed algorithms


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