Planning Flexible Interconnect in 2.5D ICs to Minimize the Interposer's Metal Layers

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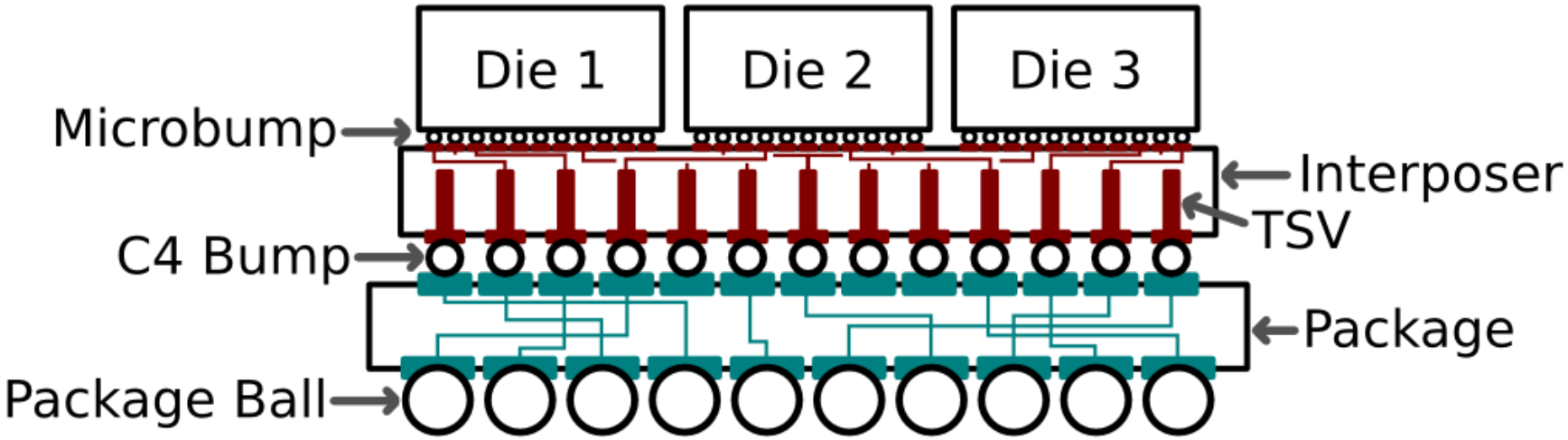
Background: 2.5D Integrated Circuits

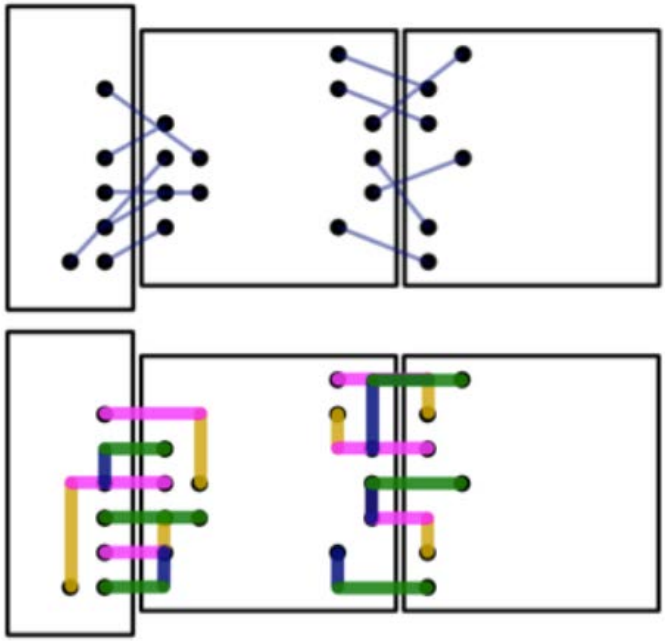


- Provides potential to assemble dies from multiple vendors together on a single 2.5D IC

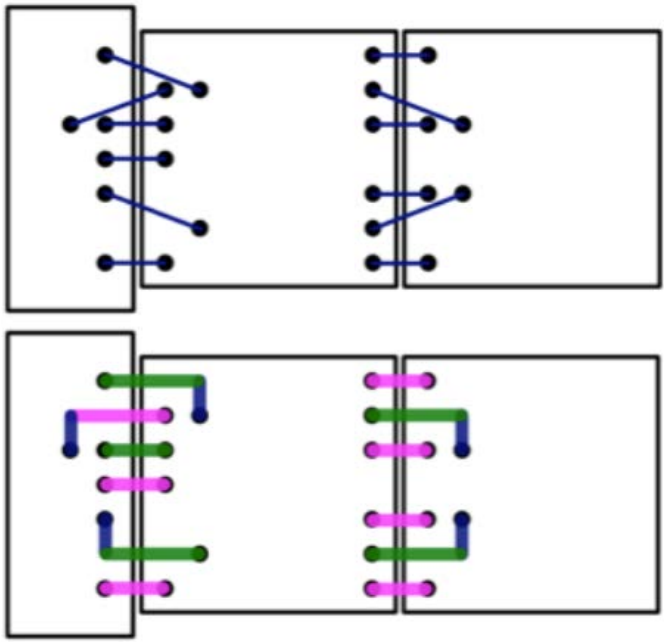
Key Focus: Flexible Interconnect

- Many designs have freedom in pin assignment
  - FPGAs, Microprocessor GPIOs, etc.
- Exploit flexibility without limiting design decisions by specifying *eligible pins* for needed connections
  - Pin function
  - Bank
  - Set of pins

Pin Assignment Affects Layer Count

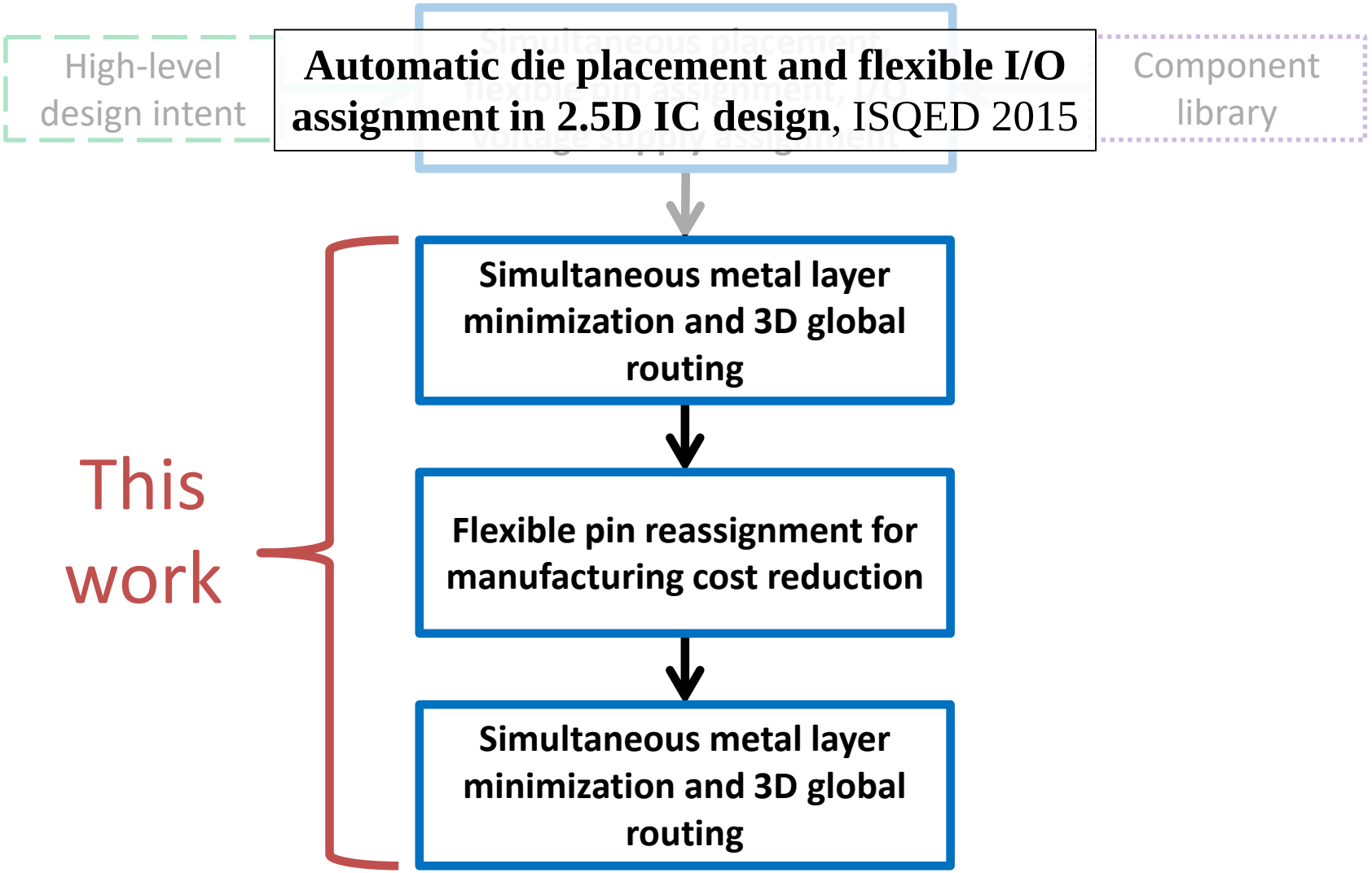


4 routing layers



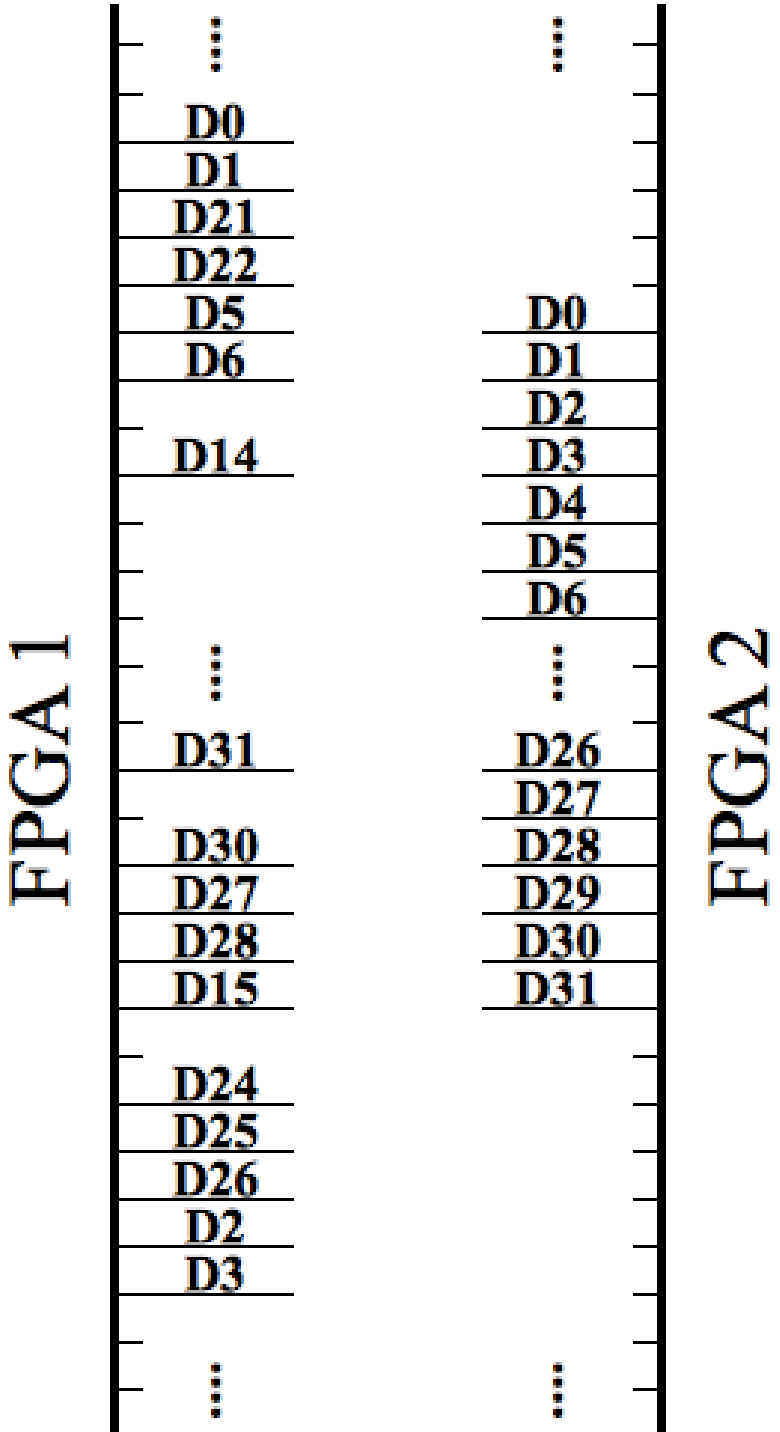
3 routing layers

Framework Overview



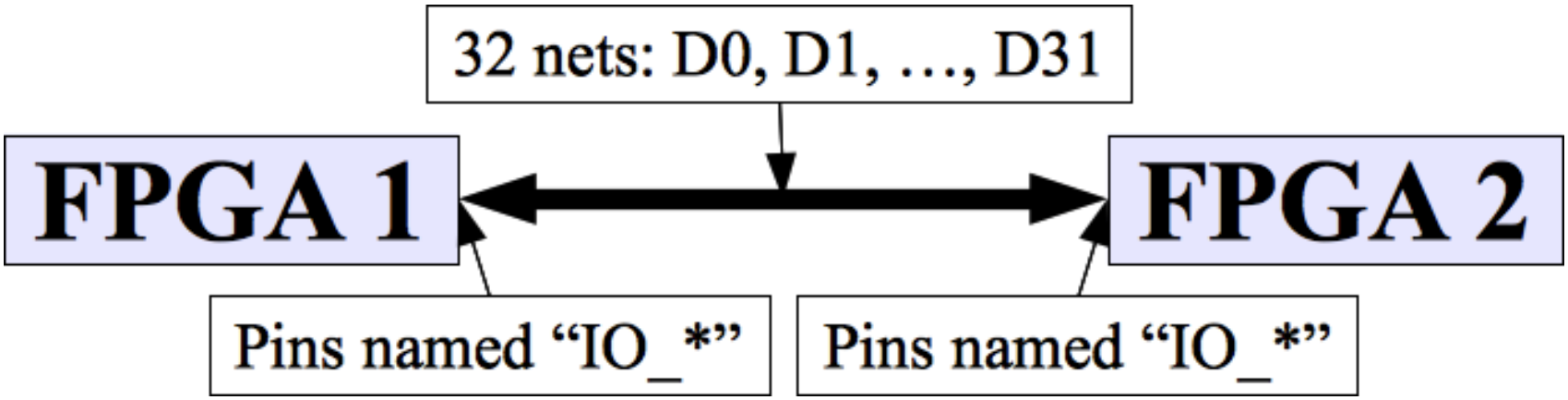
Schematic Capture

- Explicitly connect pins
- Graphical or tabular
- Tedious
- Error-prone

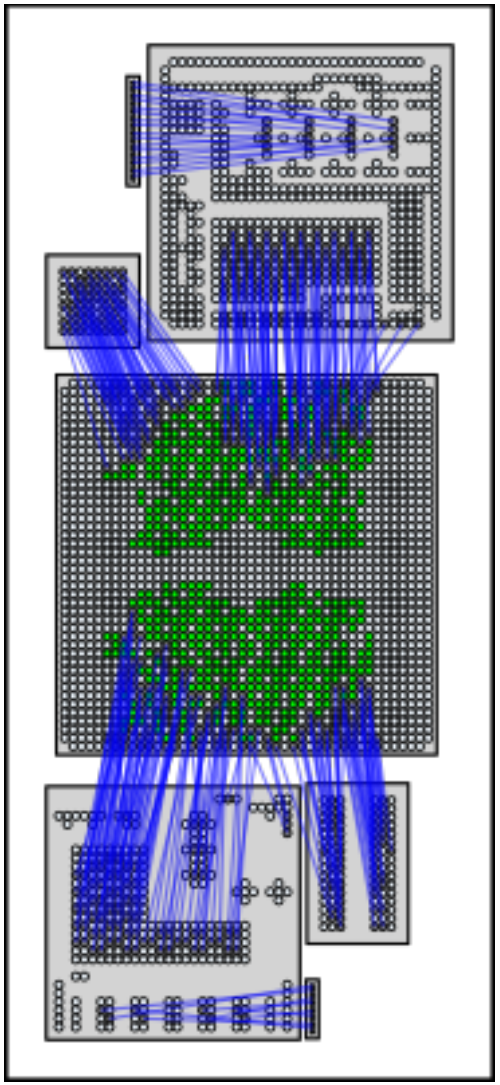


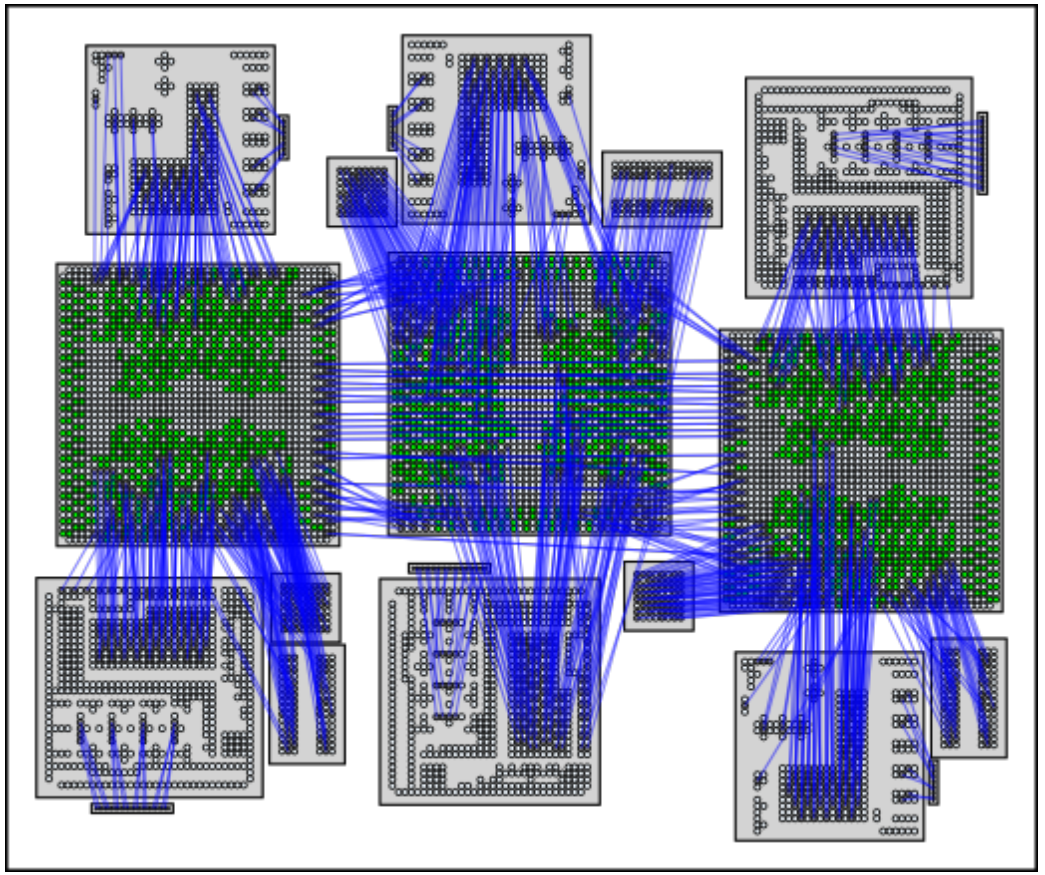
High-Level Design Capture

- Specify requirements with fewer details necessary
  - Flexible and powerful



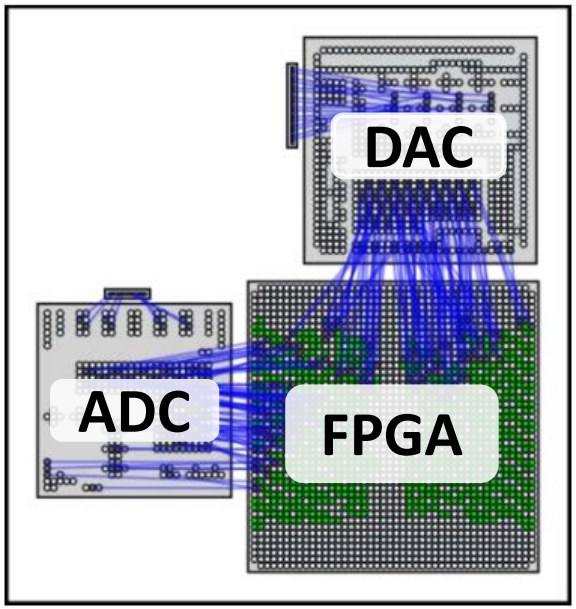
Placement and Pin Assignment

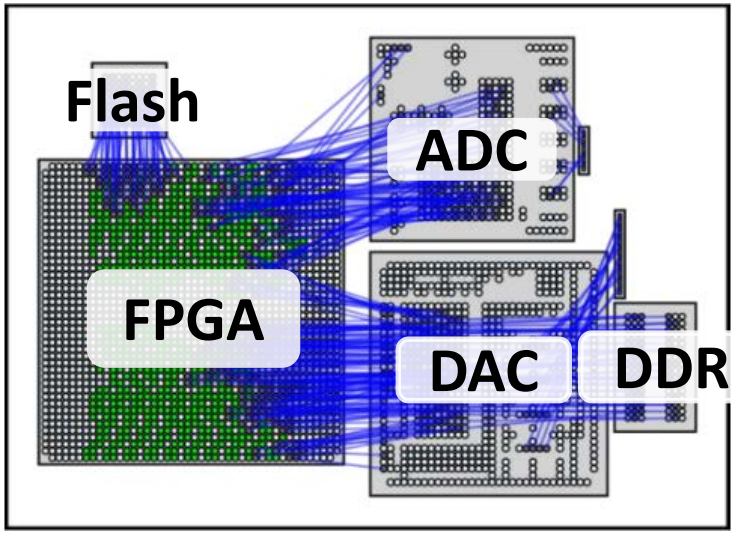


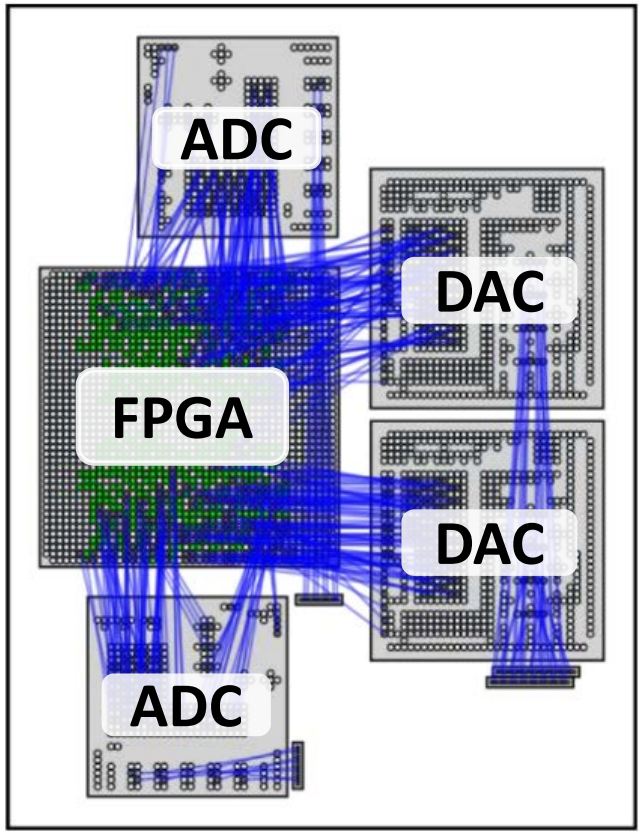


D. P. Seemuth, A. Davoodi, and K. Morrow, Automatic die placement and flexible I/O assignment in 2.5D IC design, 16th International Symposium on Quality Electronic Design (ISQED), pp. 524-527, 2015.

Example Input Layouts







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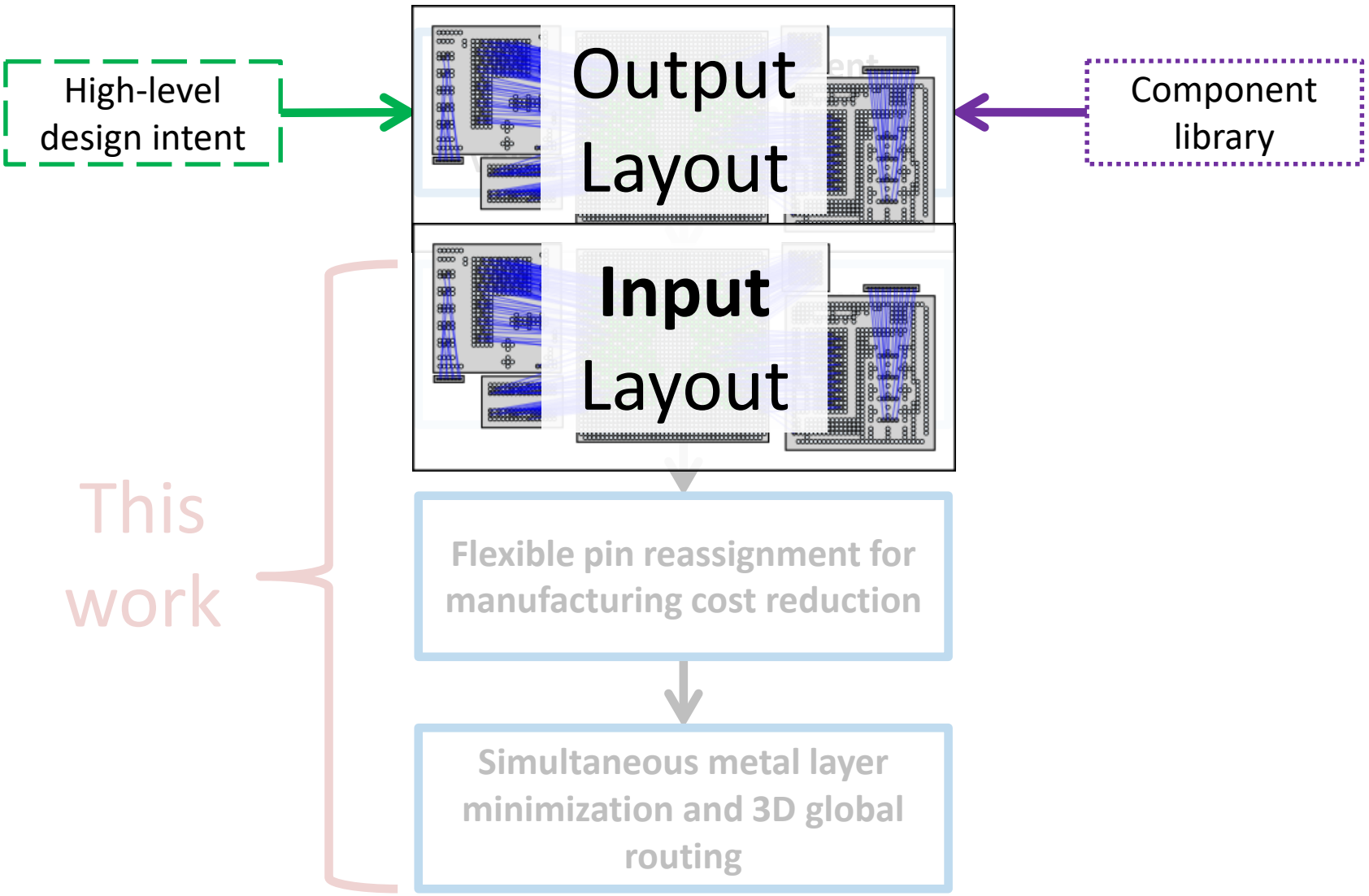
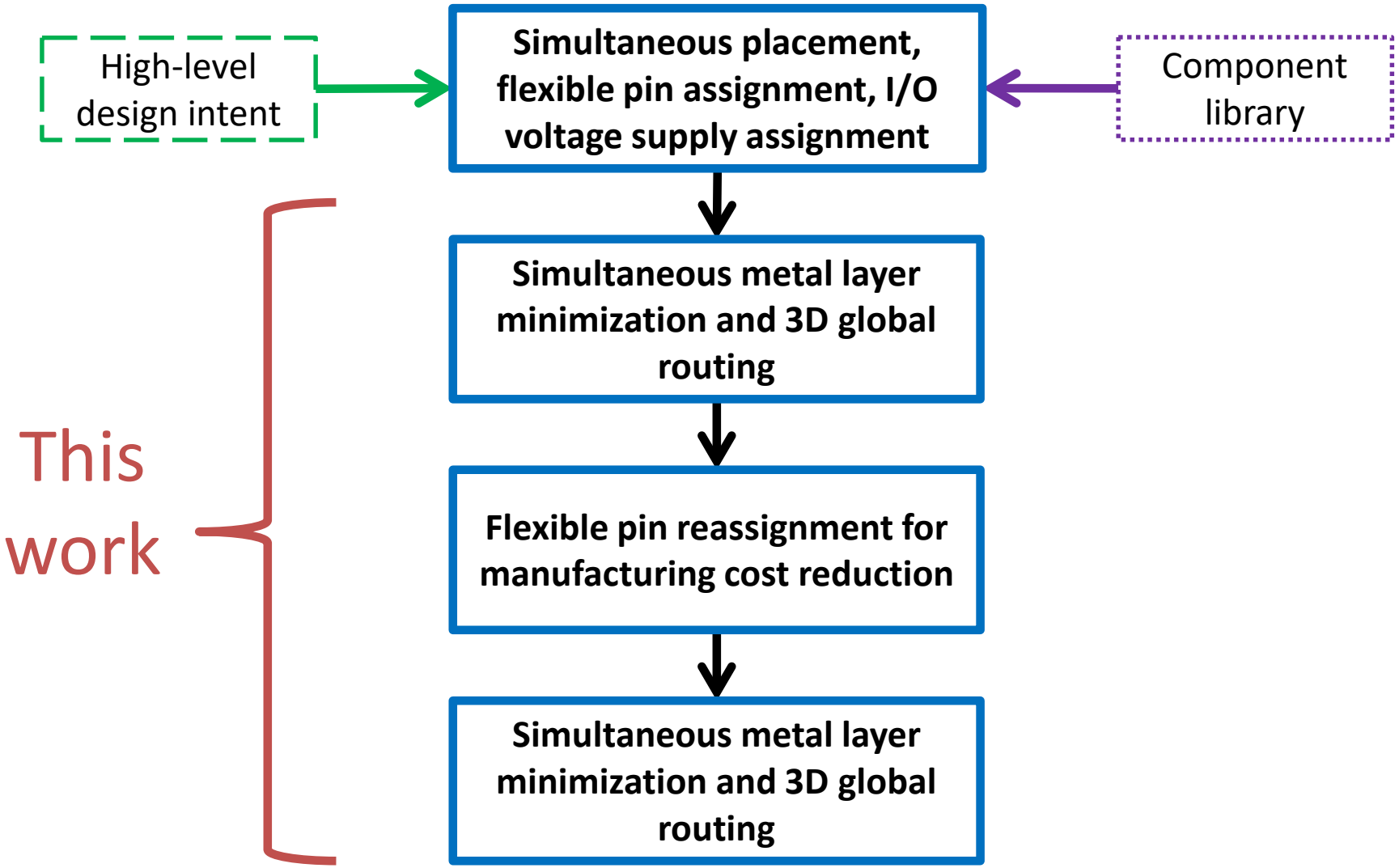
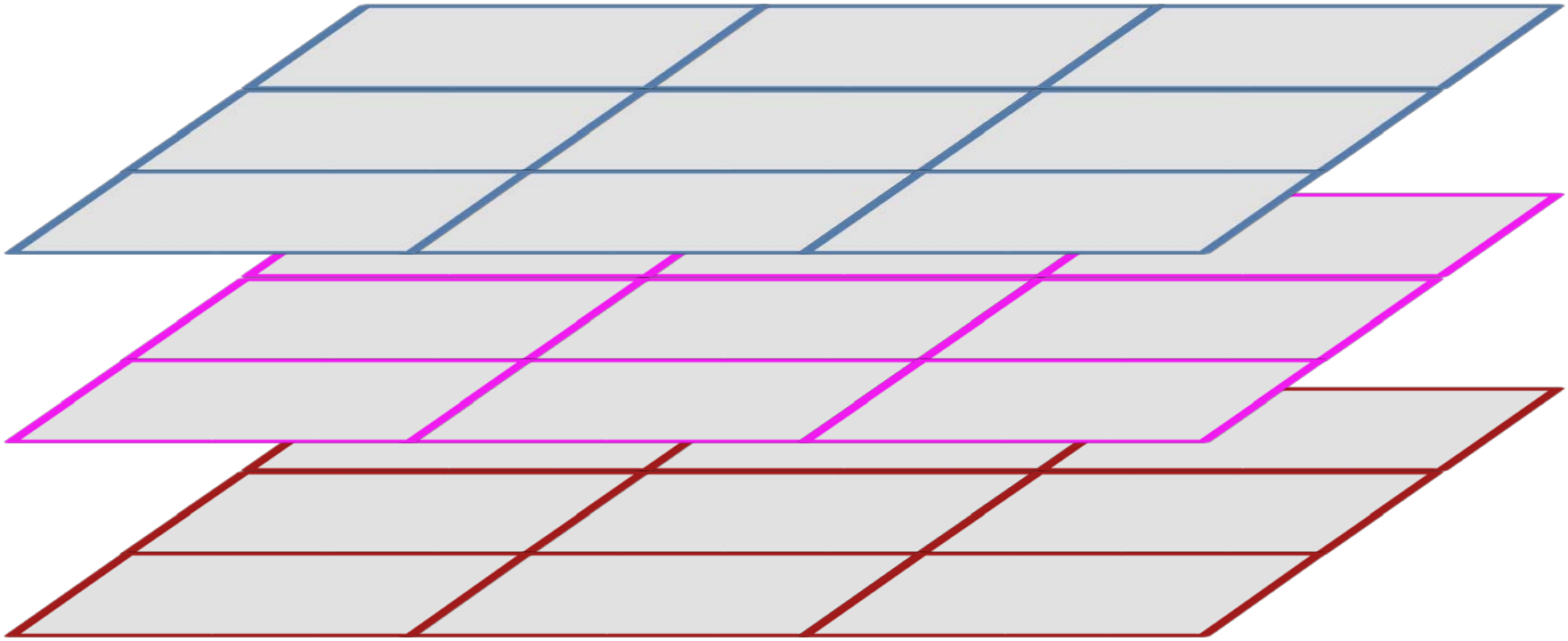


Framework Overview



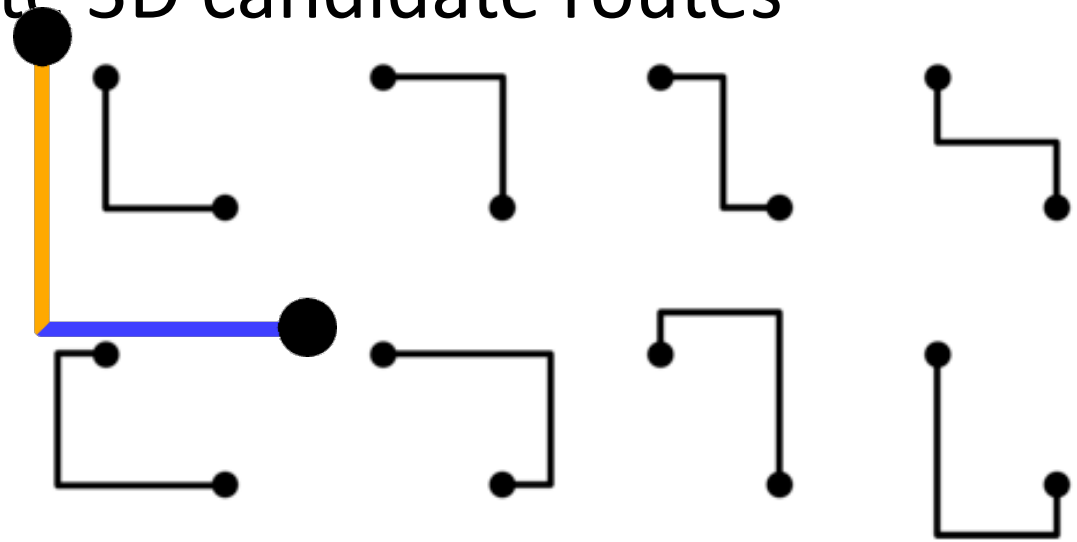
Metal Layer Minimization and 3D GR

Divide interposer into uniform grid of “bins”



MLM3DGR Candidate Routes

Generate 3D candidate routes

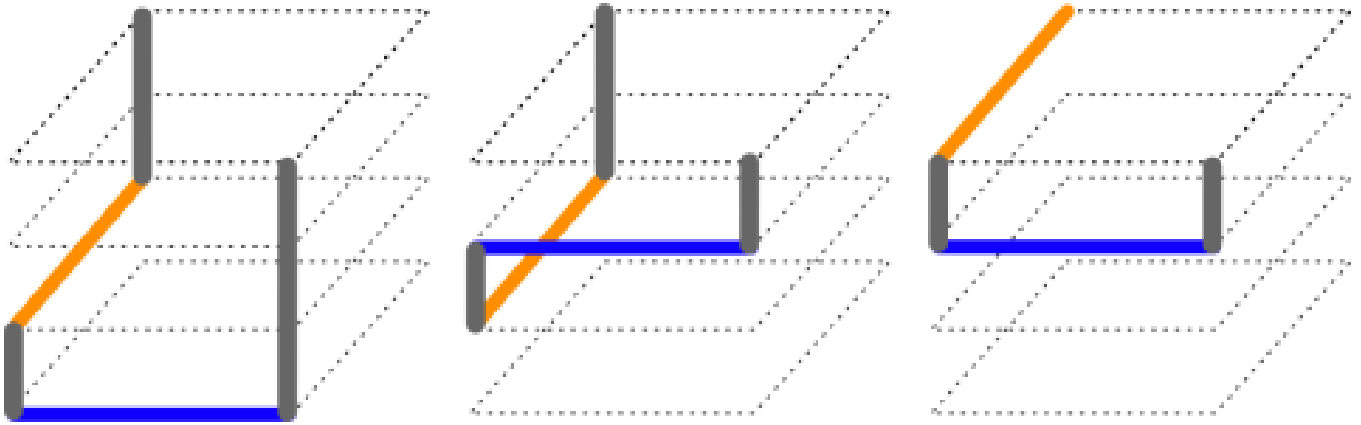


MLM3DGR ILP Variables

Generate ILP variables

$$x_{it} = \begin{cases} 1, & net\ i\ is\ assigned\ route\ t; \\ 0, & otherwise \end{cases}$$

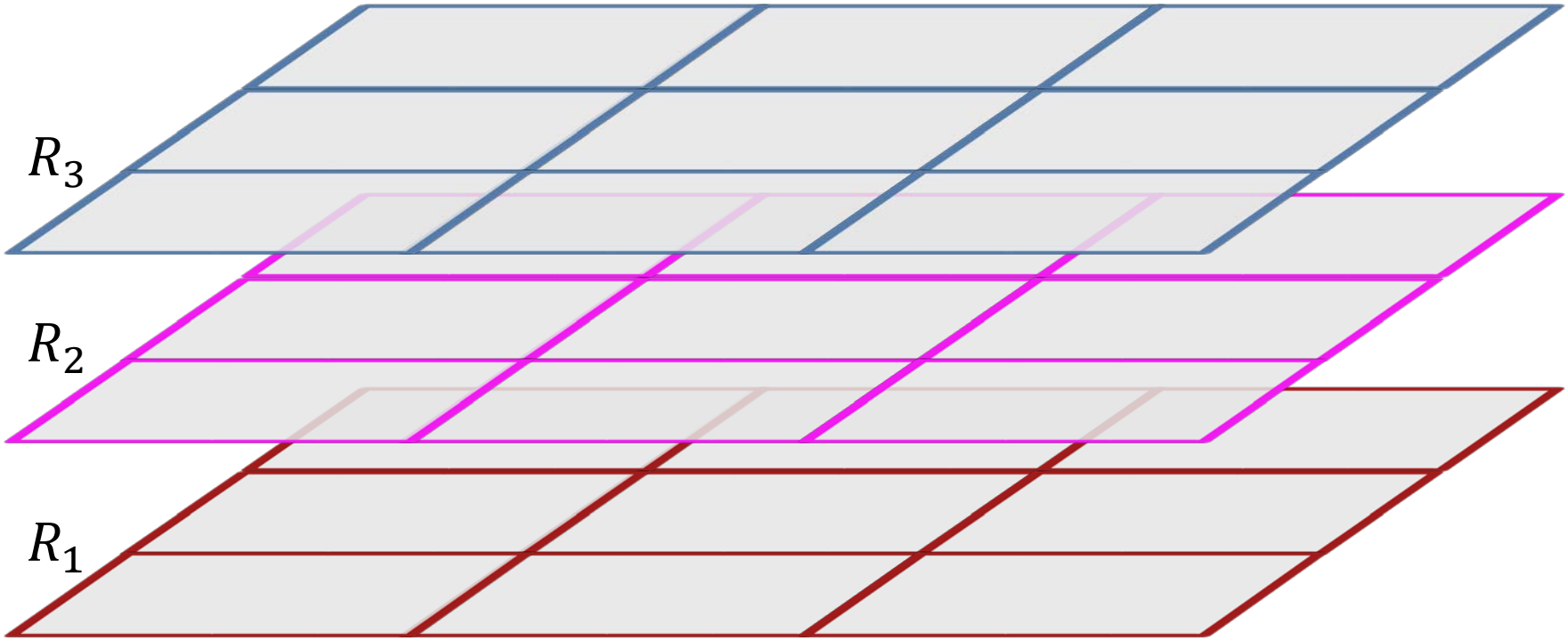
For net #1:



x_{11} x_{12} x_{13} ...

MLM3DGR ILP Variables, cont'd

$$R_l = \begin{cases} 1, & layer\ l\ is\ assigned\ to\ be\ used\ for\ routing; \\ 0, & otherwise \end{cases}$$



MLM3DGR ILP Formulation

$$\min \sum_{l=1}^{R} k^{l-1} \times R_l$$

Minimize # layers

$$\sum_{i \in N} \sum_{t \ni e} x_{it} \leq C_e \quad \forall e \in E$$

Heed grid edge capacities

$$\sum_{t \in T_i} x_{it} = 1 \quad \forall i \in N$$

Every net needs a route

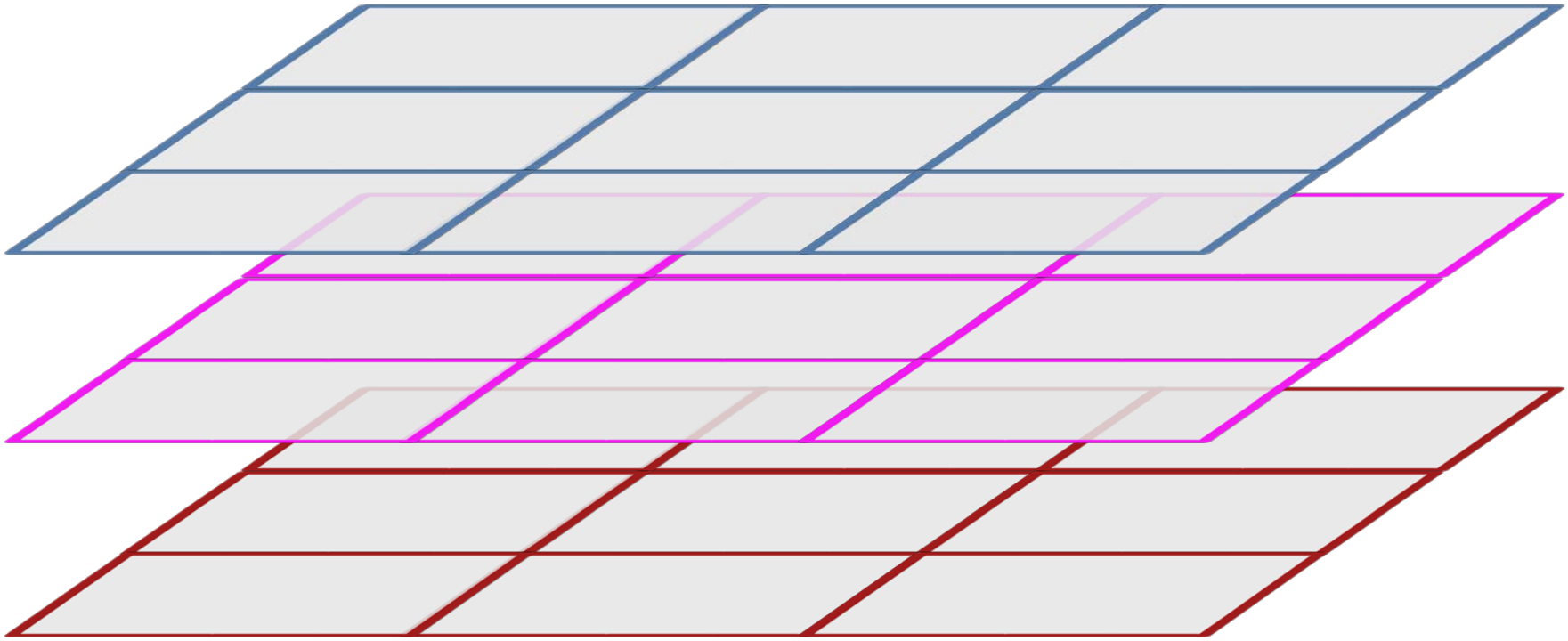
$$x_{it} \leq R_l \quad \forall l \in \{1, \ldots, R\} \quad \forall i \in N$$

$$| \; if \; t \ni e \; and \; e \; on \; layer \; l$$

Route on a layer only if that layer may be used

Metal Layer Minimization and 3D GR

Divide interposer into uniform grid of “bins”



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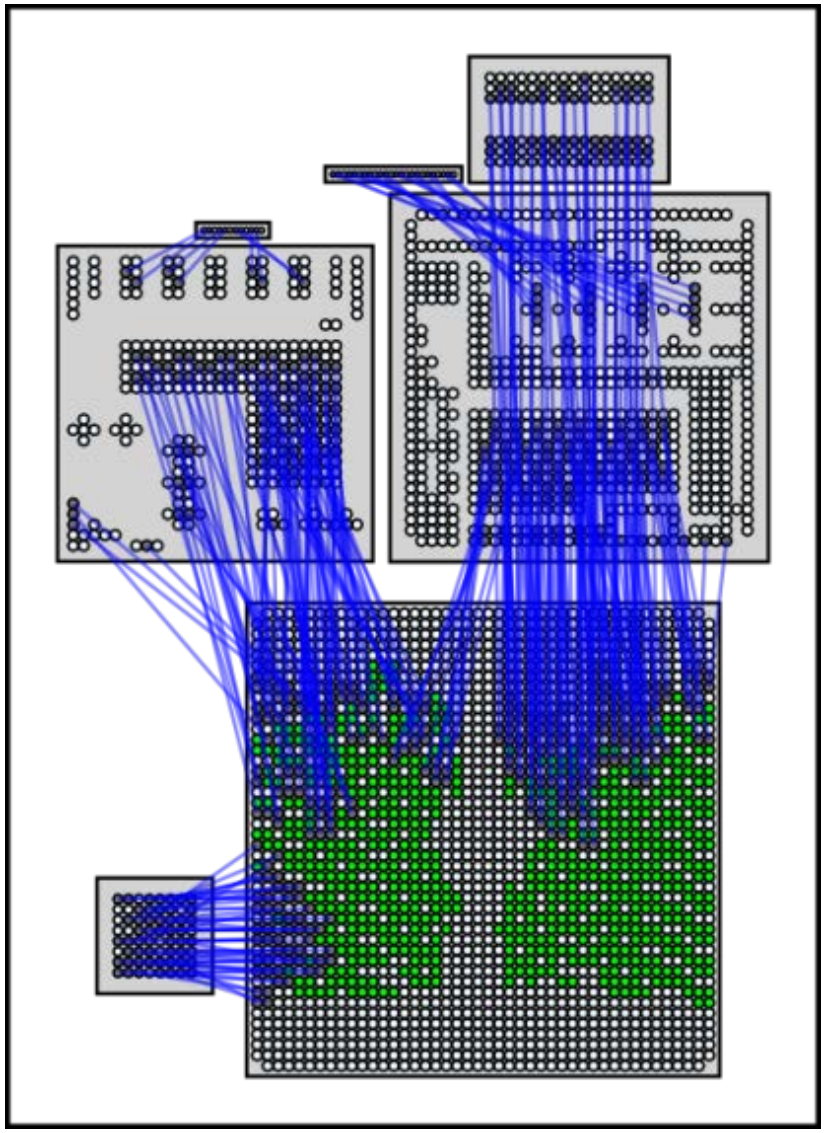
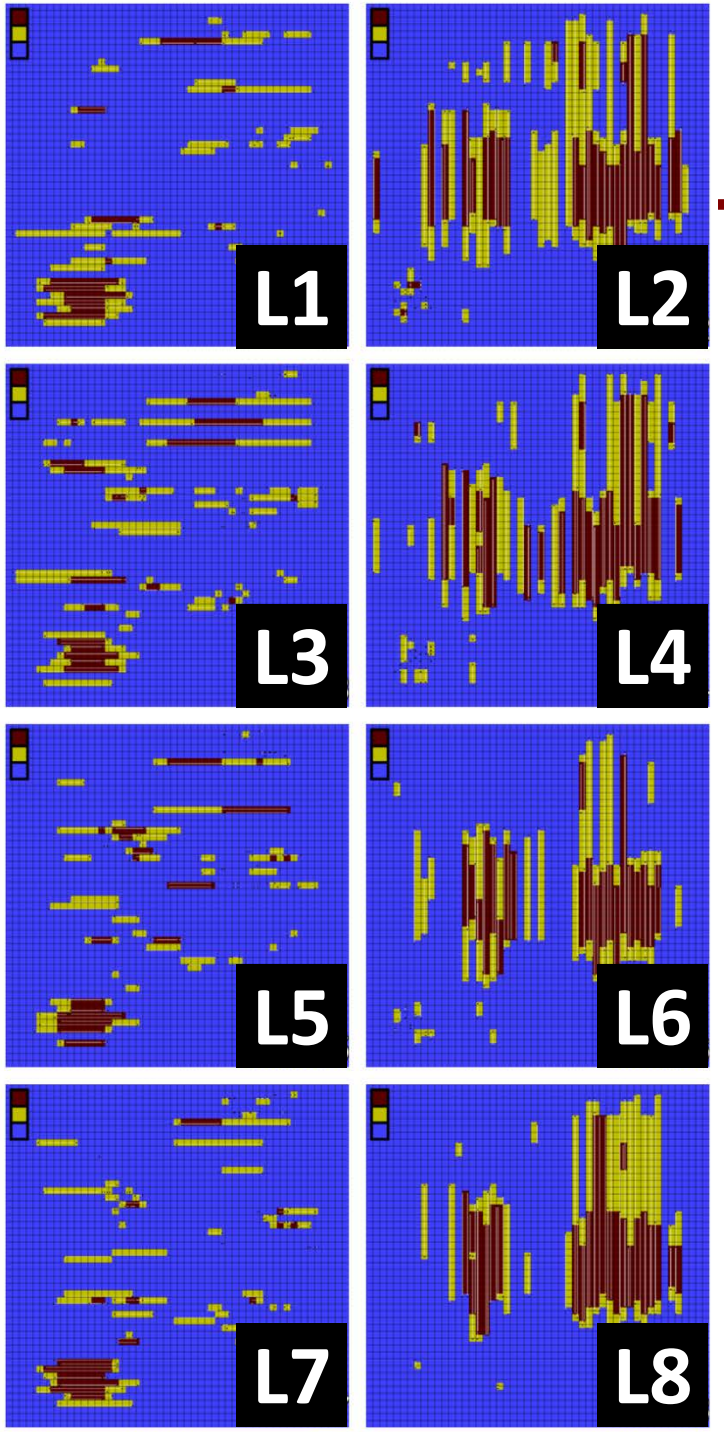
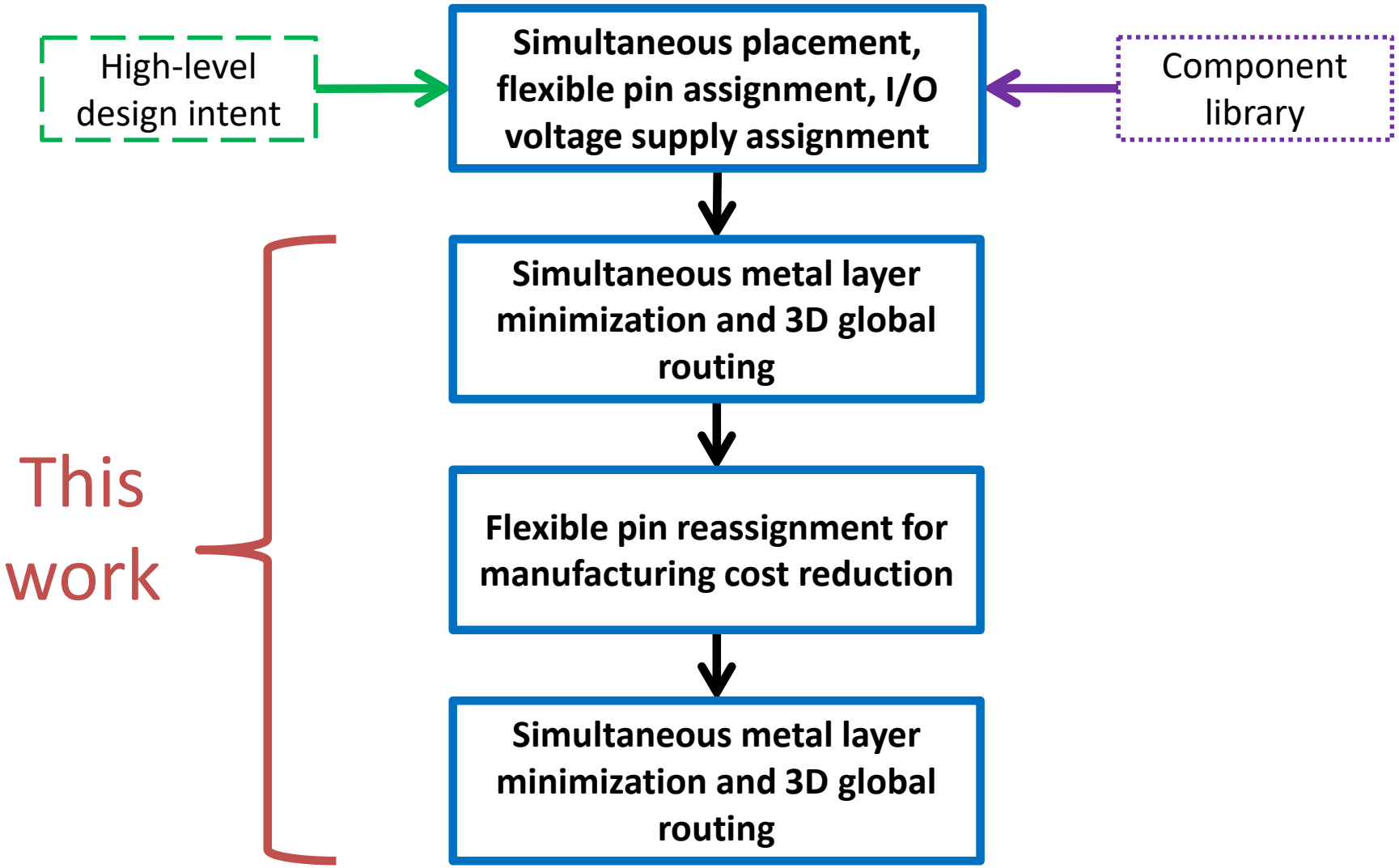
MLM3DGR Results





Framework Overview



Flexible Pin Reassignment

- Refine pin assignment based on results from metal layer minimization and 3D global routing
- Explore flexible pin solution space

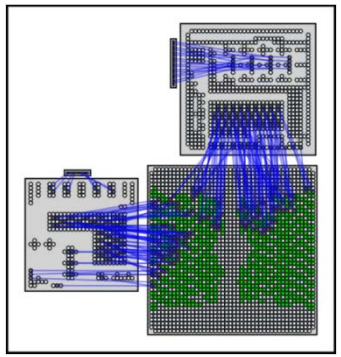
- Create 2D grid of bins based on 3D results
- Repeatedly reassign each pin until no more improvement
  - Choose pin and route that minimizes cost
    - Total overflow
    - Random ordering for breaking ties

Flexible Pin Reassignment

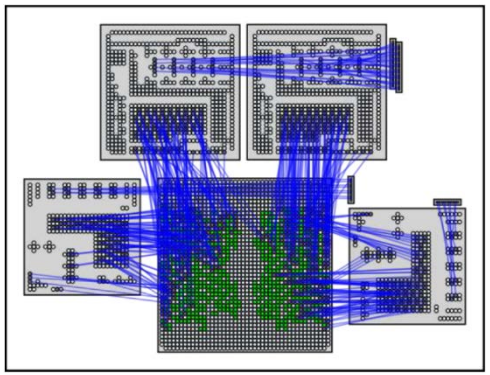
do:
improved := false
Randomly shuffle N^F
For each net $i \in N^F$:
Choose flexible pin p **and candidate route** $t_i \in T_i^p$ such that:
Pin p is not assigned to any net, or is already assigned to the current net i
Pin p is within a bank that is compatible with net i
Route $t_i \in T_i^p$ **minimizes total overflow** in the 2D grid
If new p, t_i were chosen:
improved := true
Update the 2D grid utilization according to choosing p, t_i
while improved is true

Pin Reassignment Experiments

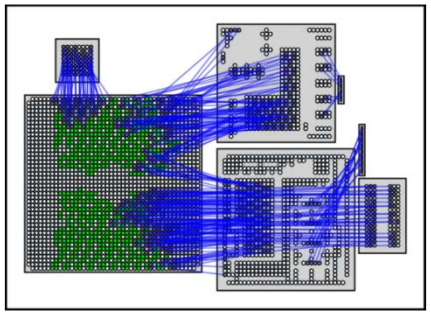
A



B

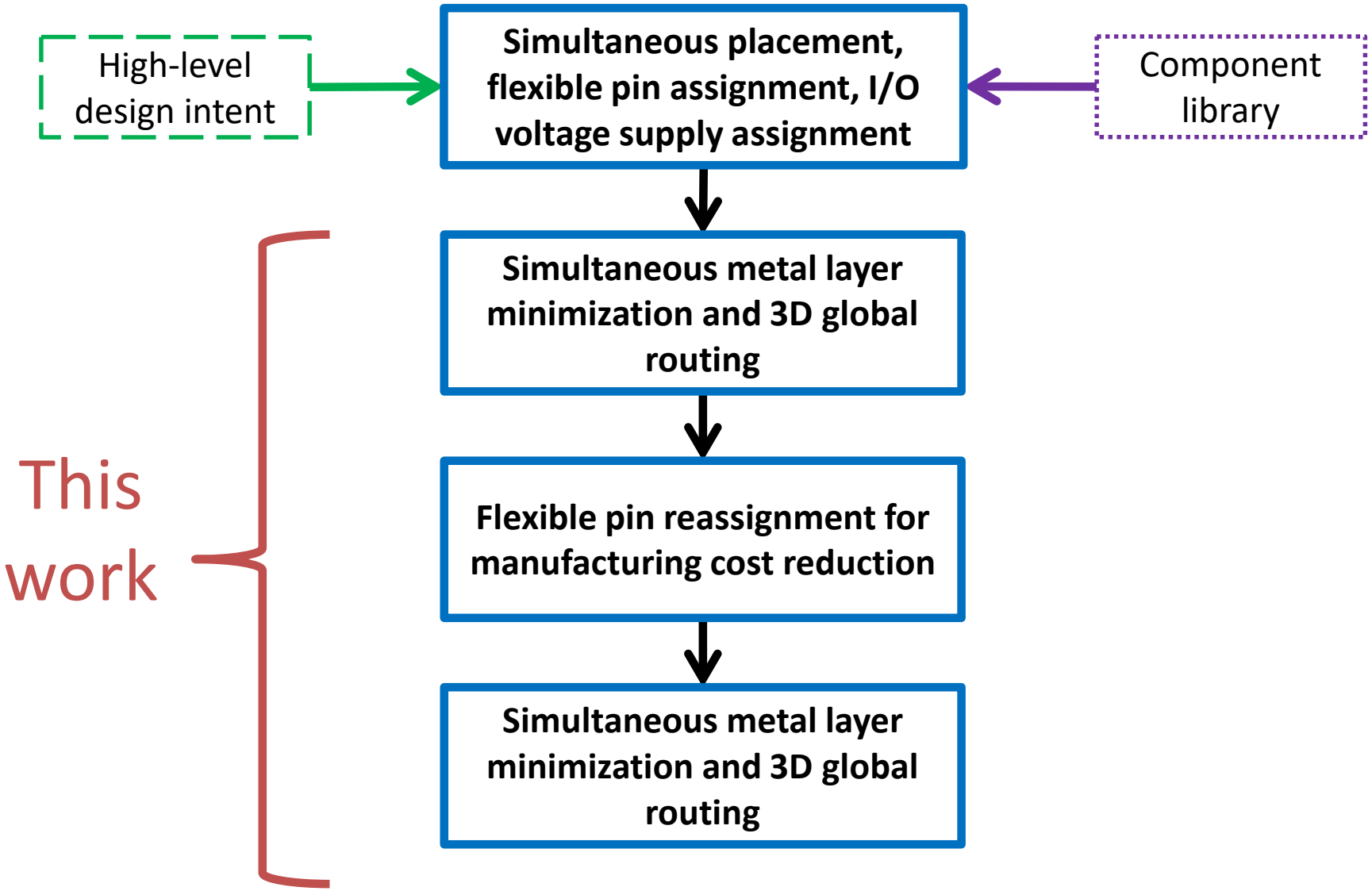


C



	Single / Differential	# Pins	Reassignment Runtime (s)
A	11 / 85	948	108
B	22 / 170	1056	129
C	99 / 88	1039	312

Framework Overview

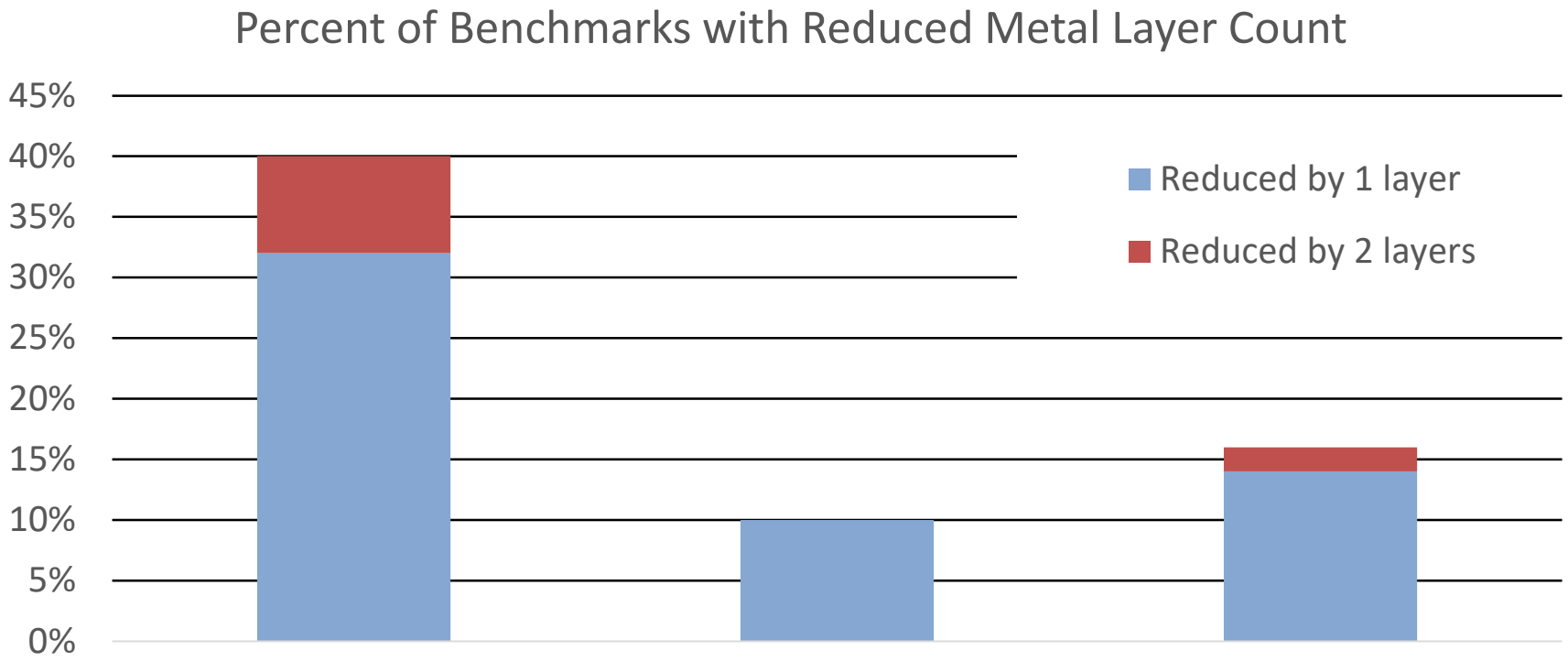


Repeat MLM3DGR

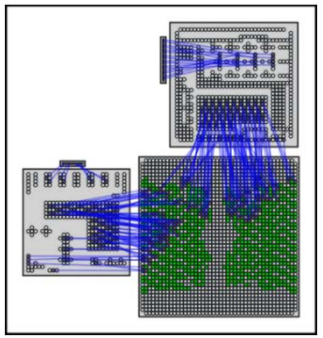
- Perform metal layer minimization and 3D global routing
- Same placement
- New pin assignments

- Keep new pin assignments if fewer metal layers

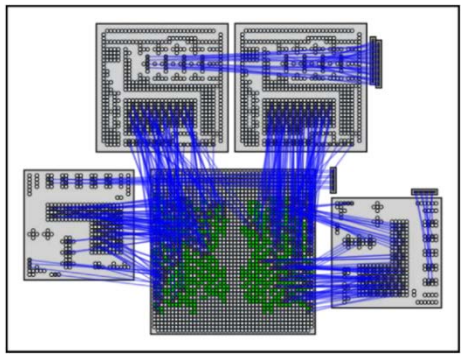
Pin Reassignment Layer Results



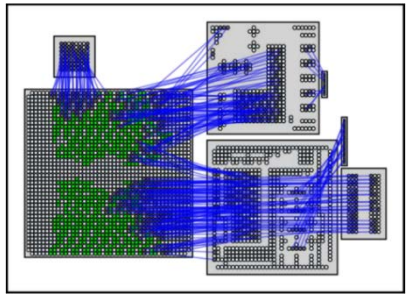
A



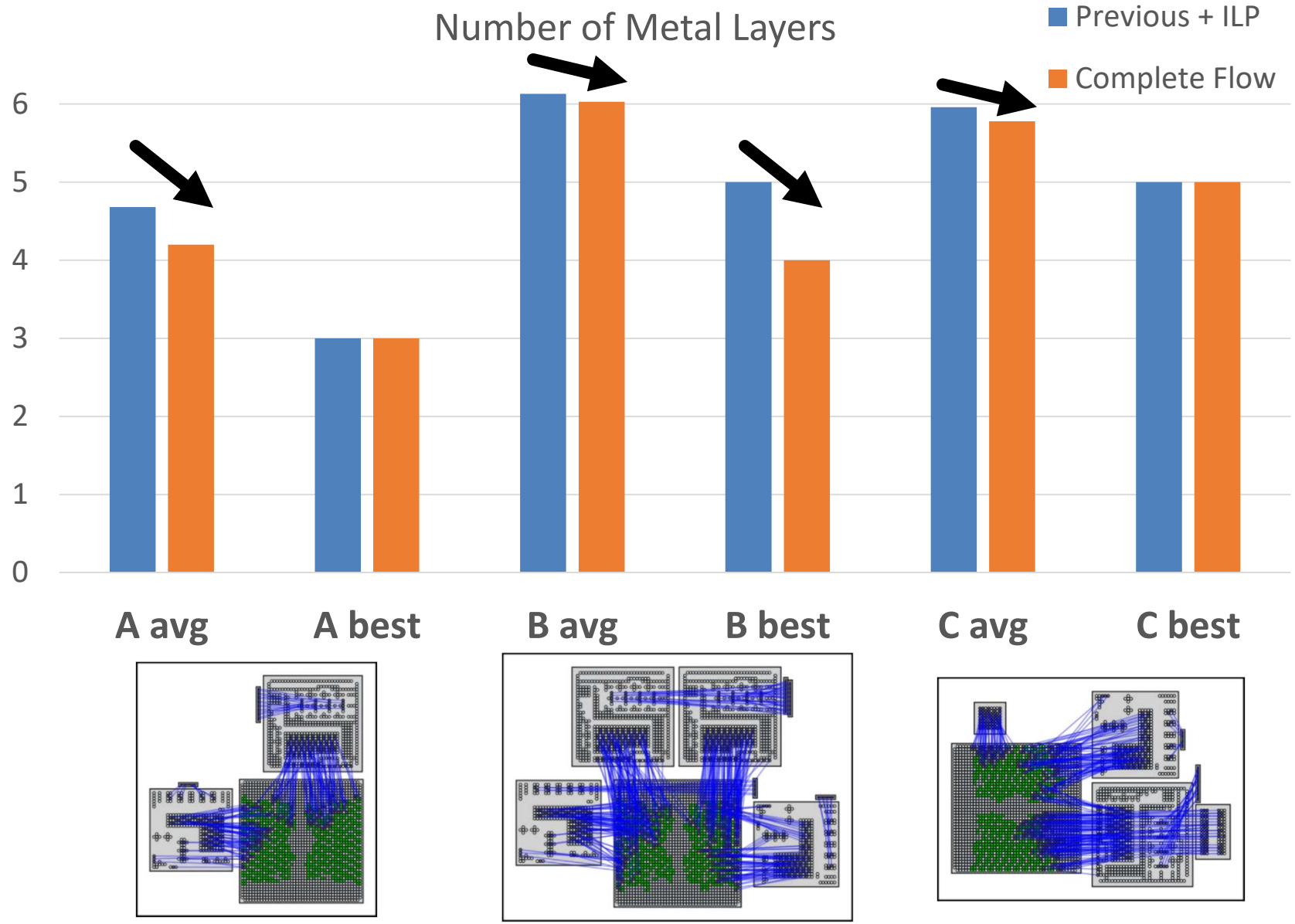
B



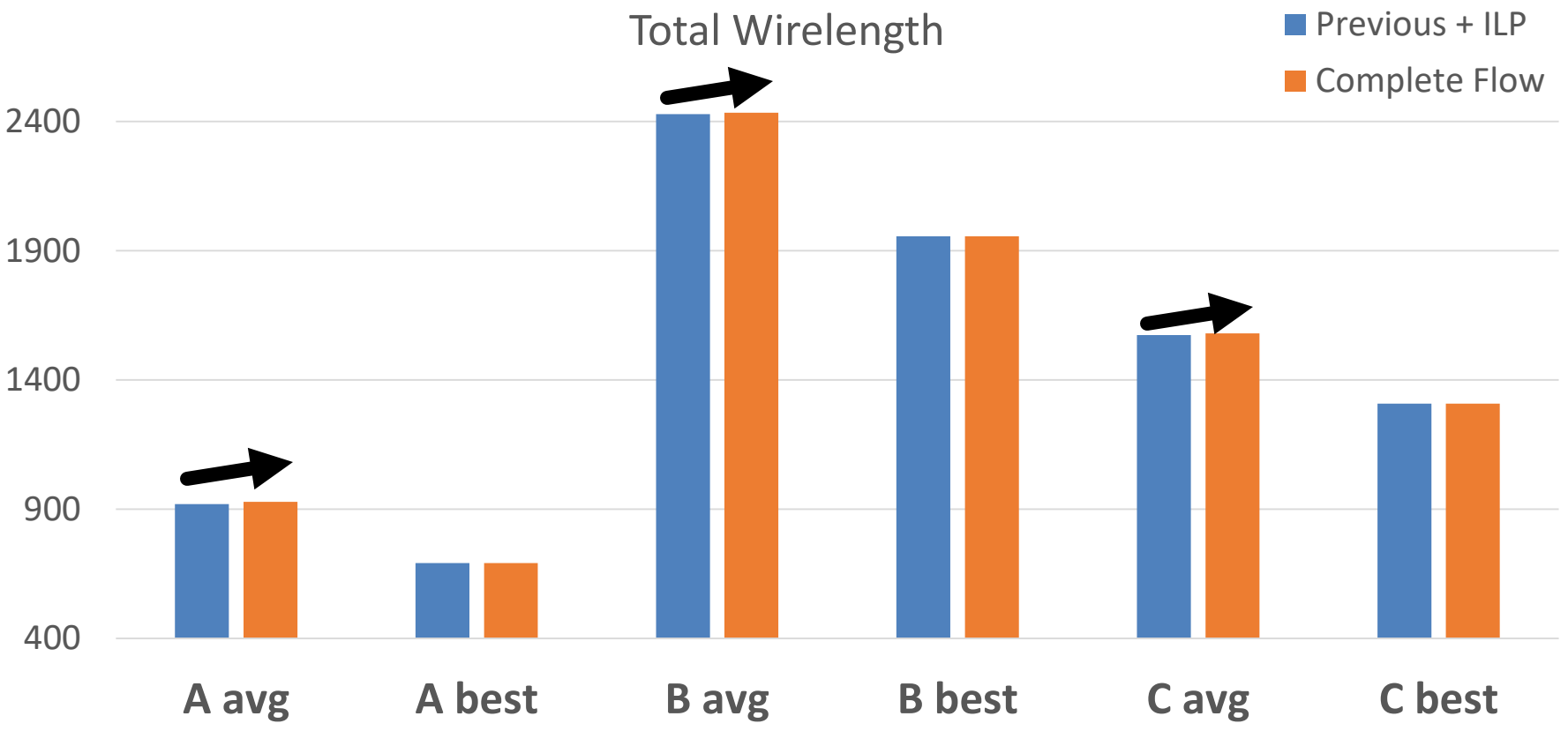
C

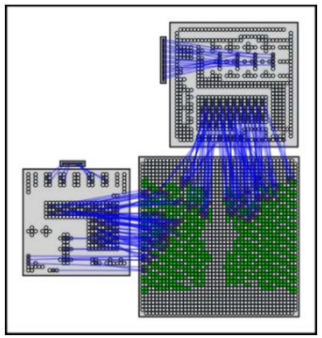


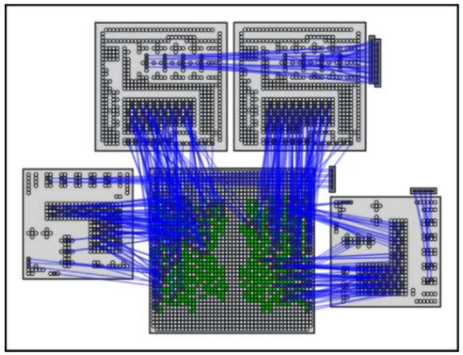
Previous Work vs. This Work

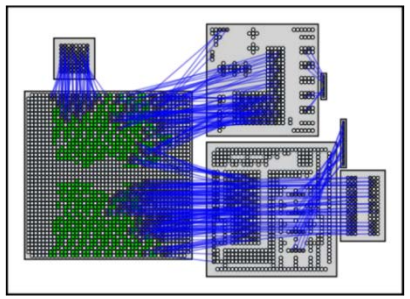


Previous Work vs. This Work









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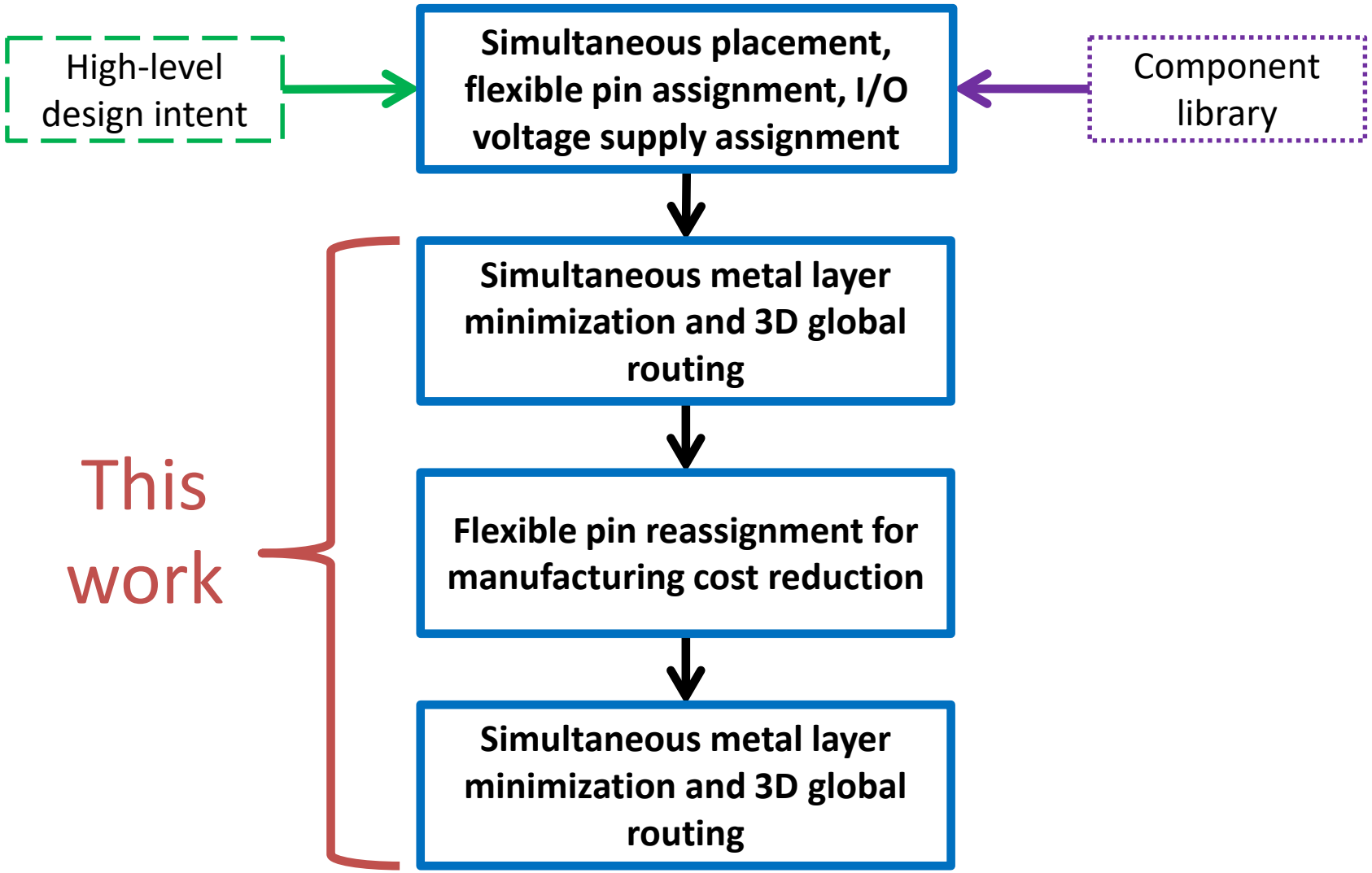

Conclusions

- Flexible interconnect enables other routing paths
- Reassign pins to permit easier routing
- Plan routing to reduce interposer metal layers
  - Reduce manufacturing costs
  - Improve yields

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