Optimizing DSA-MP Decomposition and Redundant Via Insertion with Dummy Vias

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Outline

- Introduction
- Preliminaries
- Problem Formulation
- Algorithm
- Experimental Results
- Conclusion

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What is DSA

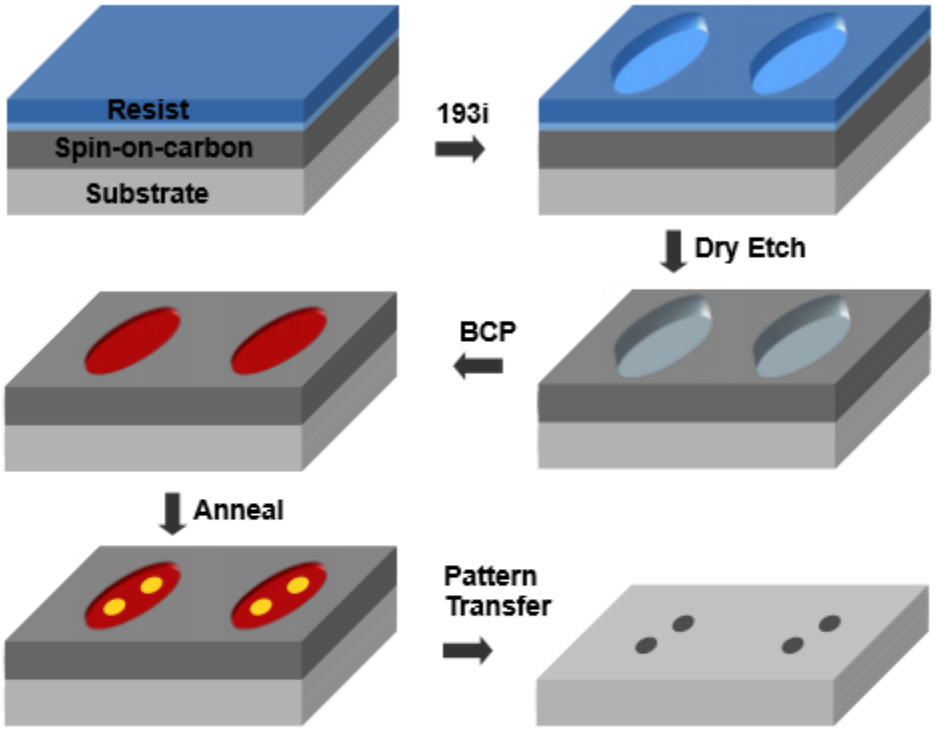
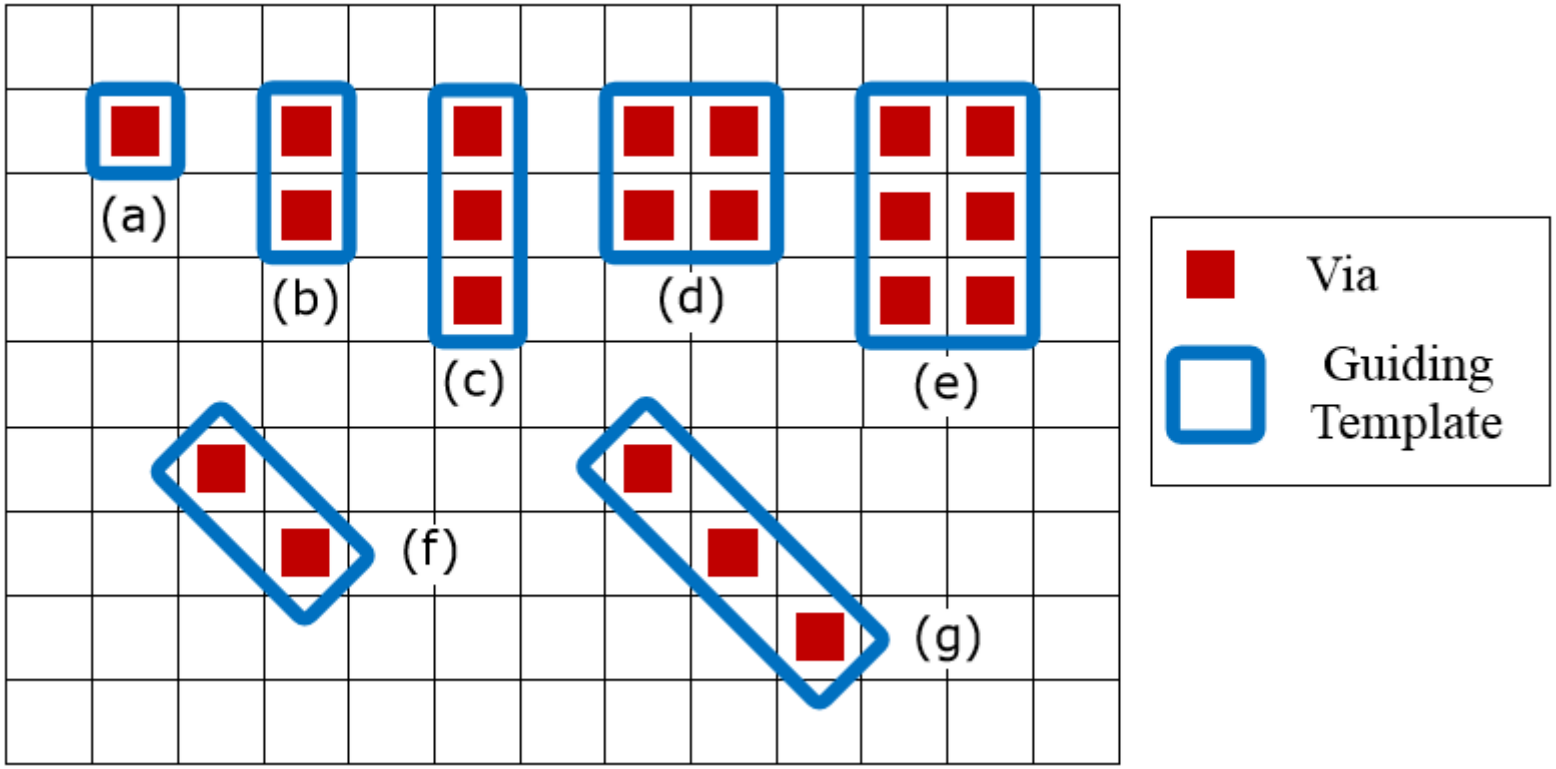


Figure 1: DSA process flow: 193i lithography and etch define the guiding template, the final DSA patterns are generated inside the template.

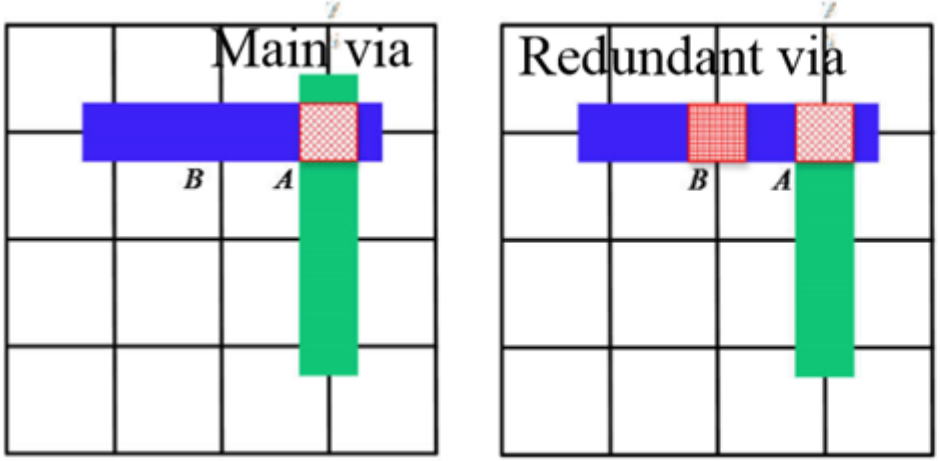
What is DSA (cont.)

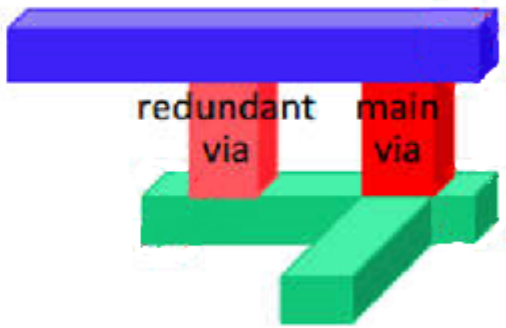
- To print vias using the DSA process, we must be able to group all the vias into a set of feasible guiding templates.



Redundant Via Insertion*

- Why do we need to insert redundant via?
  - Via failure has a critical impact on chip performance, functionality, and manufacturing yield.
  - Redundant via insertion is one of the most effective techniques recommended by foundries to provide via reliability.
- What is a redundant via?





* X. Jia, Y. Cai, Q. Zhou, and B. Yu. MCFRoute 2.0: A Redundant Via Insertion Enhanced Concurrent Detailed Router. In GLSVLSI'16

Introduction

- Previous works show that there are still some unmanufacturable vias.
  - We combine dummy via insertion to improve via manufacturability.
- Considering DSA with redundant via insertion and dummy via insertion may not solve the problem completely.
  - Multiple patterning is necessary for successful manufacturing when technology node goes beyond 10nm.

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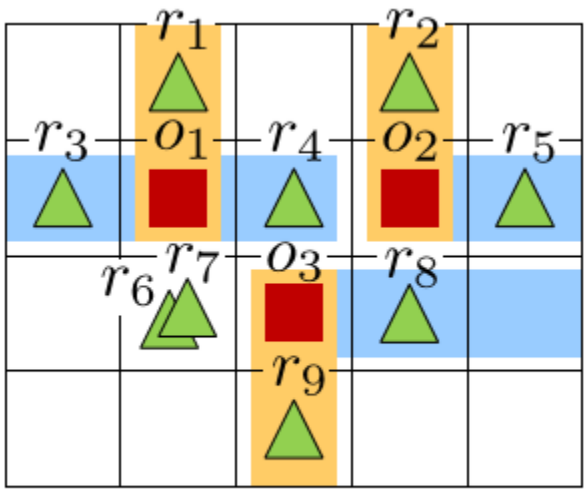
Guiding Template Assignment

- The goal of Guiding Template Assignment is to cover as many vias as possible by guiding templates.

- Because guiding templates are printed by traditional lithography, if the distance between two different guiding templates is less than min_litho_dis, they need to be manufactured using different masks.

Redundant Via and Dummy Via insertion

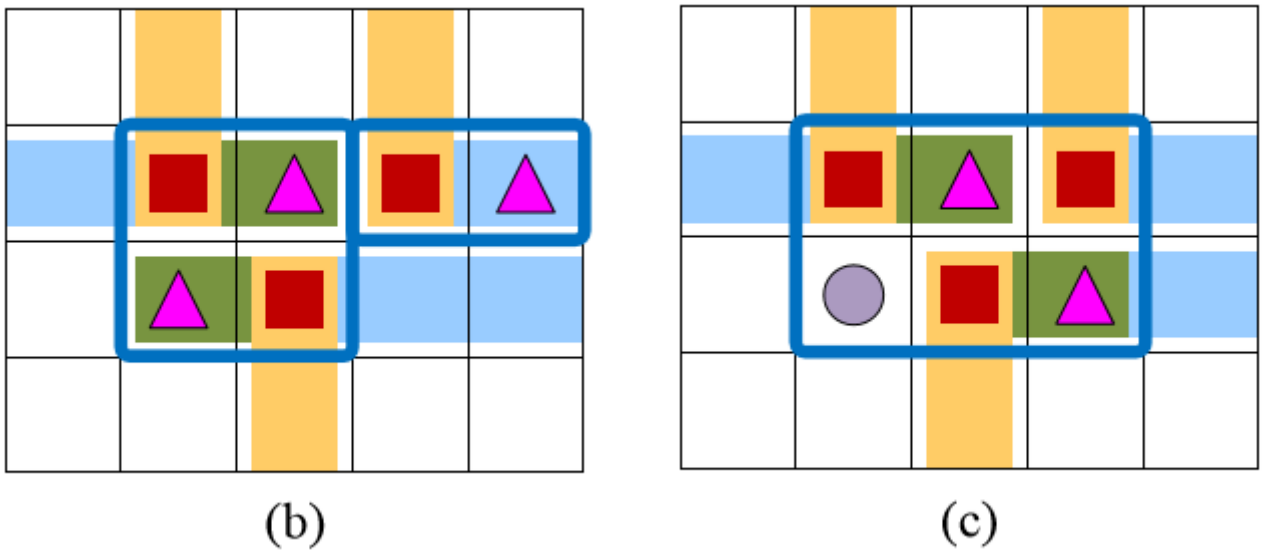
- To ensure the same functionality and minimize the impact on the layout, the position of redundant via candidate is feasible when the following two conditions are satisfied.
  - It is at the grid point horizontally or vertically adjacent to the original via.
  - There will be no short circuit or design rule violation if it is chosen.



(a)

Redundant Via and Dummy Via insertion

- Due to the characteristic of DSA, vias must form some specific patterns so that they can be assigned to the same guiding template.
- Increase the choices to form guiding templates with the help of dummy via insertion.



(b) (c)

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Problem Formulation

- Given a routing result, a pre-defined guiding template set, and the number of masks
- We want to find an optimal guiding template assignment with suitable dummy vias to
  - maximize the number of original vias patterned by DSA guiding templates, and
  - maximize the redundant via insertion rate.

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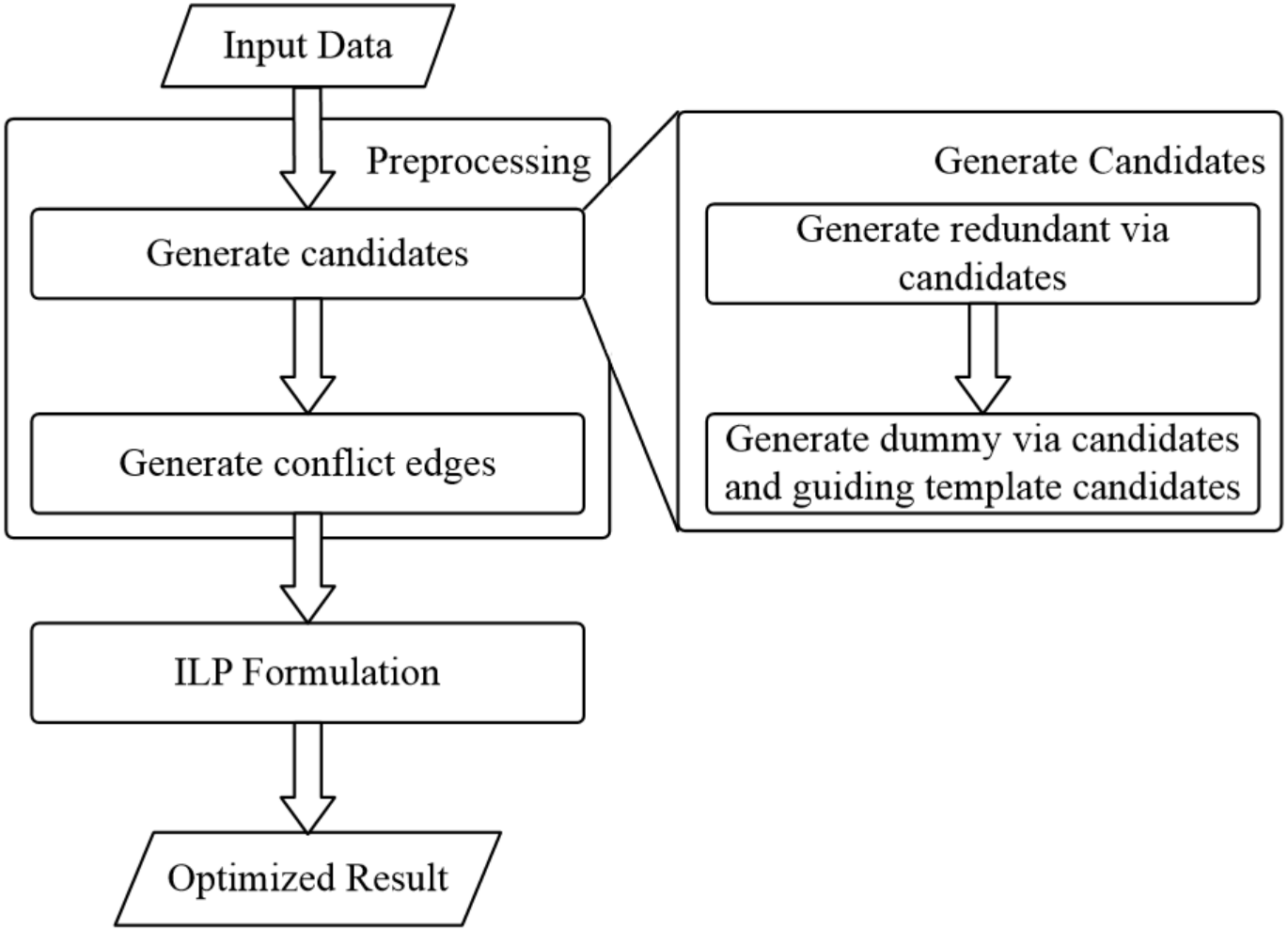
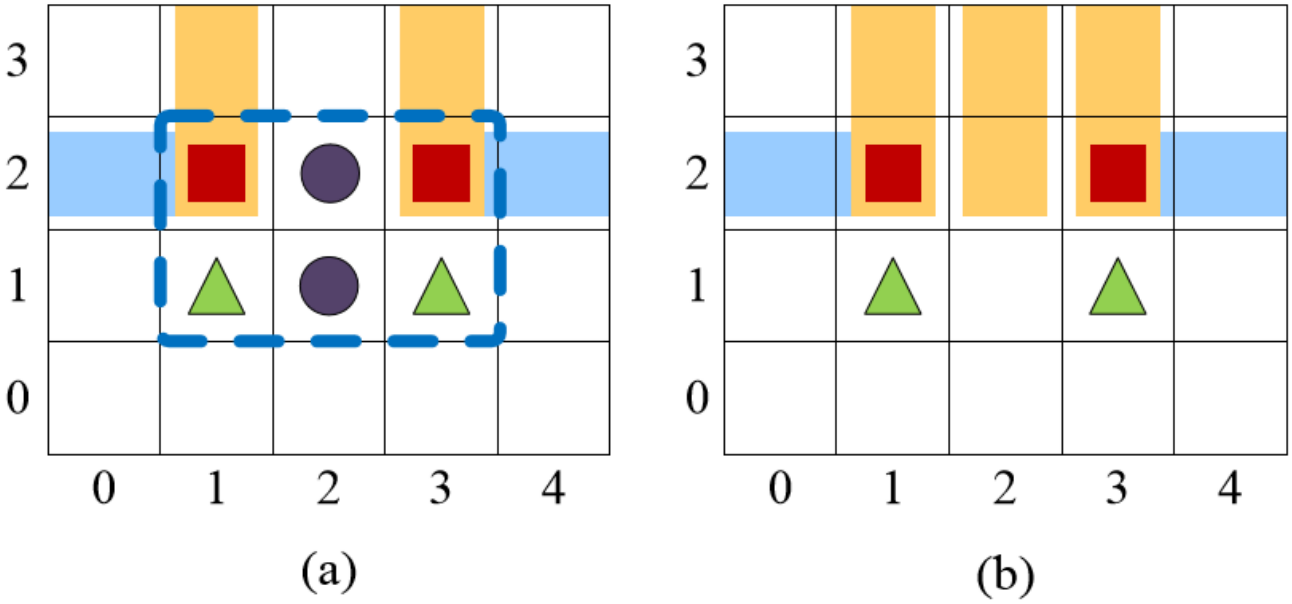
Overview


Input Data
Preprocessing
Generate candidates
Generate conflict edges
ILP Formulation
Optimized Result
Generate Candidates
Generate redundant via candidates
Generate dummy via candidates and guiding template candidates

Generate guiding template candidates and dummy via candidates

- For each original via o, we check its immediate neighbors to see if it is feasible to form a vertical/horizontal 1×2 DSA pattern with o.
  - all grid points covered by the pattern have an original via or a redundant via candidate
  - if the pattern covers some empty grid points and they can all be inserted with dummy via candidates

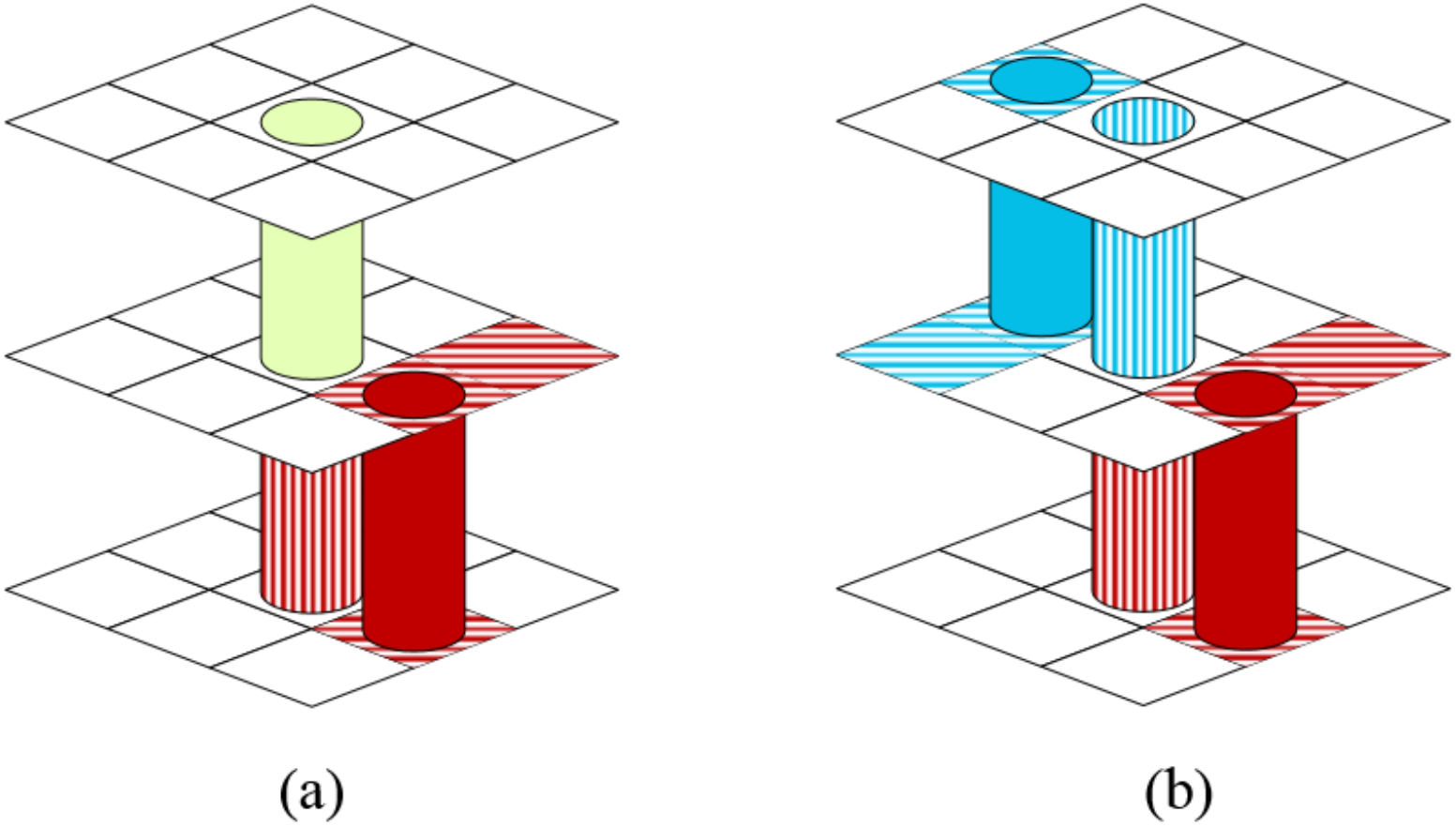


Conflicts between Via Candidates

- Via candidates at the same grid point will conflict.

- Inter-layer Conflicts
  - The insertion of redundant via or dummy via at one layer will influence the insertion of redundant via or dummy via at adjacent layers.

Inter-layer Conflicts



(a) (b)

Conflicts between Guiding Template Candidates

- Distance-conflict
  - The distance between two guiding template candidates is less than min_litho_dis and they are not overlapping with each other.
- Overlap-conflict
  - Two guiding template candidates overlap.

ILP Formulation

- After preprocessing, we get the information of **redundant via candidates**, **dummy via candidates**, **guiding template candidates**, and the **conflicts** between them.

- We propose an ILP formulation to get the optimal result that contains the **maximum number of original vias** and **most number of redundant vias** with no conflicts.

$$maximize \sum_{g_{x,y,z} \in OG} o_{x,y,z} + \alpha \sum_{r_j \in RV} r_j$$

Speed-up Technique

- Since a huge amount of candidates are generated after preprocessing, it is impractical to consider the entire layout as a single ILP.

- To solve this problem in reasonable time, we divide it into sub-problems without loss of optimality.
  - If two original vias o and o' are far away, then redundant via candidates belonging to them will not affect each other. Even the guiding template candidates covering them will not affect each other.

Speed-up Technique (cont.)

- In our experiment, the average number of variables we generated in each sub-problem is less than 0.1% of that when we consider the entire layout as a single ILP.

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Experimental Results

Benchmark	#vias	UC	[7]						Ours(DP)		
			DP-ILP			DP-AP					
		IR(%)	CR(%)	IR(%)	Time(s)	CR(%)	IR(%)	Time(s)	CR(%)	IR(%)	Time(s)
efc	4983	98.94	100.00	98.29	68.85	98.63	96.84	3.36	100	98.94	4.38
ecc	5523	99.35	100.00	98.80	56.26	98.55	97.44	3.8	100	99.35	4.13
ffu	7026	99.32	100.00	98.47	88.64	98.80	97.35	4.99	100	99.32	5.56
alu	7046	99.12	100.00	98.15	107.34	98.14	96.39	5.4	100	99.12	6.75
byp	28847	95.56	N/A	N/A	N/A	97.29	91.35	41.41	100	95.55	22.61
mul	62989	98.48	N/A	N/A	N/A	96.39	94.91	417.76	100	98.45	77.02
Avg.		98.46	N/A	N/A	N/A	97.97	95.71	79.45	100	98.45	20.08

[7] J. Ou, B. Yu, and D. Z. Pan. Concurrent guiding template assignment and redundant via insertion for dsa-mp hybrid lithography. In Proc. ISPD ’16.

Experimental Results

Benchmark	#vias	[6](SP)			Ours(SP)			Ours(DP)		
		UR(%)	IR(%)	Time(s)	UR(%)	IR(%)	Time(s)	UR(%)	IR(%)	Time(s)
Struct	12551	0.07	99.42	48	0.02	99.79	40.47	0	100.00	55.68
Primary1	8764	0.10	99.21	42	0.04	99.33	29.14	0	100.00	33.51
Primary2	32684	0.23	98.97	129	0.04	99.49	111.22	0	100.00	152.52
s5378	8649	11.68	61.78	33	2.05	75.27	34.41	0	92.39	35.88
s9234	6874	12.49	59.54	28	2.17	74.51	38.63	0	93.88	37.83
s13207	18780	9.37	66.93	80	1.60	79.28	99.96	0	95.88	91.80
s15850	22694	10.52	64.41	95	1.90	77.35	121.94	0	95.13	109.51
s38417	54225	9.65	65.71	234	1.78	78.13	320.35	0	95.87	292.08
s38584	74155	11.33	63.01	342	2.05	76.83	416.11	0	95.22	395.40
dma	34696	1.10	95.29	123	0.20	97.49	208.75	0	99.88	241.80
dsp1	30317	0.48	97.57	102	0.13	98.45	176.42	0	99.93	221.79
dsp2	31301	0.76	96.68	104	0.12	98.74	179.37	0	99.95	235.92
risc1	43858	0.62	96.93	151	0.15	98.04	216.61	0	99.85	294.65
risc2	44385	0.61	96.91	151	0.15	97.98	229.22	0	99.86	297.04
Avg.		4.93	83.03	118.71	0.89	89.33	158.76	0	97.70	178.24
Norm.		1.00	1.00		0.18	1.08		0	1.18	

[6] S. Y. Fang, Y. X. Hong, and Y. Z. Lu. Simultaneous guiding template optimization and redundant via insertion for directed self-assembly. In ICCAD ’15.

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Conclusion

- We present an effective and efficient optimal DSA-MP decomposition and redundant via insertion approach with dummy vias.

- We can see from the experimental results that DSA with double patterning can manufacture all of the original vias and insert optimal number of redundant vias.

Thank you for your attention.

Q&A