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Design of Multiple Fanout Clock Distribution Network for Rapid Single Flux Quantum Technology

USC

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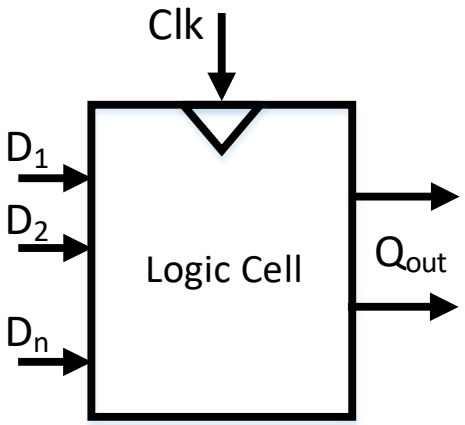
Motivation

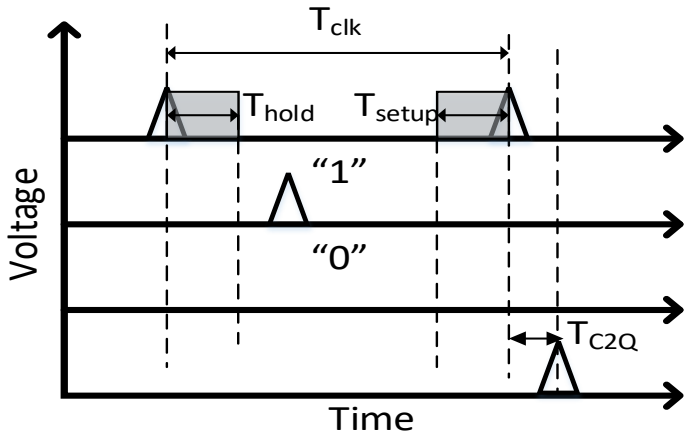
- RSFQ circuits are made of Shunted Josephson Junctions and inductances.
- Any RSFQ cell can only drive one other cell and for a larger fanout “Splitter” cells are to be used.
- RSFQ circuits are gate-level pipelined and need clock for every gate implying at least one splitter cell required for every gate.

- Reduction in the number of splitter → reduction in the area and the power consumption of the over circuit.

Basic Convention: Standard Protocol



Typical RSFQ Cell



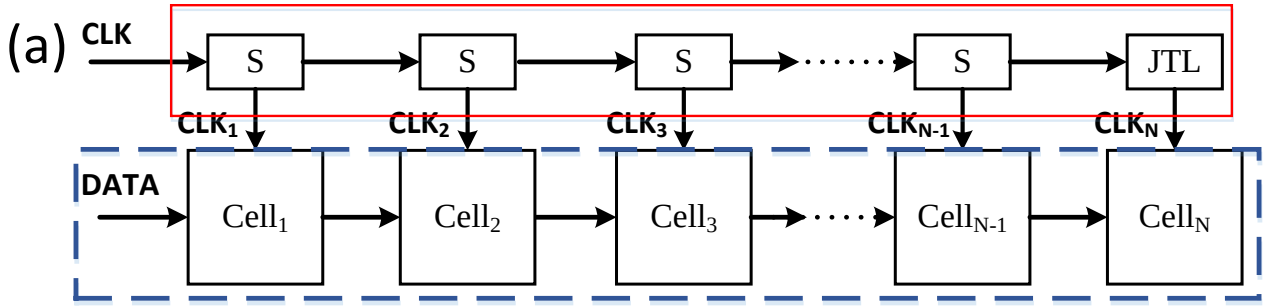
Standard timing

- **RSFQ Basic Convention:**
  Arrival of an SFQ pulse -> '1'
  Absence of a pulse -> '0'

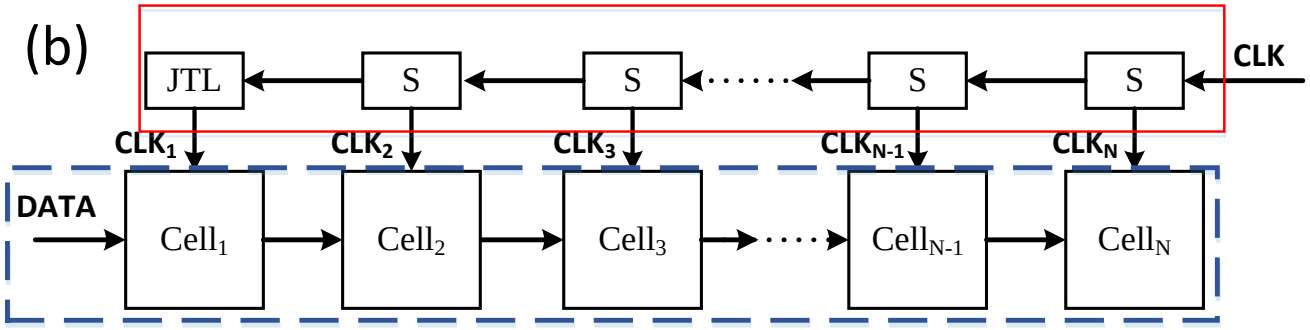
P. Bunyk , K. Likharev and D. Zinoviev "RSFQ logic/memory family: A new technology: Physics and devices", *Int J. High Speed Electron. Syst.*, vol. 11, no. 1, pp.257 -306 2001

Clock Distribution Network
(widely used)

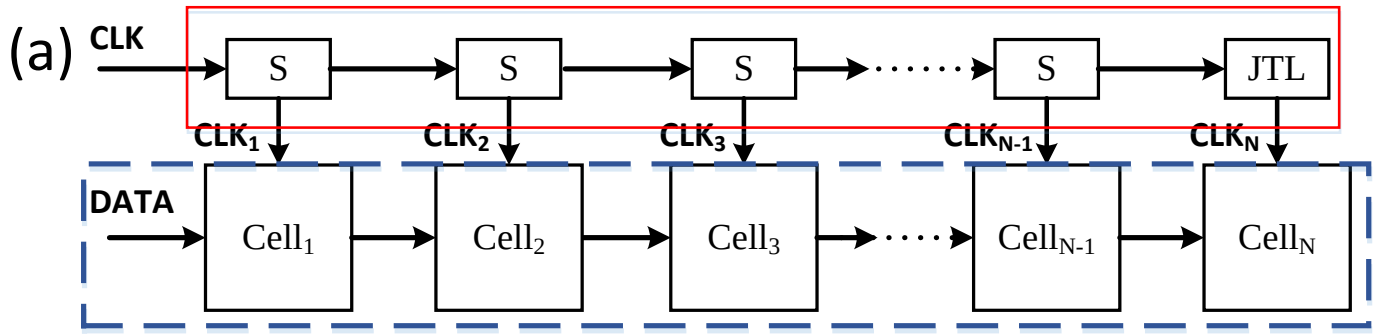
- Concurrent-Flow clocking



- Counter-flow clocking



Clock Distribution network

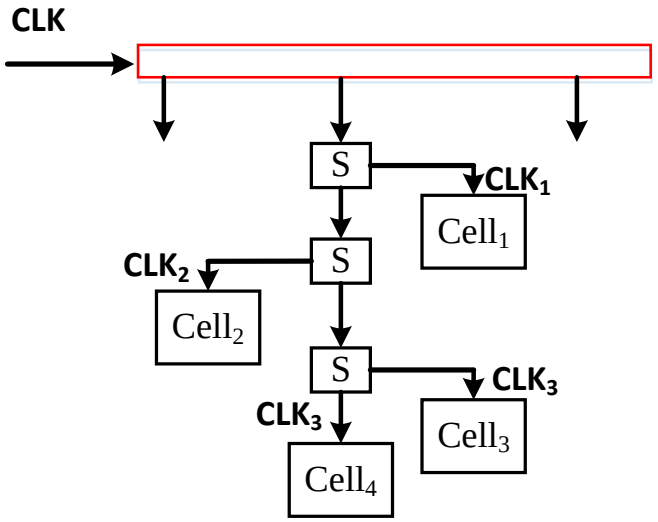


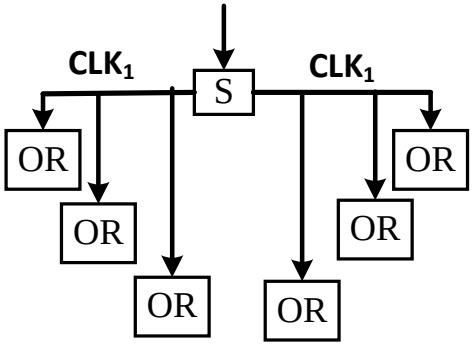
$Cell_2$

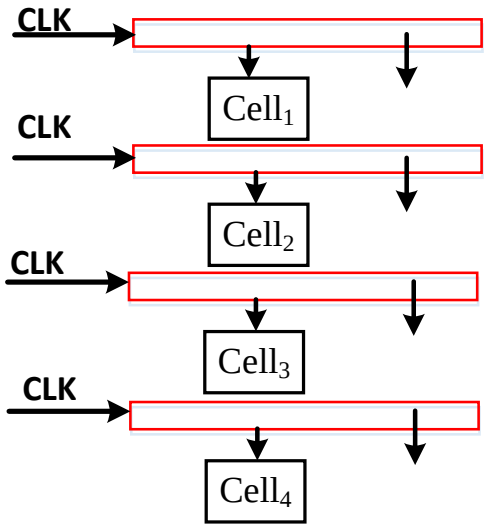
$Cell_3$

$Cell_4$

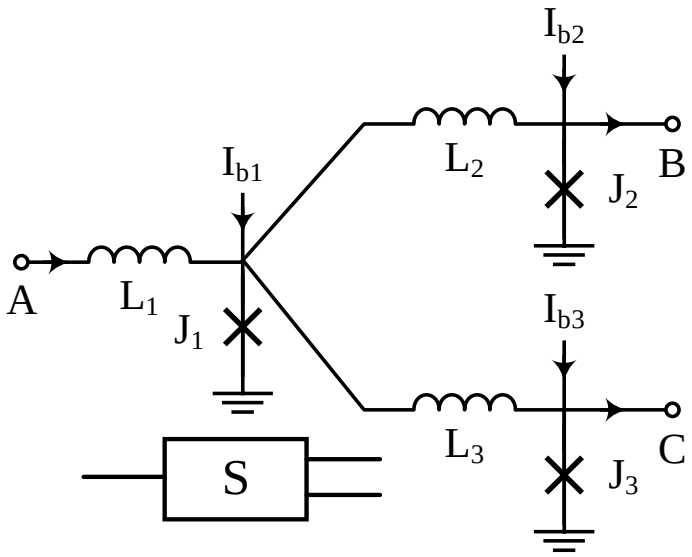
Distribution of clock at the same time



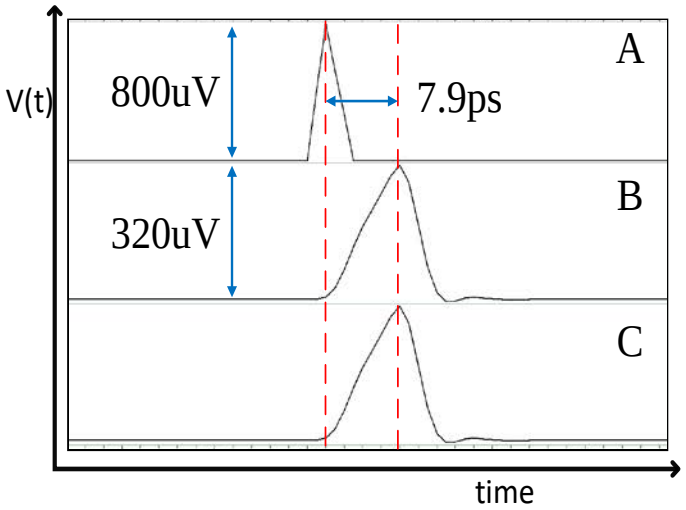




Splitter

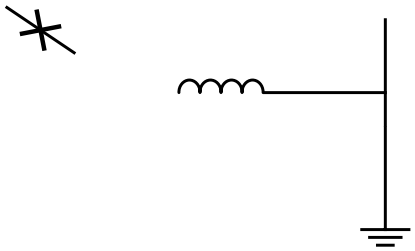


(a) Splitter implementation



(b) Pulse propagation (simulation result)

RSFQ Gate and interface JTL



OR gate with JTL interface.
(a) Core of the gate
(b) JTL interface

Algorithm: Modification of Interface

1 *At the output of clock network, connect one more cell (incrementing fanout of splitter cell by one)*

2 **IF** the output cannot be read by all receiver cells

3 *Increase the bias current and go to 2 (cannot go beyond the sum of critical currents of both junctions)*

ELSE

4 *Calculate yield of cell*

IF yield is acceptable

5 *Store the solution for current fanout and go to 1*

ELSE

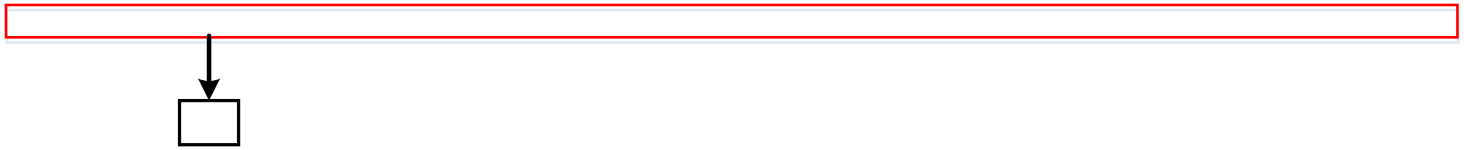
6 Increase critical current (I_c) of JJs

7 **IF** new I_c is beyond the margin of Ic of base cell

8 *Cannot obtain better solution than previous solution Terminate*

9 Go to 2

Test structures



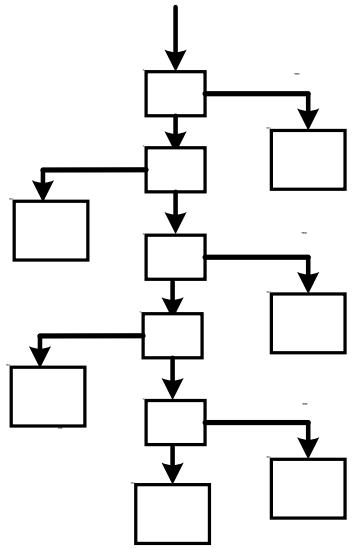
Fanout =1
(baseline case)

Fanout =2
(baseline case)

Fanout =3
(baseline case)

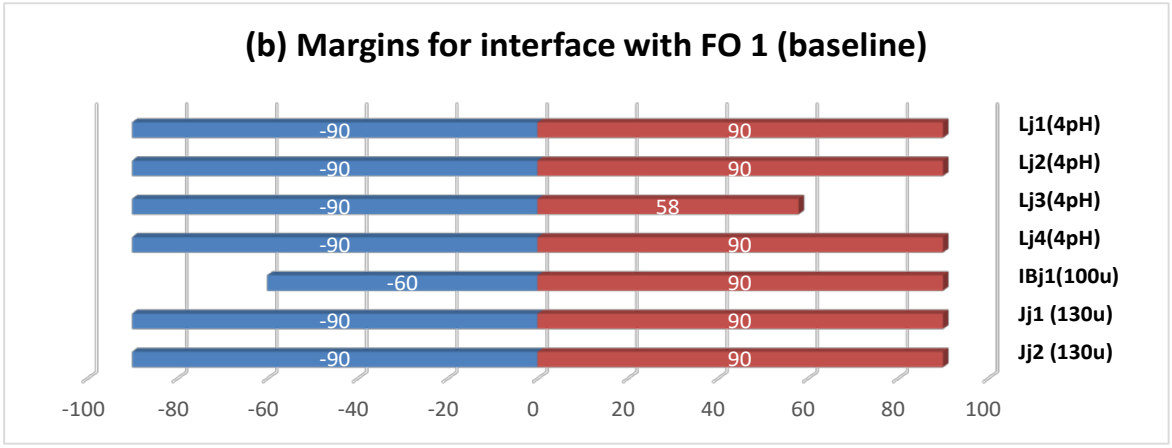
Results Comparison

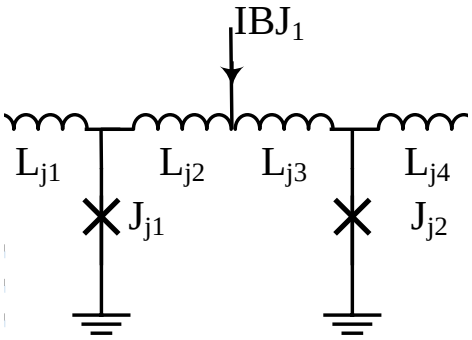
Test Structure		FO 1 (a) baseline	FO 2 (b)	FO 3 (c)
Delay (ps)	C2FS	23.1	11	10
	C2FQ	29	16	14
Static power (µW)		12.3	11.4	10.5
Area	# of JJs	81	75	69
	Inductance (pH)	422	390	358
	Approx. (μm^2)	1112	1014	916

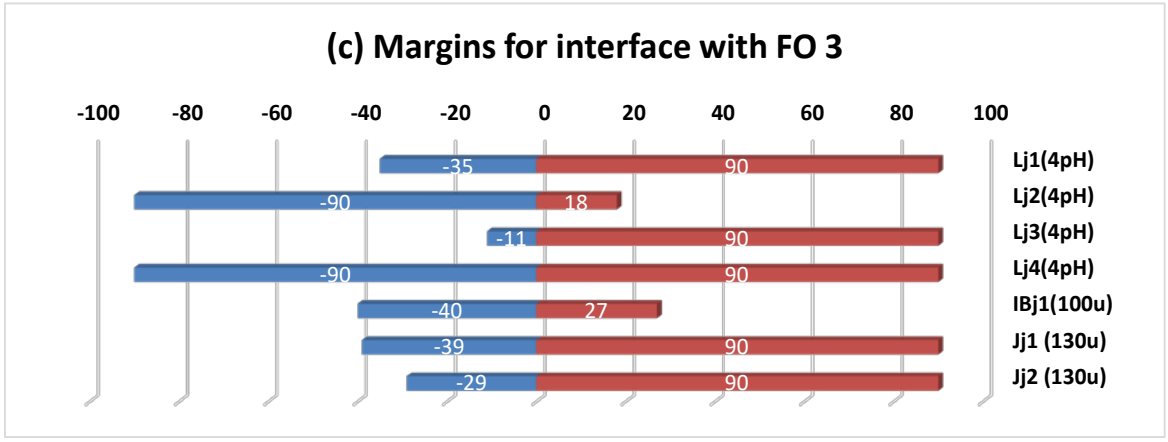


C2FS – Clock to final Splitter Output
C2FQ - Clock to Q value of final cell in the structure

Margins


(b) Margins for interface with FO 1 (baseline)
-90
90
-90
90
-90
58
-90
90
-60
90
-90
90
-90
90
Lj1(4pH)
Lj2(4pH)
Lj3(4pH)
Lj4(4pH)
IBj1(100u)
Jj1 (130u)
Jj2 (130u)
-100
-80
-60
-40
-20
0
20
40
60
80
100


IBJ1
Lj1
Lj2
Lj3
Lj4
Jj1
Jj2


(c) Margins for interface with FO 3
-100
-80
-60
-40
-20
0
20
40
60
80
100
-35
90
-90
18
-11
90
-90
90
-40
27
-39
90
-29
90
Lj1(4pH)
Lj2(4pH)
Lj3(4pH)
Lj4(4pH)
IBj1(100u)
Jj1 (130u)
Jj2 (130u)

Yield

Fanout	Bias current (I_b)	Critical current of JJs (I_c)	OR yield	
			Margin based	Monte Carlo
1	100μA	130μA	0.999	0.999
2	150μA	130μA	0.999	0.972
3	250μA	150μA	0.981	0.865

Conclusion

- Yield suffers as we increase the fanout count.
- If the process variations can be brought low, fanout>1 is realizable for splitter.
- With some modification of the algorithm, we can get greater fanout for general RSFQ cells.