ASIA SOUTH PACIFIC DESIGN AUTOMATION CONFERENCE

Parasitic-Aware GP-Based Many-Objective Sizing Methodology for Analog and RF Integrated Circuits

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Outline

- Problem definition
- Previous works
- Our work:
  - Synthesis flow
  - Parasitic-awareness
  - The geometrical programming (GP)
  - The theta-dominance-based evolutionary algorithm (θ-DEA)
- Experimental results and conclusions

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Circuit Sizing Problem

Given: A circuit topology

Find: Device sizes and bias information that make the performance meet the specification.

- The biggest problem in the sizing task:
  - Performance not converge between pre- and post-layout (Due to layout effects)
  - Unexpected design cycles
  - Parasitic effects: primary and inevitable

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Recent Works on Automatic Sizing

- Synthesis approaches categorization:[1]

- How parasitics considered:
  - Analytic modelling (our approach)
  - Heuristic exploration
  - From extraction and simulation tools

[1]T. Liao and L. Zhang, “Analog integrated circuit sizing and layout dependent effects: A review,” *Microelectronics and Solid State Electronics*, 3(1A), pp. 17-29, 2014.

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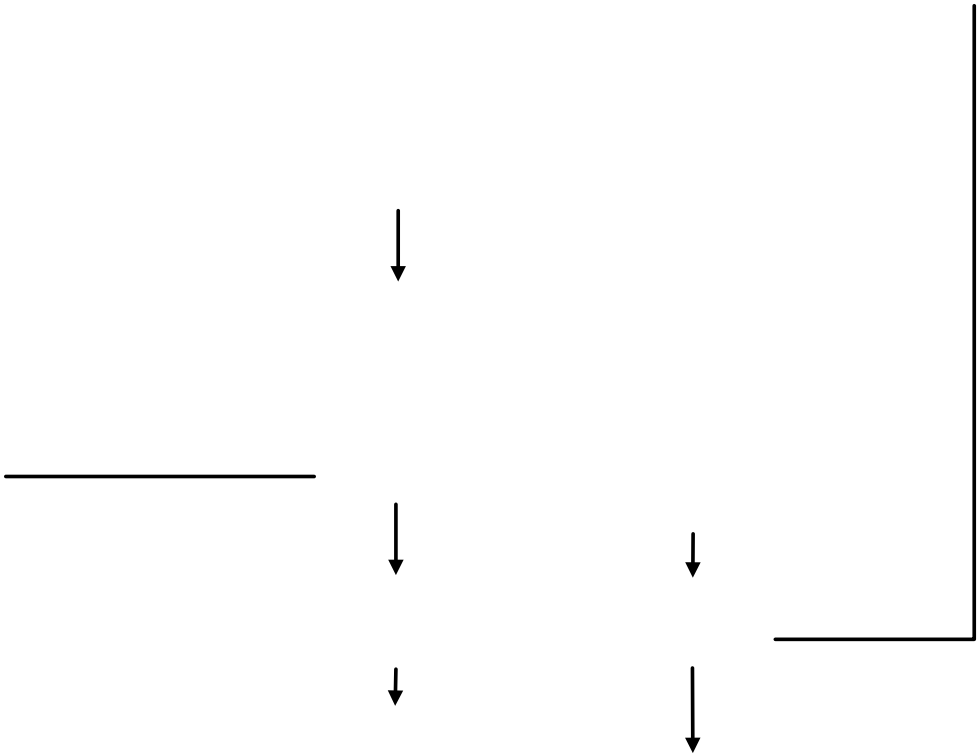
Synthesis Flow



- **Geometric Requirements:**
  - Area and other constraints representing relationship between modules & devices
- **Preferable Floorplan:**
  - B*-tree + SA-engine optimize
  - Symbolic interconnect length

Fig. 1. The GP-many-objective two-phase hybrid sizing flow

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Parasitic-awareness

- Interconnect parasitic models [2][3]
  - New models firstly being applied to GP platform

- Device parasitics from foundry provided (PDK)
  - GP phase (technology files)
  - EA phase (model in netlist, called in simulation)

[2] G. Shomalnasab and L. Zhang, “New analytic model of coupling and substrate capacitance in nanometer technologies,” *IEEE Trans. on Very Large Scale Integration* (*VLSI*) *Systems*, vol. 23, no. 7, pp. 1268-1280, 2015.

[3] L. Zhang, N. Jangkrajarng, S. Bhattacharya, and R. Shi, “Parasitic-aware optimization and retargeting of analog layouts: a symbolic template approach,” *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol. 27, no. 5, pp. 791-802, 2008.

Interconnect Parasitics

- Interconnect length:
  - Int._length = **f**(w, l, nf, interconnect relationship)
- Express parasitic R and C in symbolic way:
  - Para._R,C = **g**(Int._length, Int._width, parameters)
  - Interconnect relationship ← preferable floorplan
  - w, l, nf, and Int._width { GP variables; EA variables }
- Merits:
  - Models reusable in GP and EA
  - Parasitic-awareness throughout the two phases

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Geometrical Programming

- A GP is a type of mathematical optimization problem characterized by objective and constraint functions that have a special form (posynomial and monomial). It is a class of nonlinear optimization.

GP Pros & Cons

- Pros:
  - Quickly determine a first-level optimum global solution
- Cons:
  - Requires in a convex form (GP-compatible)
  - Controversy of accuracy
- Contribution:
  - Two actions to address the cons

Action to the 1st Cons

- Transfer non-posynomial to be GP compatible:

$$f_i(x) = \frac{ax^b + cx^d + \cdots}{pq^r + lm^n + \cdots}$$

$$ax^b + cx^d + \cdots \leq temp_1, \quad \text{(posynomial)}$$
$$pq^r + lm^n + \cdots \leq temp_2, \quad \text{(posynomial)}$$
$$temp_1/temp_2 = f_i(x). \quad \text{(monomial)}$$

Action to the 2nd Cons

- Idea of two-phase sizing process:
  - GP solution => Cadence verification => elite
  - Improve the elite: 2nd-phase optimizer with numerical simulation (fix the accuracy issue!)
- New problem:
  - Large EA search space + simulation => slow
- Solution:
  - Benefits of GP-elite:

    Imply information => shrink variable ranges/trimmed space => decreases search configuration and time

- In order to be efficient: GP and EA cannot be isolated!

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A many-OEA: θ-DEA

- Multi-objective EA (MOEA):
  - Weak in handling problems with more than 3 objectives
- Analog circuit design:
  - > 3 objectives
- Many-OEA*:*
  - Good for >3 objectives
  - θ-DEA:
    - Structural strength of NSGA-III (H. Jain and K. Deb, 2014)
    - Aggregation function as the selection scheme from MOEA/D (Q, Zhang, 2007)
    - First practice in sizing domain

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Experimental Circuits

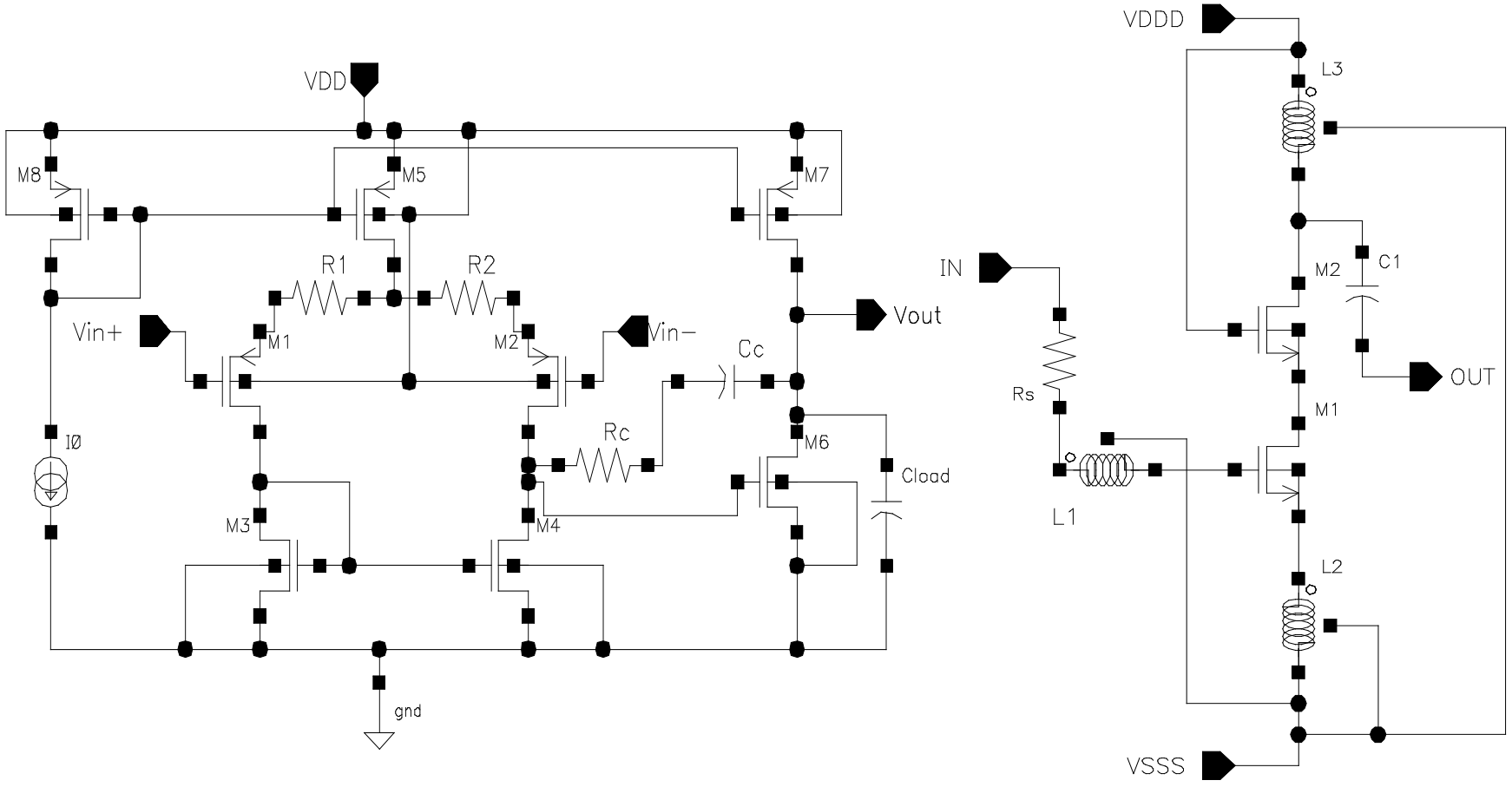
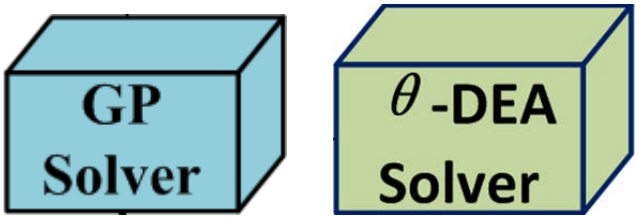


Fig. 2. Circuit diagrams for a): two-stage OpAmp and b): Cascode common source LNA with source degeneration

Experiment Setups

- Schemes:



One solution: best cost, performance

One set: average cost, SR

  - Sch-0 and Sch-1 to 4: GP elite? large or small EA setting?

- Cost function:
  - minimize $\sum_{i=1}^{n} \alpha_i \cdot \frac{S_i}{P_i} + \sum_{j=n+1}^{m} \beta_j \cdot \frac{P_j}{S_j}$
  - Performance vector ⟶ single cost as a representative

Experimental Results: Op-Amp

Table I. Settings and performance of the Two-Stage OpAmp

OpAmp 0.18um: Schemes	GP	Many-objective improved θ-DEA Methods			
	0:	1: GP-Small	2: GP-Large	3: NoGP-Small	4: NoGP-Large
Best cost	0.593	0.460	0.458	0.478	0.450
Average cost	-	0.569	0.528	0.552	0.519
Successful rate	-	21.88%	5.36%	25.00%	30.36%
Run Time(hrs)	1.31s	2.25	8.25	2.25	8.25
Specification	Performance				
Gain > 60dB	88.93 (0.675)	80.75 (0.743)	73.26 (0.819)	72.46 (0.828)	85.97 (0.698)
UGF > 1M	1.50 (0.667)	5.52 (0.181)	20.83 (0.048)	4.32 (0.231)	4.06 (0.246)
PM > 60°	80.13 (0.749)	87.59 (0.685)	91.32 (0.657)	131.35 (0.457)	124.41 (0.482)
GM > 10dB	35.33 (0.283)	43.48 (0.230)	32.26 (0.310)	25.34 (0.395)	26.82 (0.373)

Experimental Results: LNA

Table II. Settings and performance of the Low Noise Amplifier

LNA 90nm: Schemes	GP	Many-objective improved θ-DEA Methods			
	0:	1: GP-Small	2: GP-Large	3: NoGP-Small	4: NoGP-Large
Best cost	0.866	0.709	0.753	0.766	0.766
Average cost	-	0.765	0.782	0.766	0.766
Successful rate	-	15.63%	8.93%	3.13%	1.79%
Run Time(hrs)	1.76s	2.50	8.50	2.50	8.50
Specification	Performance				
Gain > 15dB	20.32 (0.738)	19.34 (0.776)	19.16 (0.783)	16.47 (0.911)	21.00 (0.714)
NF < 2.5dB	1.87 (0.748)	2.01 (0.804)	2.022 (0.809)	2.20 (0.878)	2.12 (0.847)
S11 < -15dB	-15.16 (0.989)	-19.41 (0.773)	-23.67 (0.634)	-29.13 (0.515)	-22.17 (0.677)
S22 < -15dB	-15.16 (0.989)	-30.94 (0.485)	-19.05 (0.787)	-19.79 (0.758)	-18.14 (0.827)

Conclusion

- Two-phase hybrid sizing flow
  - Floorplan optimization
  - Parasitic-awareness:
    - intrinsic parasitics
    - interconnect parasitics
  - GP
  - θ-DEA with numerical simulation
- Experimental analysis
  - Methodology efficacy: easy and hard problems


Thank You for Your Attention!
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