High-Speed Stochastic Circuits Using Synchronous Analog Pulses

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Overview

- **Introduction**
  - Stochastic Computing, advantages, main weakness
  - Representation of stochastic numbers
- **Stochastic Number Generation**
  - Conventional approach
  - Proposed approach: PWM
- **Correlation in stochastic circuits**
  - Operations with correlated inputs, advantages, disadvantages
  - Low cost sorting unit, stochastic comparator
- **Stochastic Operations with synchronous PWM signals**
- **Experimental results**
  - Hardware cost, operation time, performance comparison
- **Sources of computational error**
- **Conclusions**

Introduction

- **Stochastic Computation**
  - A re-emerging computing paradigm: introduced in 1969
  - Logical computation on random bit streams

  - Value: **probability of obtaining a one versus a zero**
    - **Unipolar [0, 1] positive**
      - Each bit has probability X of being 1
    - **Bipolar [-1, 1] positive, negative**
      - Each bit has probability (X+1)/2 of being one

    - **000111, 1010, 110010 = 0.5 (unipolar), 0.0 (bipolar)**

  - **Variable length bit streams**

Introduction

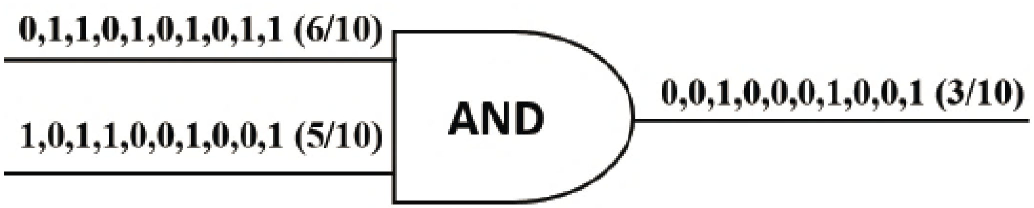
- **Key Advantages**
  - Simple hardware for complex operations
    - Multiplication: **AND** (unipolar), **XNOR** (Bipolar)
    - Scaled Addition: **MUX**
  - Gracefully tolerate noise
    - Redundant representation provides error tolerance
    - Stochastic: **0010000011000000 (3/16)** -> 4/16=0.25
    - Binary: 0.0011=0.1875 -> 0.1011=0.68
  - Skew tolerance
    - **Polysynchronous stochastic circuits [Najafi et al, ASP-DAC, 2016]**

Introduction

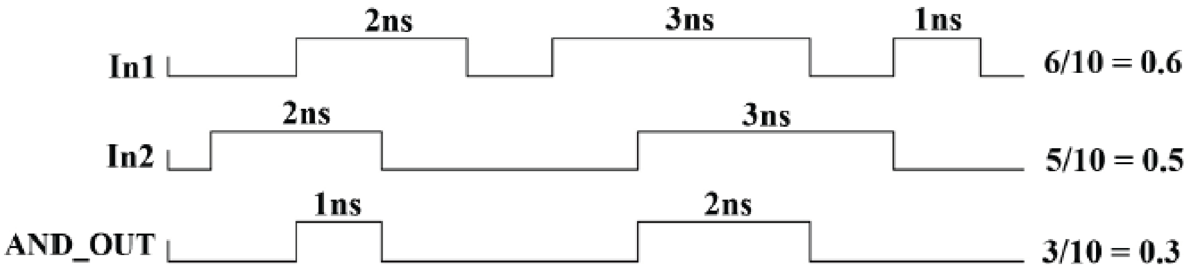
- Main Weakness
  - High accuracy ~ Long stochastic streams
  - Long computation time -> High energy consumption
    - Much slower
    - More energy consumption
      - than conventional binary design

Introduction

- **Representation of Stochastic Numbers**
  - **Digital**
    - Probability of obtaining a one versus a zero

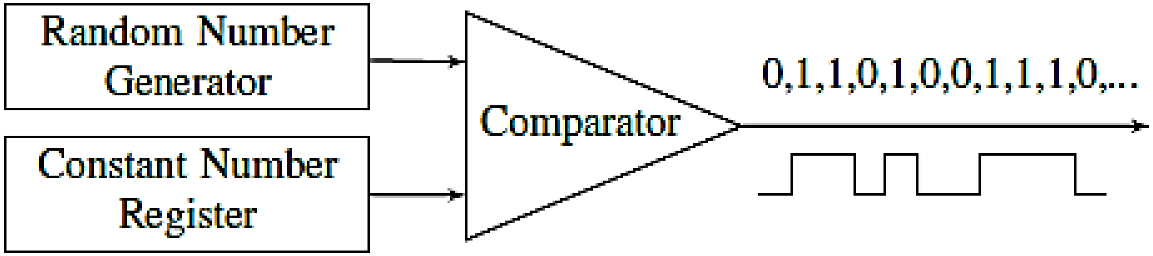


  - **Analog**
    - Encoding the value as the **fraction of time the signal is high**



Stochastic Number Generation

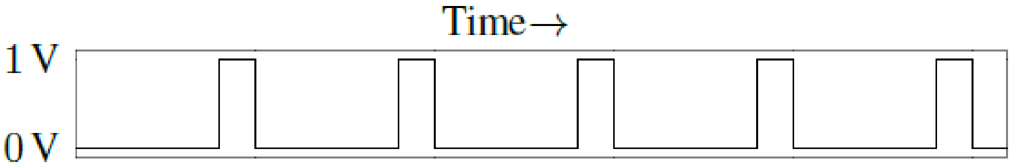
- **Conventional approach**
  - Using random or pseudo-random constructs
    - e.g. LFSR



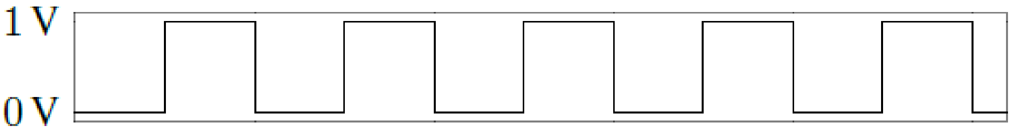
- **Proposed approach**
  - **Pulse Width Modulation**
    - **Analog periodic pulses signals as the stochastic number**

Stochastic Number Generation

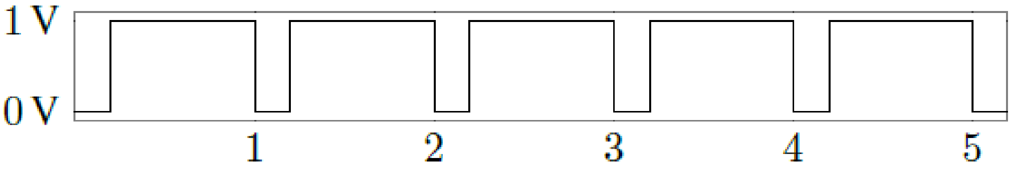
- **PWM signals as the stochastic number**
  - Defined by a **frequency** and a **duty cycle**.
  - **Duty cycle** describe the amount of high time



(a) 20% duty cycle



(b) 50% duty cycle



(c) 80% duty cycle

PWM signals with different duty cycles.

Correlation in Stochastic Circuits

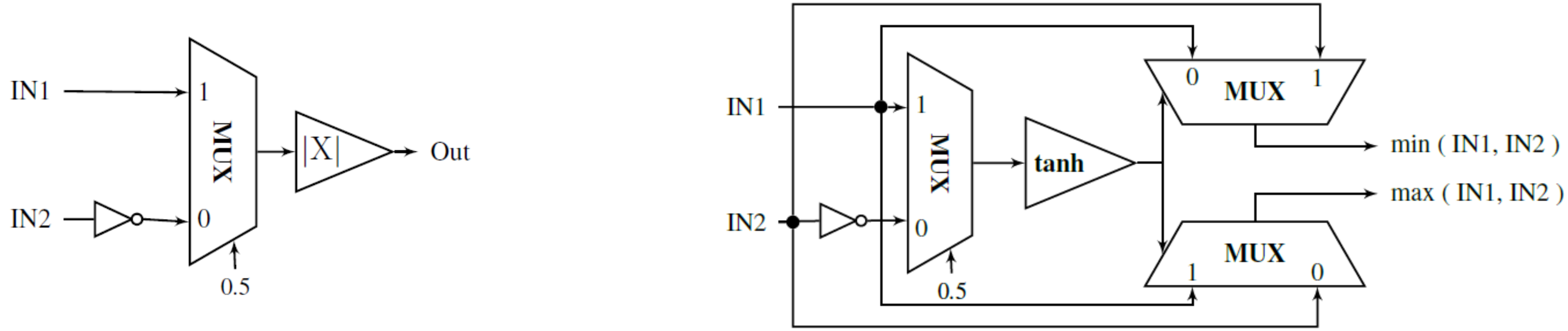
- **Stochastic Operations based on their inputs**
  - **Independent** or uncorrelated. 110101, 101100
    - **AND**: Multiplication

  - **Correlated**. 111100, 110000
    - **XOR**. Absolute value subtraction |X1 – X2| : **001100**
    - **AND**. Minimum: **110000**
    - **OR**. Maximum: **111100**

  - **Insensitive** to correlation
    - **MUX.** Scaled addition/subtraction

Correlation in Stochastic Circuits

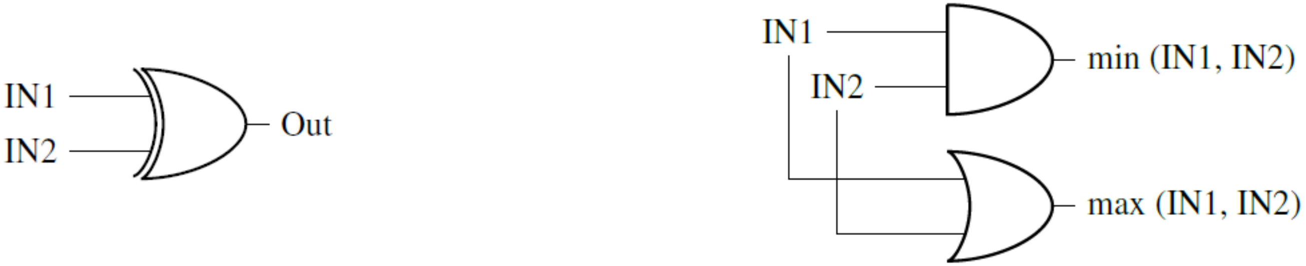
Absolute Value Subtraction   **Basic Sorting Unit (min, max)**



(a)

(a) Both correlated and uncorrelated Inputs [Peng *et al.* TVLSI’ 16]

- **FSM-based operations (|X|, tanh) are expensive**



(a)

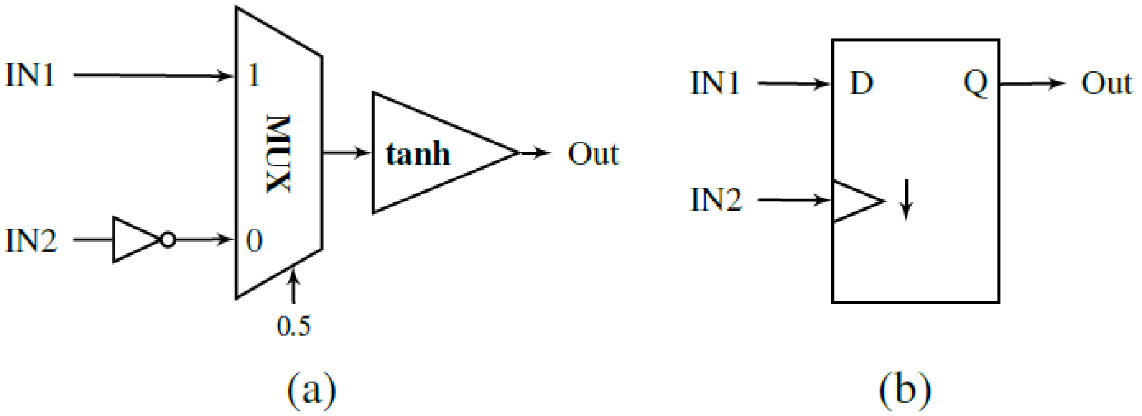
(b) Only correlated Inputs [Alaghi and Hayes, ICCD’ 13]

- **Much cheaper when working only on correlated inputs**

Correlation in Stochastic Circuits

- **Still no general method for synthesizing stochastic operations to work on correlated inputs**

- **We propose low cost stochastic comparator**



(a) (a) High-cost stochastic comparator [Li and Lilja, ICCD’11]

(b) (b) Proposed low cost stochastic comparator

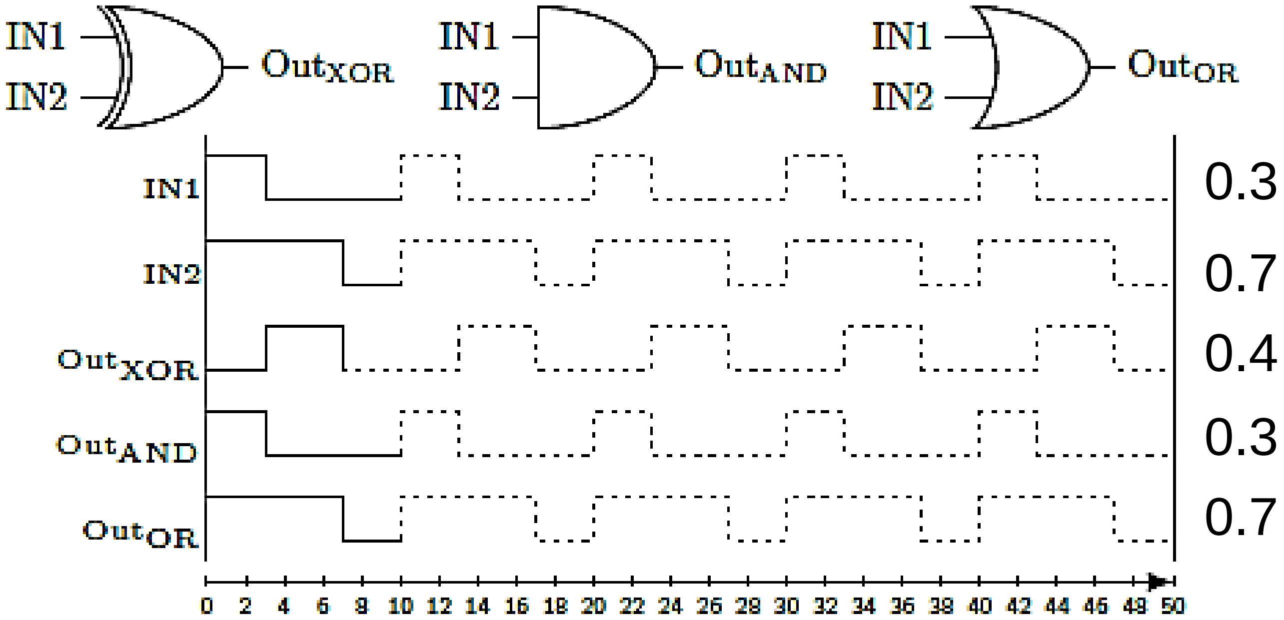
Stochastic operations with synchronous PWM signals

- **We define correlation for analog representation of SN**
- **High correlation in PWM signals**
  - 1) choosing the **same frequency** for the input signals
  - 2) having **maximum overlap** between the high parts

- **Advantage**:
  - Still have **area saving** benefit of correlated stochastic
  - **Accurate output** after running for only one period
    - Eliminating random fluctuation inaccuracy

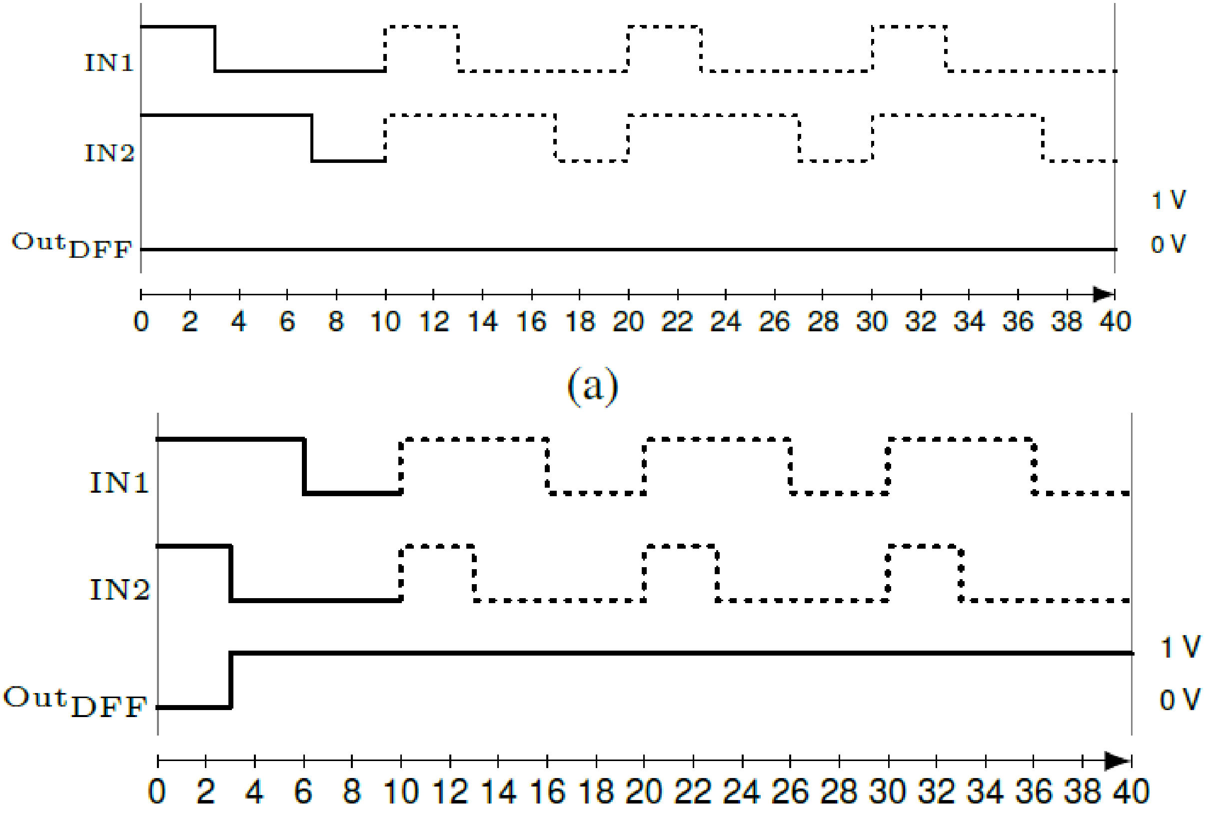
- **Disadvantage**
  - Difficult to provide synchronization (correlation) in the second (or higher) levels of the circuit.

Stochastic operations with synchronous PWM signals



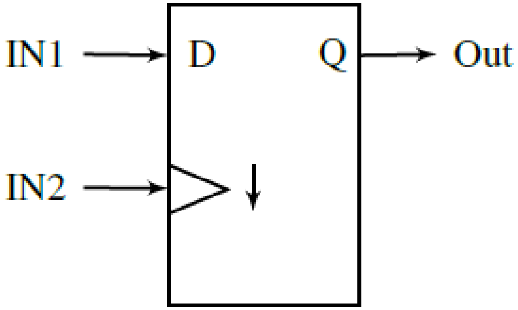
Examples of performing stochastic **absolute-valued subtraction**, **minimum**, and **maximum** operations on two **synchronized PWM signals**.

Stochastic operations with synchronous PWM signals



(a)

(b)



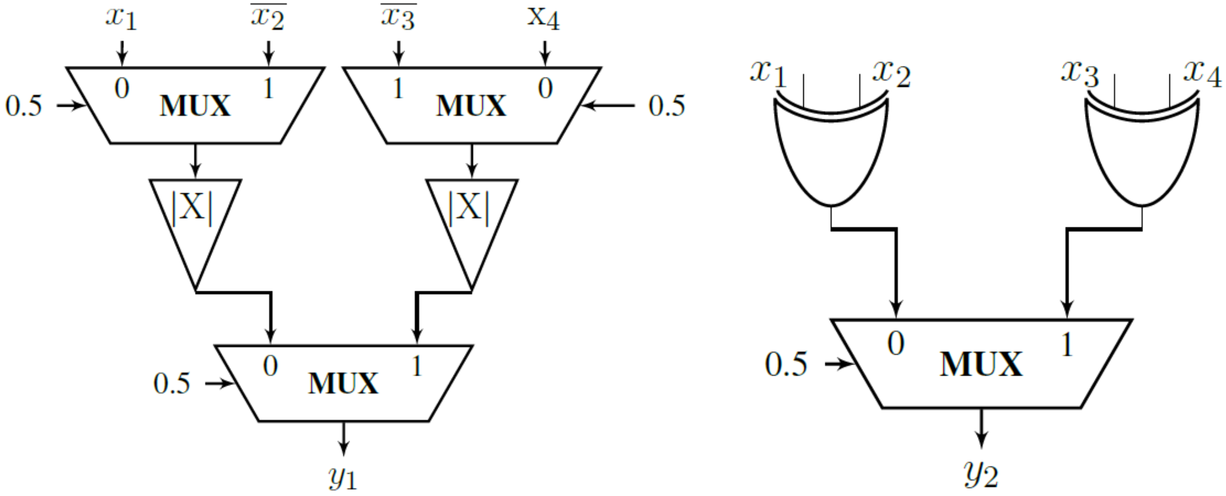
Examples of comparing SN, represented by correlated PWM signals, using the proposed stochastic comparator.

IN1 < IN2 : Out=0, IN2 > IN1: Out:1

Experimental Results

- **Three image processing case studies**
  - **Robert's cross edge detection**

$$y_1 = 0.5 \times (0.5 \times |x_1 - x_2| + 0.5 \times |x_3 - x_4|)$$
$$y_2 = 0.5 \times (|x_1 - x_2| + |x_3 - x_4|)$$



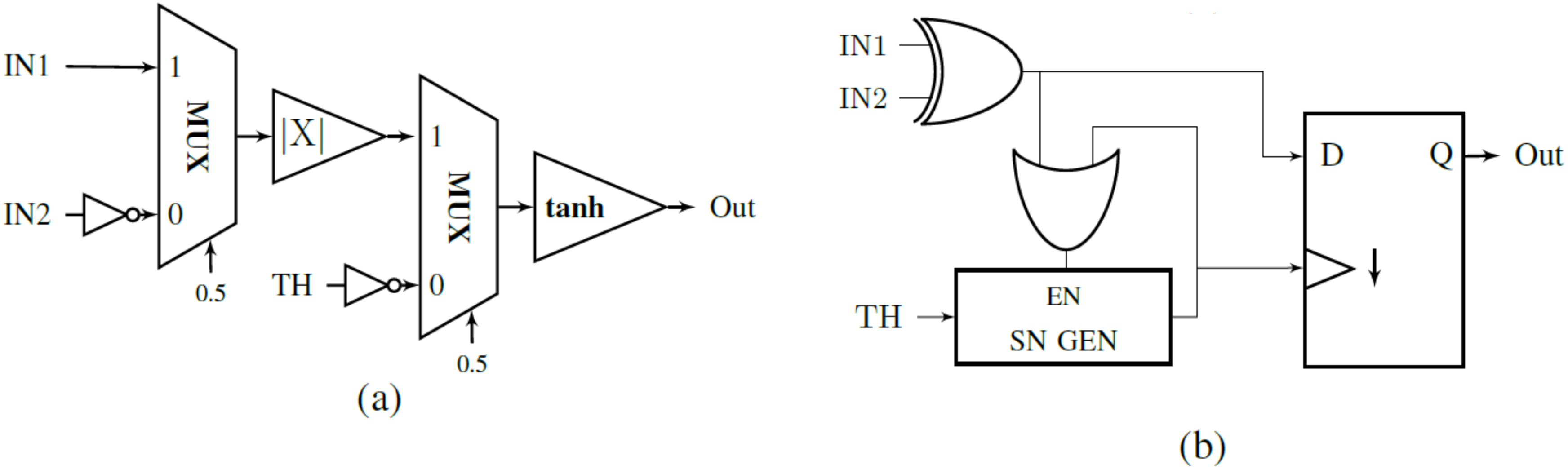
(a) (b)

(a) **both correlated and uncorrelated** inputs [Peng *et al.* TVLSI' 14];
(b) **only correlated** inputs [Alaghi *et al.* DAC' 13].

- **Circuit (a) is about 20 times more expensive than circuit (b)**

Experimental Results

- **Three image processing case studies**
  - **Frame difference-based image segmentation**



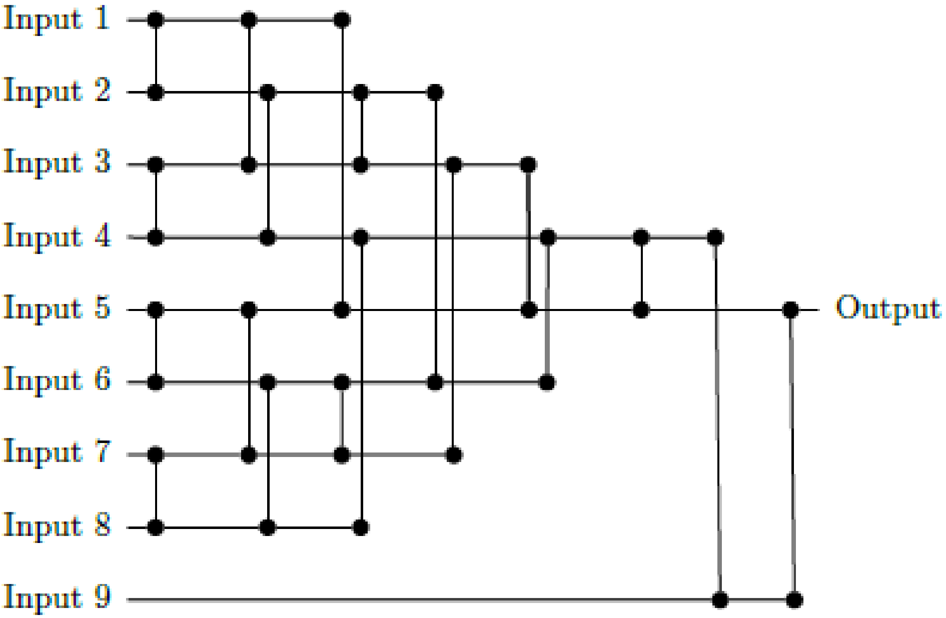
(a)

(b)

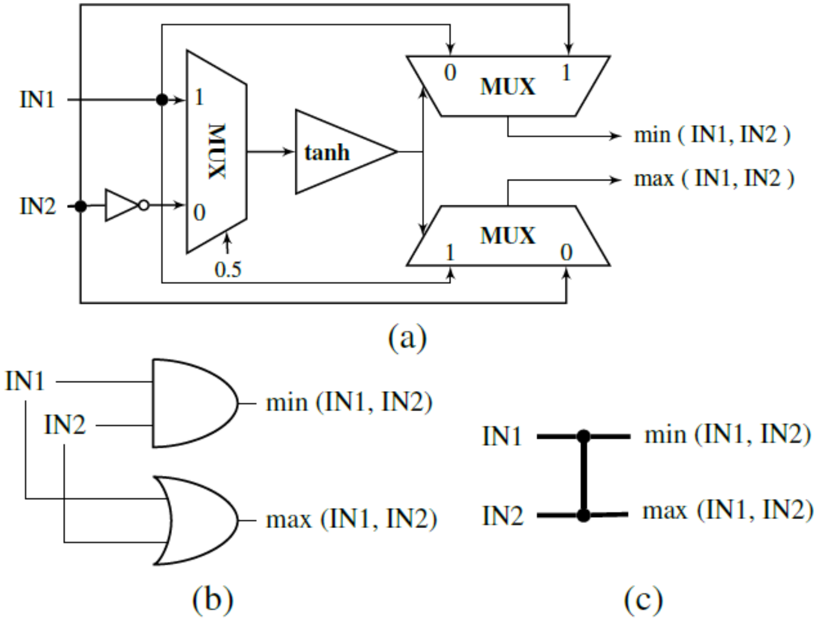
(a) both correlated and uncorrelated inputs [Peng *et al.* TVLSI' 14];
(b) Proposed low-cost implementation, only correlated inputs.

Experimental Results

- **Three image processing case studies**
  - **3x3 Median filter noise reduction based on a sorting network**



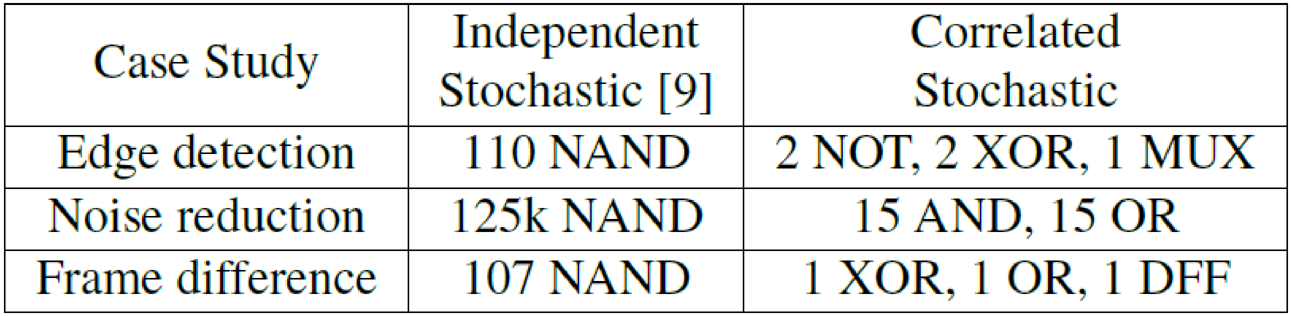
3x3 Median filter circuit
[Peng *et al.* TVLSI' 14]



Basic sorting unit
(a) Correlated and uncorrelated inputs
(b) low-cost circuit, only correlated inputs
(c) Simplified model

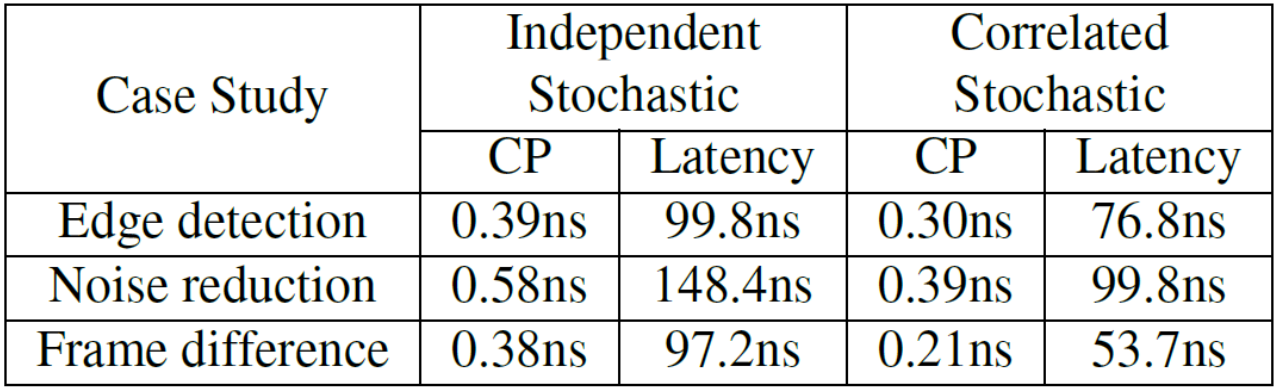
Experimental Results

- **Hardware cost comparison**



Case Study	Independent Stochastic [9]	Correlated Stochastic
Edge detection	110 NAND	2 NOT, 2 XOR, 1 MUX
Noise reduction	125k NAND	15 AND, 15 OR
Frame difference	107 NAND	1 XOR, 1 OR, 1 DFF

- **Operation time comparison: prior approach (256-bit)**
  - Synthesized with Synopsys Design Compiler, 45-nm library



Case Study	Independent Stochastic		Correlated Stochastic	
	CP	Latency	CP	Latency
Edge detection	0.39ns	99.8ns	0.30ns	76.8ns
Noise reduction	0.58ns	148.4ns	0.39ns	99.8ns
Frame difference	0.38ns	97.2ns	0.21ns	53.7ns

Experimental Results

- **Performance evaluation**
  - **Average error rate** of processing sample images

(a) Original sample images

(b) Golden outputs with no errors

Experimental Results

- **Performance evaluation**
  - **Prior approach** of stochastic number generation

	Design method	Average Error Rate for different operation time (# of clock cycles)							
		8	16	32	64	128	256	512	1024
Edge detection	Independent	27.5%	19.3%	13.1%	9.02%	6.52%	4.91%	3.70%	2.84%
	Correlated	3.57%	2.41%	1.50%	0.95%	0.62%	0.41%	0.29%	0.20%
Noise reduction	Independent	25.8%	17.3%	11.8%	8.33%	6.06%	4.43%	3.26%	2.42%
	Correlated	6.20%	3.08%	1.59%	0.82%	0.45%	0.26%	0.08%	0.04%
Frame difference	Independent	23.6%	42.0%	30.3%	14.6%	7.53%	3.91%	1.30%	0.48%
	Correlated	80.0%	1.09%	0.16%	0.16%	0.16%	0.09%	0.00%	0.00%

4.91% 4.43% 3.91%

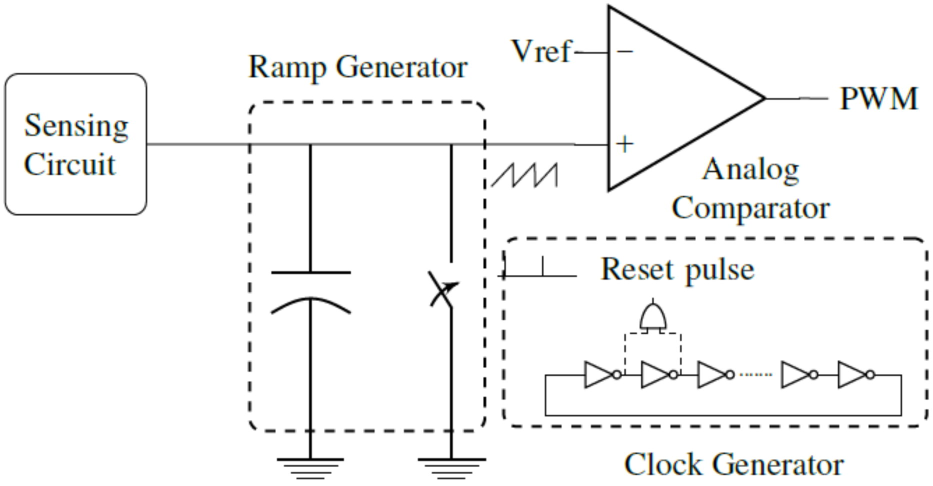
(c) Independent method outputs (256-bit streams)

0.41% 0.26% 0.09%

(d) Correlated method outputs (256-bit streams)

Experimental Results

- Performance evaluation
  - **PWM-based approach**
    - SPICE-level simulation, 45-nm technology
      - PWM signals with periods: **0.3ns, 0.5ns, 1ns, and 2ns**

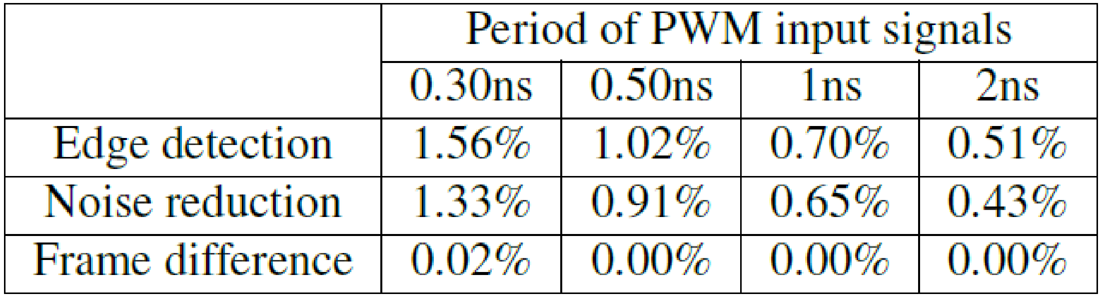


Decreasing PWM period =
Increases the error rate but
Lowers implementation cost

- **The area cost of the PWM generator (when period=2ns) is roughly as expensive as the cost of the conventional SNG with 8-bit LFSR.**

Experimental Results

- **Performance evaluation**
  - **PWM-based approach**
    - **Only one period of the PWM signal is sufficient for determining an accurate output**



	Period of PWM input signals			
	0.30ns	0.50ns	1ns	2ns
Edge detection	1.56%	1.02%	0.70%	0.51%
Noise reduction	1.33%	0.91%	0.65%	0.43%
Frame difference	0.02%	0.00%	0.00%	0.00%

0.51% 0.43% 0.00%

(e) PWM-based method outputs (period of 2ns)

PWM approach
Much faster
than prior approach

Sources of Computational Errors

- **Three primary sources of errors in performing stochastic operations on synchronized PWM signals**
  - $E_G =$ **Error in generating PWM signals**
    - Average error rate of the PWM generator used
      - 0.3ns -> 0.23% 0.5ns -> 0.12%
      - 1ns -> 0.10% 2ns -> 0.09%
  - $E_S =$ **Error due to skew between input signals**
    - Perfectly synchronized PWM signals are required
    - **On-chip variations, other noise sources affecting clock generators result in deviation from**
      - **expected period, phase shift, slew rate**

Sources of Computational Errors

- **Three primary sources of errors in performing stochastic operations on synchronized PWM signals**
  - **$E_G =$ Error in measuring the output signals**
    - Simple analog integrator
      - Measuring the fraction of time the output signal is high
    - Longer rise and fall times
    - Imperfect measurement of the high and low voltages
      - Result in inaccuracies in measuring the correct output
    - In our simulations
      - Average error rate of measurements -> **0.10%**

Conclusions

- **Reducing the hardware cost**
  - One of the main advantages of exploiting correlation
- **Two new low-cost stochastic circuits**
  - Sorting unit: 1 AND + 1 OR, Comparator: a D-type flip-flop
- **Low cost implementation for**
  - Median filter noise reduction
  - Frame difference-based image segmentation
- **Introduced synchronous analog pulses as a new representation for correlated SNs**
  - Still have area saving advantages of correlated circuits
  - Highly accurate results after only one period
    - **A solution to long latency problem of SC**

Further reading

- We discussed
  - PWM signals in correlated stochastic design
  - *"High-Speed Stochastic Circuits Using Synchronous Analog Pulses", M. Hassan Najafi and David J. Lilja, ASP-DAC 2017*

- For PWM signals in independent stochastic design
  - *"Time-Encoded Values for Highly Efficient Stochastic Circuits", M. Hassan Najafi, Shiva Jamali-Zavareh, David J. Lilja, Marc Riedel, Kia Bazargan, and Ramesh Harjani, IEEE Transactions on VLSI 2017*

Thank you

Questions?

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