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Improving LDPC Performance Via Asymmetric Sensing Level Placement on Flash Memory

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Outline

- **Background**
- Problem and Challenge
- Design
- Experiments and Evaluations
- Conclusions

Flash Memory Deployment

- NAND flash memory is widely applied, from USB to data centers.
- NAND flash memory is developed in various aspects.
- Various flash products have been used around us.

USB

eMMC

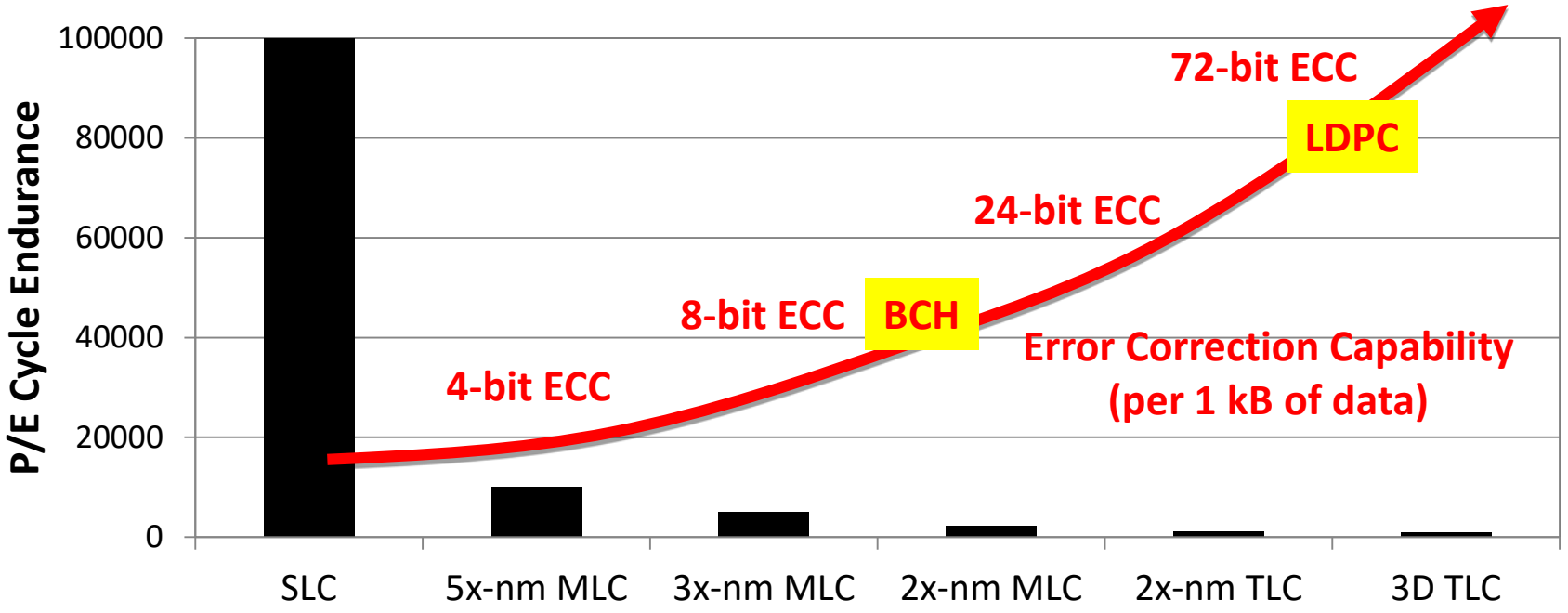
SSD

Data Center

Makers	2012	2013	1Q14	2Q14	3Q14	4Q14	2015	2016
SAMSUNG	21 nm		19 nm		16 nm		12 nm	
	3D NAND	24 L (42 nm)			32 L		48 L	
TOSHIBA SanDisk	24 nm	19 nm	A-19 nm		15 nm		10 nm	
					3D NAND		16 L	
Micron intel IM FLASH TECHNOLOGIES	20 nm		16 nm			12 nm		
						3D NAND		16 L
SK hynix	25 nm	20 nm		16 nm			12 nm	
							3D NAND	16 L

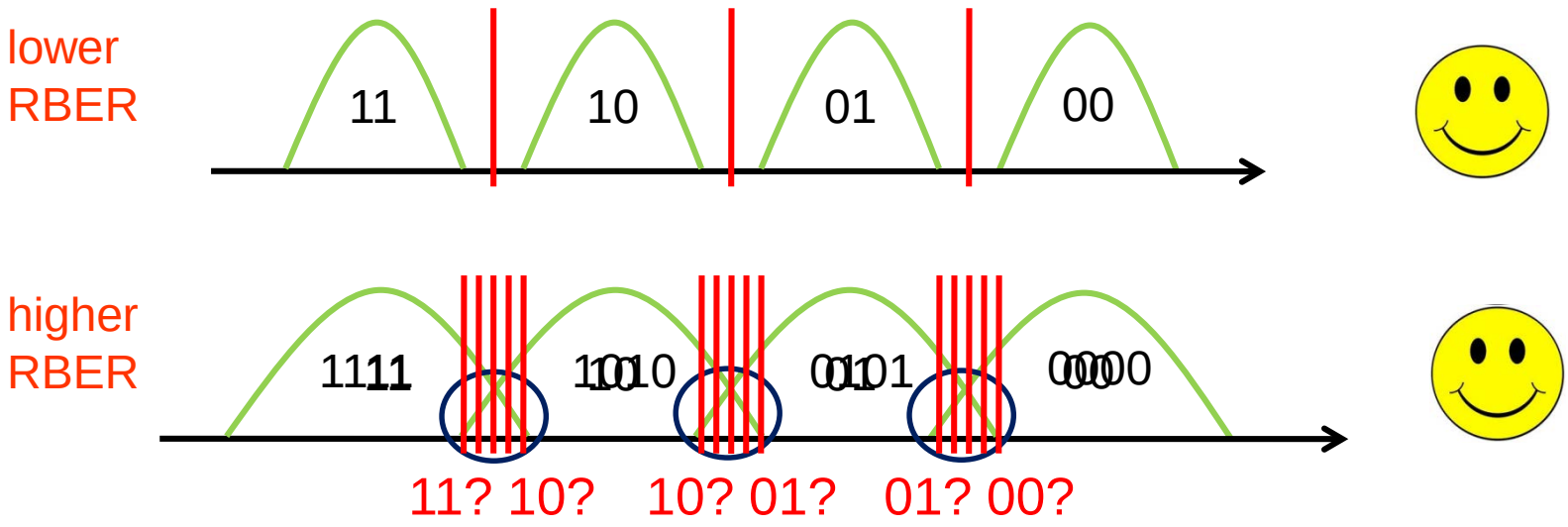
Challenges of State-of-the-art Flash

- With the development, from SLC to 3D TLC, the reliability is degraded.
- Stronger ECC has been a requirement, from BCH to the LDPC.



LDPC Codes in Flash

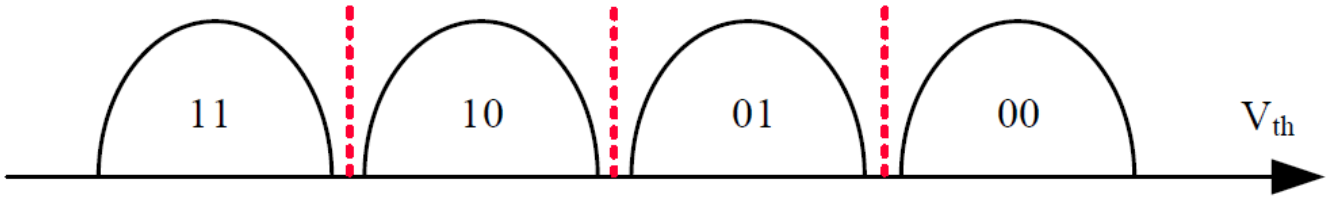
- Low-Density Parity Code (LDPC) is applied in Flash for strong ECC capability
- The decoding strength of LDPC depends on the accuracy of input information



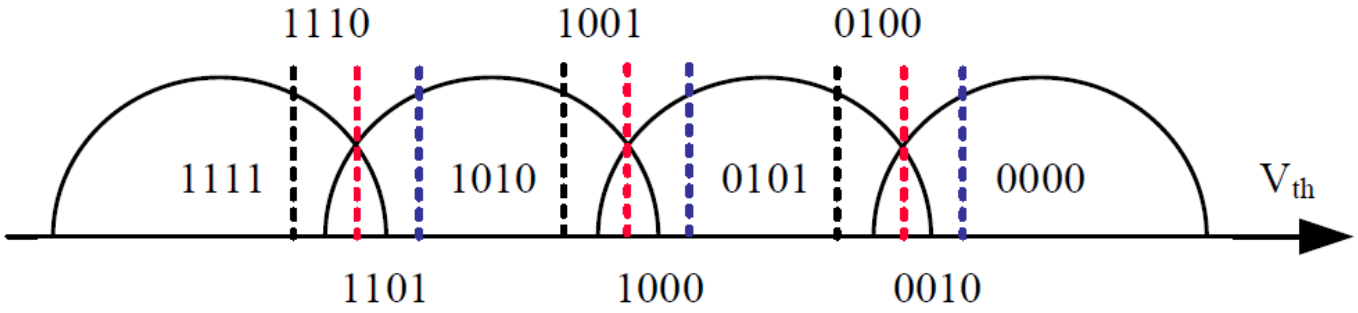
To decode data with high RBER, long read latency is needed.

Read performance is degraded using LDPC to guarantee reliability.

LDPC Codes in Flash



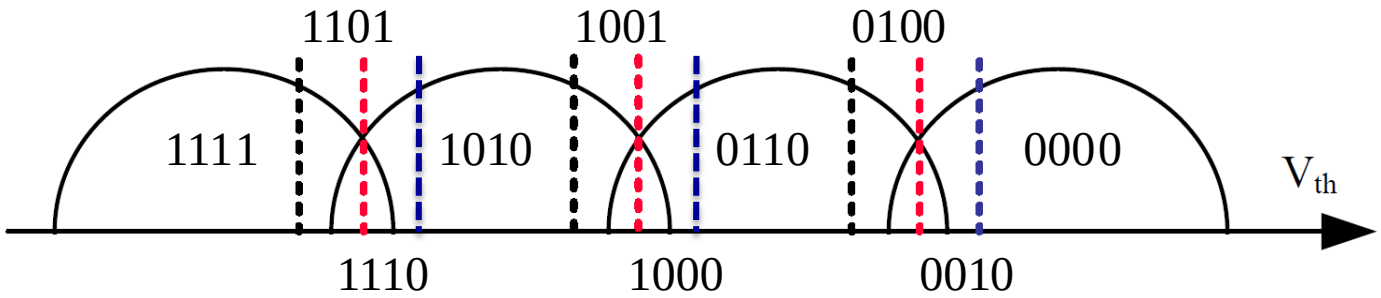
Low RBER ↔ Less Sensing Levels ↔ Low Read Latency



High RBER ↔ More Sensing Levels ↔ High Read Latency

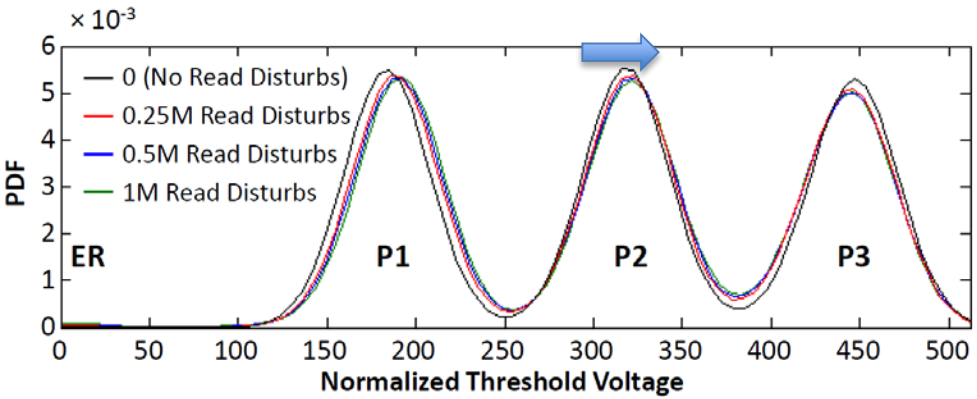
Our Goal

- Reduce LDPC sensing levels
  - As well as the information bits
- While maintaining the same error correction capability for high RBER.
- Achieved by exploiting flash reliability characteristics.

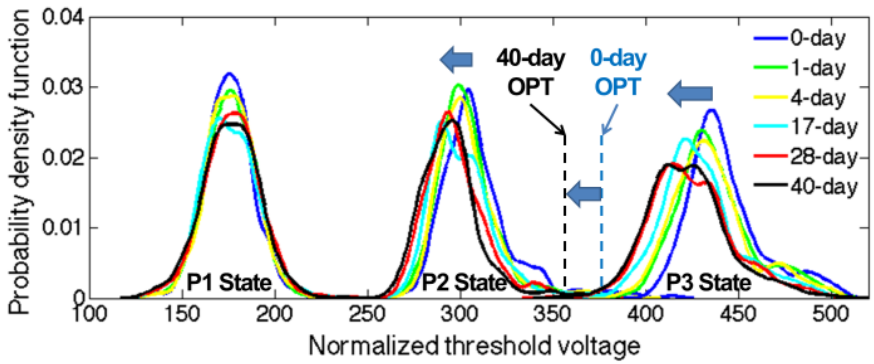


NAND Flash Reliability

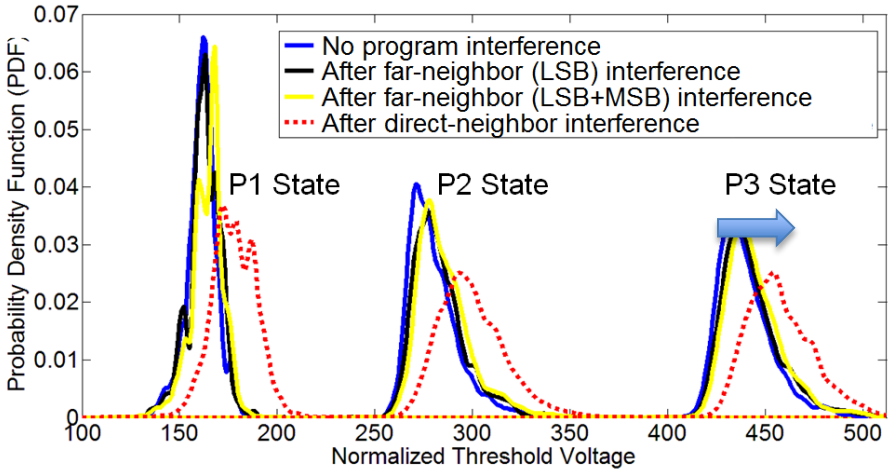
Read disturb [Cai et al. DSN 2015]



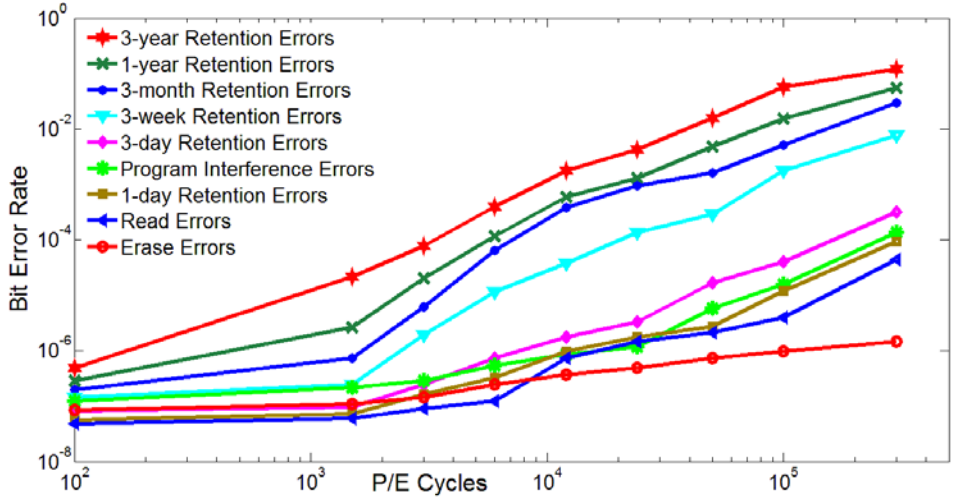
Retention error [Cai et al. HPCA 2015]



Program Interference [Cai et al. ICCD 2013]



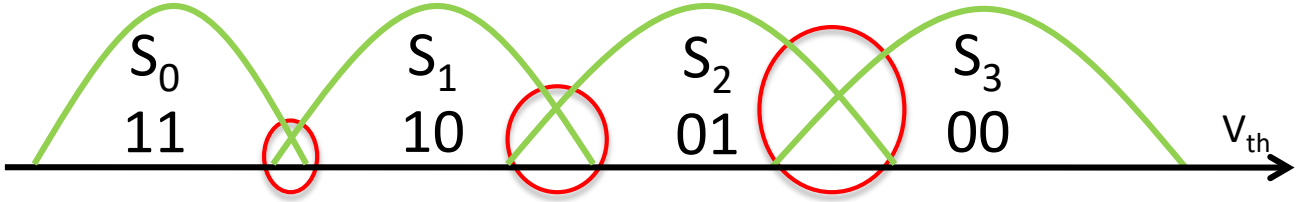
P/E Cycles [Cai et al. DATE 2012]



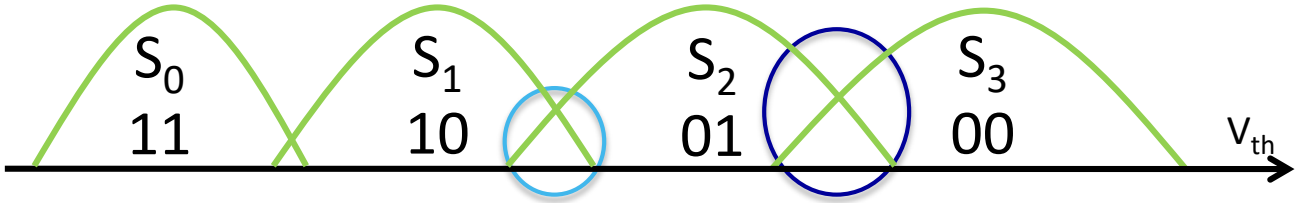
- Different types of error sources impact flash reliability.

Flash Reliability Characteristics

- Inter-State Asymmetric Errors
  - States S_2 and S_3 show the highest error rate.
  - States S_0 and S_1 show the lowest error rate.

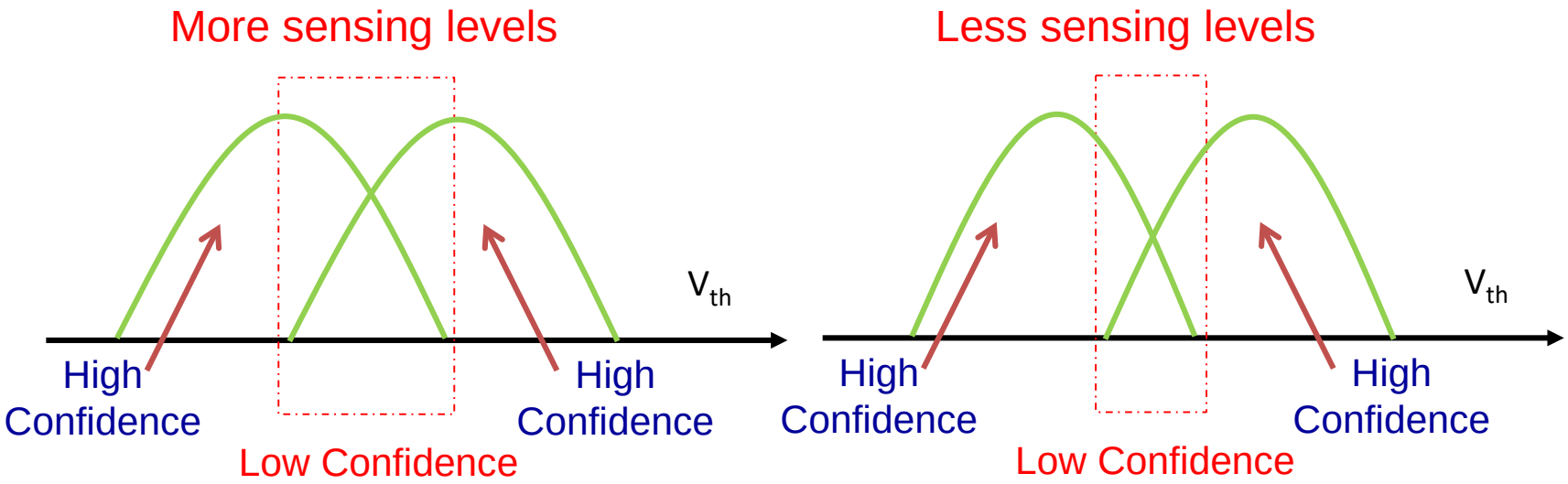


- Intra-State Asymmetric Errors
  - The voltage states mainly shift to the left with long retention time.
  - The voltage states mainly shift to the right with great P/E cycles.



Basic Idea

- Place more sensing levels in the region with high RBER
- Place less sensing levels in the region with low RBER



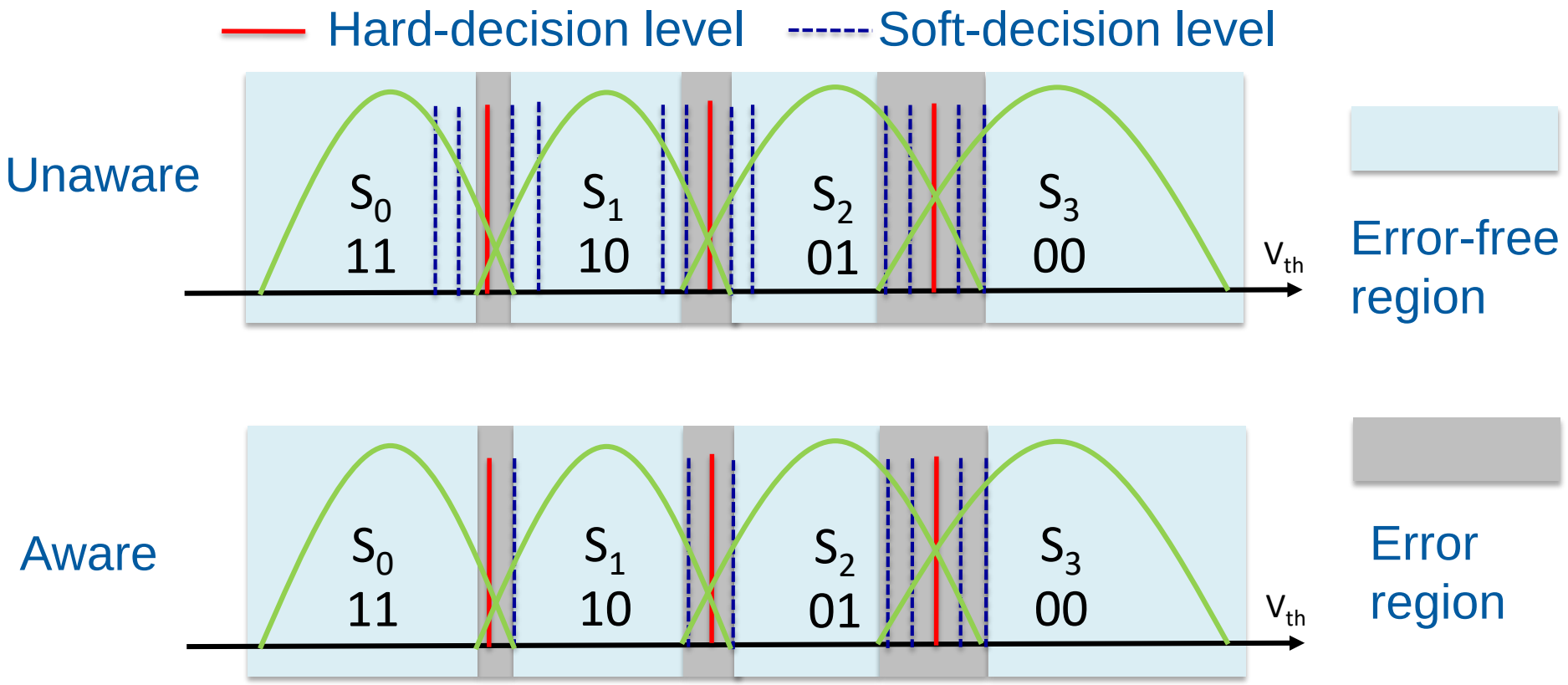
log likelihood ratio (LLR)

Sensed threshold voltage

$$\mathrm{LLR}(y_i) = \log\left(\frac{P(x_i = 0 \mid y_i)}{P(x_i = 1 \mid y_i)}\right)$$

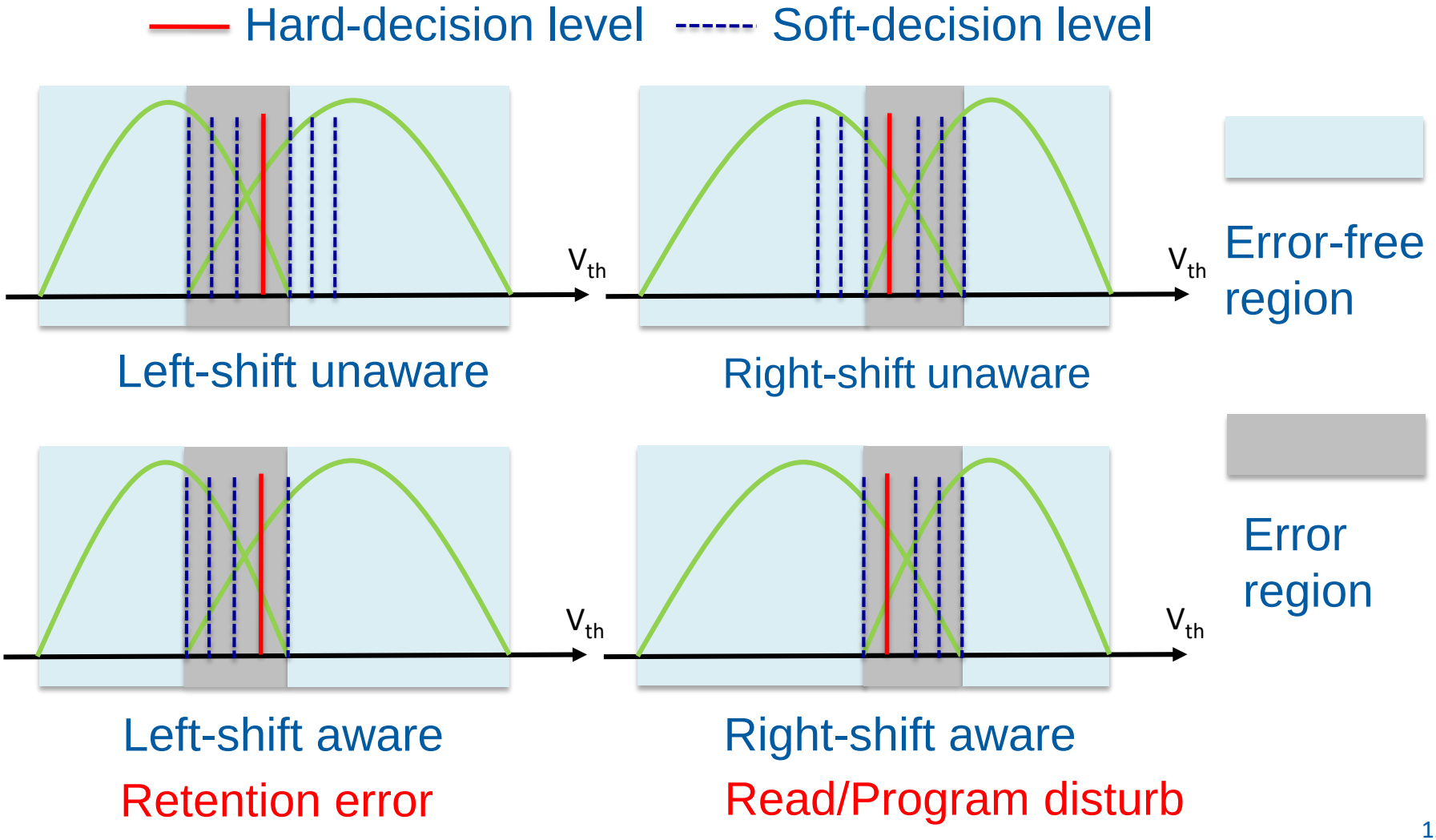
Sensing Level Placement

- Inter-state Asymmetry aware.



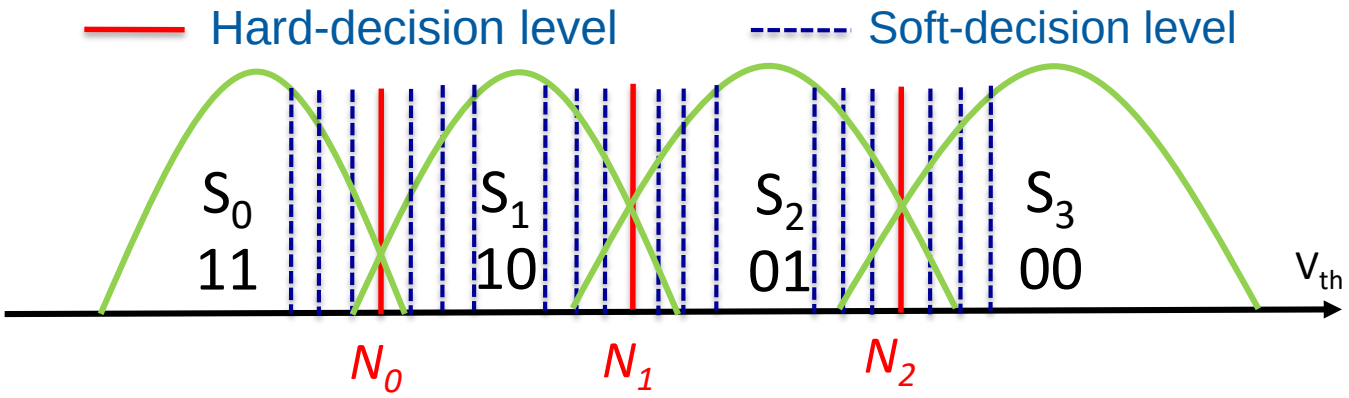
Sensing Level Placement

- Intra-state Asymmetry aware.



Implementation

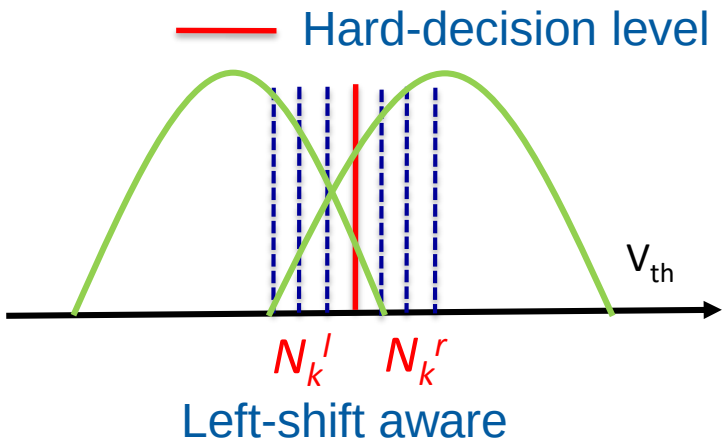
- Inter-state Asymmetry aware.
  - The region between S_2 and S_3 takes the priority for sensing level adding.

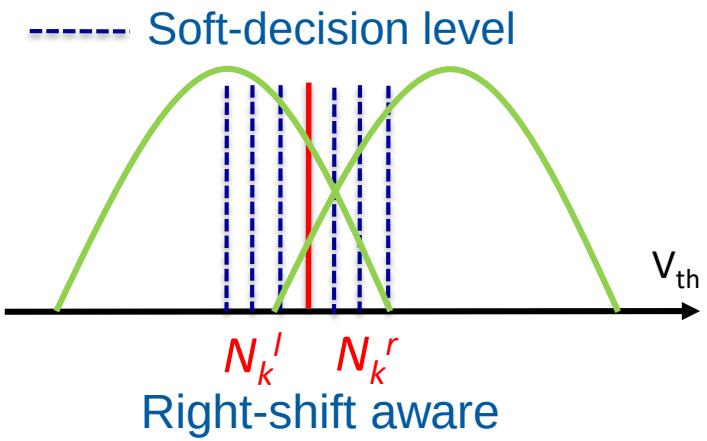


Steps	1	2	3	4	5	6	7	8	9	10	11	12
N_0	1			2			3	4		5	6	7
N_1	1	2		3	4		5	6	7			
N_2	1	2	3	4	5	6	7					

Implementation

- Intra-state Asymmetry aware.
  - Left-shift aware: left side takes priority for sensing level adding
  - Right-shift aware: right side takes priority for sensing level adding





	P/E Cycles $> T_{PE}$						P/E Cycles $\leq T_{PE}$					
Steps	1	2	3	4	5	6	1	2	3	4	5	6
N_k^l			1		2	3	1	2		3		
N_k^r	1	2		3					1		2	3

Experiments Setup

- Sensing level
  - Calculate number of sensing level bases on bit error rates [2].
  - Bit error rates are computed from the widely used flash memory error model [12].
- Read performance
  - Simulator: Disksim [15]
  - 8 channels, 8 chips per channel and 4 planes per chip
  - Default FTL, page mapping, garbage collection and wear leveling
  - 6 workloads from MSR [16]

Experiments Results

- Sensing level comparison between the proposed asymmetry aware and traditional asymmetry unaware.

Symmetric			Left-shift aware (P/E = 5K)				Right-shift aware (Retention = 1 day)			
N_{total}	bits	level placement	Retention	N_{total}	bits	level placement	P/E	N_{total}	bits	level placement
21	5	(3,3)(3,3)(3,3)	3 years	14	4	(2,0)(3,1)(3,2)	25K	15	4	(1,1)(2,3)(2,3)
18	5	(3,2)(3,2)(3,2)	1 year	12	4	(2,0)(2,1)(3,1)	24K	13	4	(1,1)(2,2)(2,2)
15	4	(2,2)(2,2)(2,2)	6 months	9	4	(1,0)(2,0)(2,1)	22K	9	4	(0,1)(1,1)(1,2)
12	4	(2,1)(2,1)(2,1)	3 months	7	3	(1,0)(1,0)(2,0)	19K	6	3	(0,0)(0,1)(1,1)
9	4	(1,1)(1,1)(1,1)	1 month	5	3	(0,0)(1,0)(1,0)	15K	5	3	(0,0)(0,1)(0,1)
6	3	(1,0)(1,0)(1,0)	1 week	4	3	(0,0)(0,0)(1,0)	10K	4	3	(0,0)(0,0)(0,1)
3	2	(0,0)(0,0)(0,0)	1 day	3	2	(0,0)(0,0)(0,0)	5K	3	2	(0,0)(0,0)(0,0)

Traditional Symmetric

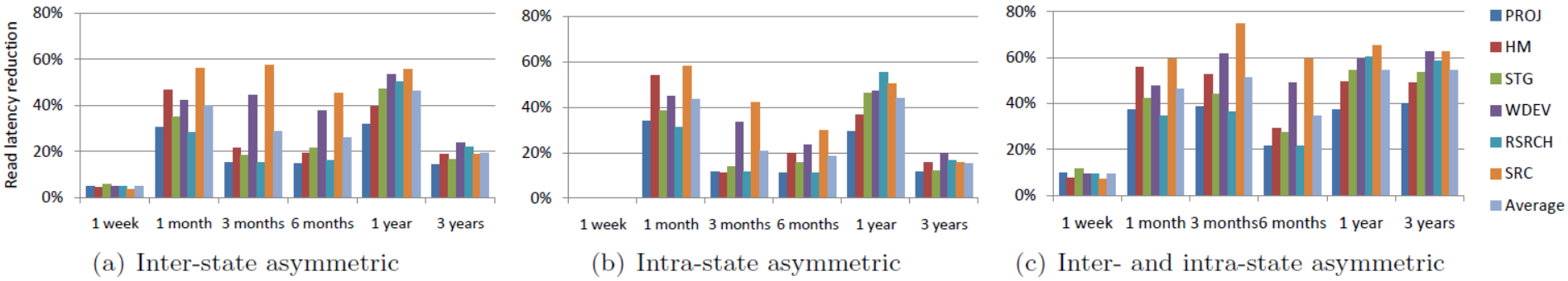
Inter- and Left Shift Aware

Inter- and Right Shift Aware

- Both sensing level and information bits reduction
- More reduction when there are more sensing levels.

Experiments Results

- Reduced read latency comparison



(a) Inter-state asymmetric (b) Intra-state asymmetric (c) Inter- and intra-state asymmetric

- The latency reduction increases with retention time.
- The reduction is degraded when retention time is 6 months, because only sensing level is reduced without information bits reduction.

Conclusions

- We studied the read performance reduction, which caused by adoption of LDPC for high RBER.
- We presented two reliability characteristics in flash memory.
- We proposed asymmetric sensing level placement approach based on the characteristics.
- Results show that the proposed approach achieves significant performance improvement with no overhead.

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Questions !

Thanks!