

Aims of the Conference:

ASP-DAC 2017 is the 22nd annual international conference on VLSI design automation in Asia and South Pacific regions, one of the most active regions of design and fabrication of silicon chips in the world. The conference aims at providing the Asian and South Pacific CAD/DA and Design community with opportunities of presenting recent advances and with forums for future directions in technologies related to Electronic Design Automation (EDA). The format of the meeting intends to cultivate and promote an instructive and productive interchange of ideas among EDA researchers/developers and system/circuit/device designers. All scientists, engineers, and students who are interested in theoretical and practical aspects of VLSI design and design automation are welcomed to ASP-DAC.

Areas of Interest:

Original papers in, but not limited to, the following areas are invited.

[1] System-Level Modeling and Design Methodology:

- 1.1. HW/SW co-design, co-simulation and co-verification
- 1.2. System-level design exploration, synthesis and optimization
- 1.3. Model- and component-based embedded system/software design
- 1.4. System-level formal verification
- 1.5. System-level modeling, simulation and validation tools/methodology

[2] Embedded System Architecture and Design:

- 2.1. Many- and multi-core SoC architecture
- 2.2. Reconfigurable and self-adaptive SoC architecture
- 2.3. IP/platform-based SoC design
- 2.4. Domain-specific architecture
- 2.5. Dependable architecture
- 2.6. On-chip memory architecture
- 2.7. Cyber physical system
- 2.8. Storage system architecture
- 2.9. Internet of things

[3] On-chip Communication and Networks-on-Chip:

- 3.1. On-chip communication network
- 3.2. Networks-on-chip
- 3.3. Interface and I/O design
- 3.4. Optical and RF on-chip communication

[4] Embedded Software:

- 4.1. Kernel, middleware and virtual machine
- 4.2. Compiler and toolchain
- 4.3. Real-time system
- 4.4. Resource allocation for heterogeneous computing platform
- 4.5. Storage software and application
- 4.6. Human-computer interface
- 4.7. System verification and analysis

[5] Device/Circuit-Level Modeling, Simulation and Verification:

- 5.1. Device/circuit/interconnect modeling and analysis
- 5.2. Device/circuit-level simulation tool and methodology
- 5.3. RTL and gate-level modeling, simulation and verification
- 5.4. Circuit-level formal verification

[6] Analog, RF and Mixed Signal:

- 6.1. Analog/mixed-signal/RF synthesis
- 6.2. Analog layout, verification and simulation techniques
- 6.3. Noise analysis
- 6.4. High-frequency electromagnetic simulation of circuit
- 6.5. Mixed-signal design consideration
- 6.6. Power-aware analog circuit/system design
- 6.7. Analog/mixed-signal modeling and simulation techniques
- 6.8. CAD for memory circuits

[7] Cross-layer Power Analysis, Low Power Design, and Thermal Management:

- 7.1. Power modeling, analysis and simulation
- 7.2. Low-power design and methodology
- 7.3. Thermal aware design
- 7.4. Architectural low-power design technique
- 7.5. Energy harvesting and battery management

[8] Logic/Behavioral/High-Level Synthesis and Optimization:

- 8.1. High-level synthesis tool and methodology
- 8.2. Combinational, sequential and asynchronous logic synthesis
- 8.3. Logic synthesis and physical design technique for FPGA
- 8.4. Technology mapping

[9] Physical Design:

- 9.1. Floorplanning, partitioning and placement
- 9.2. Interconnect planning and synthesis
- 9.3. Placement and routing optimization
- 9.4. Clock network synthesis
- 9.5. Post layout and post-silicon optimization
- 9.6. Package/PCB/3D-IC routing

[10] Design for Manufacturability and Reliability:

- 10.1. Reticule enhancement, lithography-related design and optimization
- 10.2. Resilience under manufacturing variation
- 10.3. Design for manufacturability, yield, and defect tolerance
- 10.4. Reliability, aging and soft error analysis
- 10.5. Design for reliability, aging, and robustness

[11] Timing and Signal/Power Integrity:

- 11.1. Deterministic/statistical timing and performance analysis and optimization
- 11.2. Power/ground and package modeling, analysis and optimization
- 11.3. Signal/power integrity, EM modeling and analysis
- 11.4. Extraction, TSV and package modeling
- 11.5. 2D/3D on-chip power delivery network analysis and optimization

[12] Test and Design for Testability:

- 12.1. ATPG, BIST and DFT
- 12.2. Fault modeling and simulation
- 12.3. System test and 3D IC test
- 12.4. Online test and fault tolerance
- 12.5. Memory test and repair
- 12.6. Analog and mixed-signal/RF test

[13] Security and Fault-Tolerant System:

- 13.1. Security modeling and analysis
- 13.2. Architecture, tool and methodology for secure hardware
- 13.3. Design for security and security primitive
- 13.4. Cross-layer security
- 13.5. Fault analysis, detect and tolerance

[14] Emerging Technology:

- 14.1. New transistor/device and process technology: spintronic, phase-change, single-electron etc.
- 14.2. CAD for nanotechnology, MEMS, 3D IC, quantum computing etc.

[15] Emerging Application:

- 15.1. Biomedical application
- 15.2. Big data application
- 15.3. Advanced multimedia application
- 15.4. Energy-storage/smart-grid/smart-building design and optimization
- 15.5. Datacenter optimization
- 15.6. Automotive system design and optimization
- 15.7. Electromobility

It is mandatory that at least one co-author per accepted paper registers the conference at the speaker's registration rate and attends the conference to present the work. ACM, IEEE, IEICE and IPSJ reserve the right to exclude a paper from distribution after the conference (e.g., removal from ACM Digital Library and IEEE Xplore) if the paper is not presented at the conference by the author of the paper. ASP-DAC does not allow double and/or parallel submissions of similar work to any other conferences, symposia, and journals.

Submission of Papers:

Deadline for submission: **5 PM AOE (Anywhere on earth) July 8 (Fri), 2016**
 Notification of acceptance: **Sep. 12 (Mon), 2016**
 Deadline for final version: **5 PM AOE (Anywhere on earth), Nov. 7 (Mon), 2016**

For detailed instructions for submission, please refer to the "Authors' Guide" at: <http://www.aspdac.com/>

ASP-DAC 2017 Chairs

General Chair:
Technical Program Chair:
Technical Program Vice Chairs:

Naofumi Takagi (Kyoto University, Japan)
David Z. Pan (University of Texas at Austin, USA)
Atsushi Takahashi (Tokyo Institute of Technology, Japan)
Tohru Ishihara (Kyoto University, Japan)

Panels, Special Sessions, and Tutorials: Suggestions and proposals are welcome and have to be addressed to the Conference Secretariat (aspdac2017-sec@mls.aspdac.com) no later than July 8 (Fri), 2016.

Contact: Conference Secretariat: aspdac2017-sec@mls.aspdac.com TPC Secretariat: aspdac2017-tpc@mls.aspdac.com

Call for Designs

University LSI Design Contest

ASP-DAC 2017

<http://www.aspdac.com/aspdac2017/>

January 16-19, 2017

Japan



Aims of the Contest:

As a unique feature of ASP-DAC 2017, the University LSI Design Contest will be held. The aim of the Contest is to encourage education and research on VLSI design at universities and other educational organizations. We solicit designs that fit in one or more of the following categories:

- (1) Designed, and actually implemented on chips in universities or other educational organizations during the last two years;
- (2) Designs that report actual measurements from implementations;
- (3) Innovative design prototypes.

Interesting or excellent designs selected will be honored by providing the opportunities for presentation in a special session at the conference. Award(s) will be given to a few numbers of outstanding designs, selected from those presented at the conference.

Areas of Design:

Application areas or types of circuits of the original LSI circuit designs include (but are not limited to):

- (1) Analog, RF and Mixed-Signal Circuits, (2) Digital Signal Processing, (3) Microprocessors, (4) Custom ASIC.

Methods or technology used for implementation include:

- (a) Custom ASIC and Cell-Based LSIs, (b) Gate Arrays, (c) FPGA/PLDs.

Submission of Design Descriptions:

A camera-ready summary is requested to be prepared within 2 pages including figures, tables, and references. It is strongly recommended that measured experimental results and a chip micrograph are included in the summary. Please do not submit the same paper as a regular paper.

Specification of the submission format will be available at <http://www.aspdac.com/aspdac2017/>

Deadline for summary:	5 PM AOE (Anywhere on earth) July 8 (Fri), 2016
Notification of acceptance:	Sep. 12 (Mon.), 2016
Deadline for camera-ready:	5 PM AOE (Anywhere on earth) Nov. 7 (Mon.), 2016

Review:

Submitted designs will be reviewed by the Design Contest Committee in a process similar to the review process for the technical papers. The following criteria will be applied in the selection of designs:

- (1) Reliability of design and implementation, (2) Quality of implementation, (3) Performance of the design, (4) Novelty of application, algorithm, architecture, (5) Others.

Interesting or excellent designs selected will be presented at a special session of the conference.

Presentation:

An author of each selected design will be required to make a short presentation at a special session of ASP-DAC 2017. It is mandatory that at least one co-author per accepted paper registers the conference at the speaker's registration or full-time-student registration rate. A digest of each design to be presented will be included in the conference proceedings.

Contact Email: aspdac2017-udc@mls.aspdac.com

ASP-DAC 2017 Chairs

General Chair:	Naofumi Takagi (Kyoto University, Japan)
Technical Program Chair:	David Pan (University of Texas at Austin, USA)
Technical Program Vice Chair:	Atsushi Takahashi (Tokyo Institute of Technology, Japan) Tohru Ishihara (Kyoto University, Japan)
Design Contest Co-Chairs:	Hiroyuki Ito (Tokyo Institute of Technology, Japan) Noriyuki Miura (Kobe University, Japan)

Prospective Sponsors: ACM SIGDA, IEEE CASS, IEEE CEDA, IEICE ESS, IPSJ SIGSLDM