

Call for Participation

# ASP-DAC 2017

22nd Asia and South Pacific Design Automation Conference



**Date: January 16 – 19, 2017**

**Place: Makuhari Messe International Convention Complex,  
Chiba/Tokyo, Japan**

## Aims of the Conference

ASP-DAC is the largest conference in Asia and South-Pacific regions on Electronic Design Automation (EDA) area for VLSI and systems. ASP-DAC has been started at 1995 and this ASP-DAC 2017 is 22nd conference. ASP-DAC 2017 offers you an ideal opportunity to touch the recent technologies and the future directions on the LSI design and design automation areas by technical papers and tutorials. ASP-DAC also holds Designers' Forum to make presentations about the latest designs for designers. Please do not miss ASP-DAC 2017.

## Features of ASP-DAC 2017

### ■ Keynote Speeches

1. Prof. Tim Cheng (Hong Kong Univ. of Science and Technology), Prof. John Rogers (Northwestern Univ.), Prof. Hiroto Yasuura (Kyushu Univ., Japan), "In Memory of Edward J. McCluskey: The Next Wave of Pioneering Innovations"
2. Dr. Napoleon Torres (CEA-Leti, France), "Emerging Medical Technologies for INTERFACING THE BRAIN: From Deep Brain Stimulation to Brain Computer Interfaces"
3. Dr. Steve Trimberger (Xilinx Research Labs), "All-Programmable FPGAs: More Powerful Devices Require More Powerful Tools"

### ■ Tutorials

Tutorials will be given on Monday. Attendees who register for the tutorials may select three of the six tutorials listed below.

- "Silicon Photonics for Computing Systems: Opportunities, Challenges, and Implementations,"  
organizers: Jiang Xu (Hong Kong University of Science and Technology), Yuichi Nakamura (NEC)
- "Towards Energy-Efficient Intelligence in Power-/Area-Constrained Hardware,"  
organizer: Jae-sun Seo (Arizona State University)
- "Post-Silicon Validation and Emulation-Based Validation Using Exercisers,"  
organizers: Ronny Morad (IBM Research - Haifa), Vitali Sokhin (IBM Research - Haifa)
- "Quick Start Guide of Digital PLL for Digital Designers," organizer: Kenichi Okada (Tokyo Institute of Technology)
- "The Emergence of Hardware Oriented Security and Trust," organizer: Chip-Hong Chang (Nanyang Technological University)
- "Cross-Layer Reliability Aware Design: Optimization and Dynamic Management,"  
organizer: Sheldon Tan (University of California, Riverside)

### ■ Designers' Forum

Designers' Forum is conceived as a unique program that shares the design experience and solutions of real product developments among LSI designers and EDA academia/developers. The topics discussed in this forum include IoT applications, AI technologies, automotive security, and advanced image sensing and processing technologies.

### ■ University LSI Design Contest

In University LSI Design Contest, state-of-the-art LSI designs compete on their design excellence and implementation quality. More than 20 high-quality designs all including actual silicon proof will be introduced at the short presentation and poster sessions.

### ■ Technical Sessions

There are 111 high quality papers selected from 358 submissions. We also plan the following special sessions:

- "Emerging Technologies for Biomedical Applications: Artificial Vision Systems and Brain Machine Interface",
- "Cyber-Physical Systems Security", "Neuromorphic Computing and Low-Power Image Recognition", and "When Backend Meets Frontend: Cross-Layer Design and Optimization for System Robustness"

Sponsored by: ACM SIGDA, IEEE CASS, IEEE CEDA, IEICE ESS, IPSJ SIG-SLDM

Supported by: CCB-IC

## Conference Secretariat

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