ASP-DAC 2017

22nd Asia and South Pacific Design Automation Conference

FINAL PROGRAM

Date: January 16-19, 2017
Place: Makuhari Messe
Chiba/Tokyo, Japan

Sponsored by

Supported by

JEITA

公益財団法人
電気通信普及財団

REFEC: Research Foundation for the Electrotechnology of Chubu

Chiba Convention Bureau and International Center (CCB-IC)

ASIA SOUTH PACIFIC DESIGN AUTOMATION CONFERENCE

http://www.aspdac.com/

ASP-DAC 2017

Contents

Highlights

Opening and Keynote I

Tuesday, January 17, 2017, 8:30-10:35

Keynote I: In Memory of Edward J. McCluskey: The Next Wave of Pioneering Innovations

Organizers/Chairs:

Subhasish Mitra (Stanford University), Deming Chen (University of Illinois at Urbana-Champaign)

This special plenary session will celebrate Prof. McCluskey (who passed away in 2016) through three keynote speeches by world-renowned scholars on the next wave of pioneering innovations, starting with a memorial speech by Prof. Jacob Abraham of University of Texas at Austin.

Keynote I-1: **K.-T. Tim Cheng** **(Hong Kong University of Science and Technology)** "Heterogeneous Integration of X-tronics: Design Automation and Education"

Keynote I-2: **John Rogers** **(Northwestern University)** "Electronics for the Human Body"

Keynote I-3: **Hiroto Yasuura** **(Kyushu University)** "Design of Society: Beyond Digital System Design"

Keynote II

Wednesday, January 18, 2017, 9:00-9:50

Napoleon Torres-Martinez **(CEA LETI)**

"Emerging Medical Technologies for Interfacing the Brain: From Deep Brain Stimulation to Brain Computer Interfaces"

Keynote III

Thursday, January 19, 2017, 9:00-9:50

Steve Trimberger **(Xilinx Research Labs)**

"All-Programmable FPGAs: More Powerful Devices Require More Powerful Tools"

Special Sessions

1S: (Presentation + Poster Discussion) University Design Contest

Tuesday, January 17, 2017, 11:05-13:50

2S: (Invited Talks) Neuromorphic Computing and Low-Power Image Recognition

Tuesday, January 17, 2017, 13:50-15:30

3S: (Invited Talks) Let's Secure the Physics of Cyber-Physical Systems

Tuesday, January 17, 2017, 15:50-17:30

4S: (Invited Talks) Emerging Technologies for Biomedical Applications: Artificial Vision Systems and Brain Machine Interface

Wednesday, January 18, 2017, 10:15-12:20

7S: (Invited Talks) When Backend Meets Frontend: Cross-Layer Design & Optimization for System Robustness

Thursday, January 19, 2017, 10:15-12:20

Designers' Forum

5S: (Oral Session) Advanced Devices and Networks for IoT Applications

Wednesday, January 18, 2017, 13:50-15:30

6S: (Panel Discussion) What is future AI we will create? – "Doraemon" or "Terminator" ? –

Wednesday, January 18, 2017, 15:50-17:30

8S: (Oral Session) Advanced Automotive Security

Thursday, January 19, 2017, 13:50-15:30

9S: (Oral Session) Advanced Image Sensing and Processing

Thursday, January 19, 2017, 15:50-17:30

Tutorials

ASP-DAC 2017 offers attendees a set of two-hour intense introductions to specific topics. Each tutorial will be presented twice a day to allow attendees to cover multiple topics. If you register for tutorials, you have the option to select three out of the six topics.

Tutorial-1: Silicon Photonics for Computing Systems: Opportunities, Challenges, and Implementations

Monday, January 16, 2017, 9:30-11:30, 12:45-14:45

Organizers:

Jiang Xu (Hong Kong University of Science and Technology)

Yuichi Nakamura (NEC)

Speakers:

Jiang Xu (Hong Kong University of Science and Technology)

Shigeru Nakamura (NEC)

Tutorial-2: Towards Energy-Efficient Intelligence in Power-/Area-Constrained Hardware

Monday, January 16, 2017, 9:30-11:30, 12:45-14:45

Organizer:

Jae-sun Seo (Arizona State Univ.)

Speakers:

Zhengya Zhang (U. Michigan, Ann Arbor)

Mingoo Seok (Columbia Univ.)

Jae-sun Seo (Arizona State Univ.)

Tutorial-3: Post-Silicon Validation and Emulation-Based Validation Using Exercisers

Monday, January 16, 2017, 9:30-11:30, 15:15-17:15

Organizers:

Ronny Morad (IBM Research - Haifa)

Vitali Sokhin (IBM Research - Haifa)

Speakers:

Ronny Morad (IBM Research - Haifa)

Vitali Sokhin (IBM Research - Haifa)

Tutorial-4: Quick Start Guide of Digital PLL for Digital Designers

Monday, January 16, 2017, 9:30-11:30, 15:15-17:15

Organizer:

Kenichi Okada (Tokyo Institute of Technology)

Speakers:

Kenichi Okada (Tokyo Institute of Technology)

Salvatore Levantino (Politecnico di Milano)

Tutorial-5: The Emergence of Hardware Oriented Security and Trust

Monday, January 16, 2017, 12:45-14:45, 15:15-17:15

Organizer:

Chip-Hong Chang (Nanyang Technological Univ.)

Speakers:

Chip-Hong Chang (Nanyang Technological Univ.)

Yier Jin (Univ. of Central Florida)

Tutorial-6: Cross-Layer Reliability Aware Design, Optimization and Dynamic Management

Monday, January 16, 2017, 12:45-14:45, 15:15-17:15

Organizer:

Sheldon Tan (UC Riverside)

Speakers:

Sheldon Tan (UC Riverside)

Mehdi Tahoori (Karlsruhe Inst. Tech.)

Hai-Bao Chen (Shanghai Jiao Tong Univ.)

Welcome to ASP-DAC 2017

On behalf of the Organizing Committee, I would like to invite all of the engineers on the LSI design and design automation areas to the 22nd Asia and South Pacific Design Automation Conference (ASP-DAC2017). ASP-DAC2017 will be held from January 16th (Mon.) to January 19th (Thu.), 2017 at Makuhari Messe, Chiba, Japan.

ASP-DAC is a high-quality and premium conference on Electronic Design Automation (EDA) area like other sister conferences such as Design Automation Conference (DAC), Design, Automation & Test in Europe (DATE), and International Conference on Computer Aided Design (ICCAD). ASP-DAC started in 1995 and has continuously offered opportunity to know the recent advanced technologies on LSI design and design automation areas, and to communicate each other for researchers and designers around Asia and South Pacific regions.

The conference site is Makuhari Messe, which is one of the biggest international convention complexes in Japan and a memorable place where the first ASP-DAC was held in 1995. Hundreds of companies are accumulated around the complex, and big events on various industrial fields including semiconductor and electronics are held every year. As Makuhari Messe is close to Tokyo, about 30 minutes by train, you can easily access the venue from Narita (New Tokyo) or Haneda (Tokyo) international airport. Joining the conference and participating in technological discussions, you can also enjoy many attractions in Tokyo area, such as Tokyo Disneyland and Disneysea, the world-highest TV tower called Tokyo Sky Tree, Akihabara, etc.

ASP-DAC2017 received 358 submissions from all over the world. Based on rigorous and thorough reviews and a full-day face-to-face meeting by the Technical Program Committee in August at Hong Kong, 111 papers have been accepted and 27 technical sessions have been organized. 4 Special Sessions have also been organized based on invited talks by the Technical Program Committee.

We have arranged three Keynote sessions at the beginning of each day to know the future directions of this area. The first keynote is a joint keynote celebrating Prof. McCluskey (who passed away in February 2016) through three speeches by world-renowned scholars on the next wave of pioneering innovations. The first speech is 'Heterogeneous integration of X-tronics: Design automation and education' by Prof. Tim Cheng of Hong Kong University of Science and Technology. The second one is 'Electronics for the Human Body' by Prof. John Rogers of Northwestern University. And the last one is 'Design of society: Beyond digital system design' by Prof. Hiroto Yasuura of Kyushu University, Japan. The second keynote address is 'Emerging medical technologies for interfacing the brain: From deep brain stimulation to brain computer interfaces' by Dr. Napoleon Torres-Martinez of CEA LETI, France. The third keynote address is 'All-programmable FPGAs: More powerful devices require more powerful tools' by Dr. Steve Trimberger of Xilinx Research Labs.

The Designers' Forum is a unique program that will share design experience and solutions of actual product designs of the industries. The topics discussed in this forum include IoT applications, AI technologies, automotive security, and advanced image sensing and processing technologies.

The University Design Contest is also an important annual event of ASP-DAC where more than 20 high-quality designs all including actual silicon proof were selected for presentation at Tuesday, January 17.

Six tutorials have been arranged on Monday, January 16. Each tutorial has 2 hour presentation, and will be held 2 times. Registrants can take any 3 of 6 tutorials with the reduced tutorial fee depending on their interests and can obtain wider perspective on the recent hot topics.

ASP-DAC2017 offers you an ideal opportunity to touch the recent technologies and the future directions on the LSI design and design automation areas. You will be able to meet and discuss with a lot of researchers and designers on this area, so please do not miss ASP-DAC2017. Finally, we would like to express our sincere appreciation to sponsors and supporters.

Naofumi Takagi (Kyoto University)
General Chair, ASP-DAC 2017

Message from the Technical Program Committee


David Z. Pan


Atsushi Takahashi


Tohru Ishihara

On behalf of the Technical Program Committee of the 22nd Asia and South Pacific Design Automation Conference (ASP-DAC) 2017, we would like to welcome all of you to the conference scheduled from January 16 to 19, 2017 in Chiba/Tokyo, Japan.

This year, ASP-DAC received 358 paper submissions from 25 countries/regions, with the majority of them from Asia, North America, and Europe. The challenge of selecting which papers to accept was significant. We organized the Technical Program Committee (TPC) with 107 professionals who are leading experts on EDA, IC design, system design, hardware security, and emerging technologies/applications. These TPC members are from 13 countries/regions, and organized into 15 subcommittees. The review process ensured fairness through a rigorous double-blind review process to resolve any possible conflict of interest. The full-day TPC meeting was held at the Hong Kong Polytechnic University (HKPU) on August 29, 2016, with the EDA Workshop afterwards. Almost all TPC members physically attended the TPC meeting, and some joined via teleconferencing due to personal emergency. Out of the 358 submissions, 111 high-quality regular papers were selected, which corresponds to a very competitive acceptance rate of 31%.

The complete conference program consists of regular papers, keynote speeches, as well as special and design contest sessions. They are compiled into a three-day, four parallel-session program. The keynotes are held every morning to kick off the technical sessions. The regular papers are presented in 27 sessions on tracks A, B, and C. The special and design sessions are allocated on track S.

Each Subcommittee was eligible to nominate one best paper candidate. The Best Paper Award (BPA) Committee which consists of 17 members selected 11 best paper candidates, which further went through a rigorous evaluation process. Finally two best paper award winners were selected.

The fruitful technical program of the ASP-DAC 2017 was not possible without hard work of all the authors, reviewers, and TPC members. Special thanks go to TPC Secretaries for their excellent support. Thanks to the generous financial support from HKPU, Cadence, Huawei, and IEEE/CEDA, the TPC meeting provided high-quality supplements in both academic and social programs. Finally, we would also like to thank the Organizing Committee for their extraordinary services.

We hope you enjoy the ASP-DAC 2017 technical program.

David Z. Pan (University of Texas at Austin)
TPC Chair, ASP-DAC 2017

Atsushi Takahashi (Tokyo Institute of Technology)
TPC Vice Chair

Tohru Ishihara (Kyoto University)
TPC Vice Chair

Sponsorship

Sponsored by:

ACM/SIGDA
http://www.sigda.org/

IEEE Circuits and Systems Society
http://www.ieee-cas.org/

IEEE Council on Electronic Design Automation
http://ieee-ceda.org/

IEICE ESS (Institute of Electronics, Information and Communication Engineers – Engineering Sciences Society)
http://www.ieice.org/eng/

IPSJ SIGSLDM (Information Processing Society of Japan – SIG System and LSI Design Methodology)
http://www.ipsj.or.jp/english/

Supported by:

JEITA (Japan Electronics and Information Technology Industries Association)
http://www.jeita.or.jp/english/

The Telecommunications Advancement Foundation
http://www.taf.or.jp/

SCAT (Support Center for Advanced Telecommunications Technology Research, Foundation)
http://www.scat.or.jp/english/

REFEC (Research Foundation for the Electrotechnology of Chubu)
http://www006.upp.so-net.ne.jp/refec/WELCOME.HTM

Chiba Convention Bureau and International Center (CCB-IC)
http://www.ccb.or.jp/e/

Special Support:

Cadence Design Systems, Inc.
http://www.cadence.co.jp/

Industrial Partner:

Fujitsu Limited
http://www.fujitsu.com/

NEC Corporation
http://www.nec.com/

Socionext Inc.
http://www.socionext.com/

Gold Support:

Baum Co.

Easy-Logic Technology Ltd.
http://www.easylogic.hk/

Keysight Technologies

OneSpin Solutions
http://www.onespin.com/

Silver Support:

Springer

Organizing Committee

General Chair	**Naofumi Takagi** (Kyoto University)
Past Chair	**Rui Paulo da Silva Martins** (University of Macau)
GC Advisor	**Nozomu Togawa** (Waseda University)
GC Secretaries	**Kazutoshi Kobayashi** (Kyoto Institute of Technology) **Kazuyoshi Takagi** (Kyoto University) **Kenshu Seto** (Tokyo City University)
Technical Program Chair	**David Z. Pan** (University of Texas at Austin)
TPC Vice Chairs	**Atsushi Takahashi** (Tokyo Institute of Technology) **Tohru Ishihara** (Kyoto University)
TPC Secretaries	**Zili Shao** (Hong Kong Polytechnic University, Hong Kong) **Jason Xue** (City University of Hong Kong, Hong Kong) **Bei Yu** (The Chinese University of Hong Kong, Hong Kong) **Wei Zhang** (Hong Kong University of Science and Technology, Hong Kong) **Shimpei Sato** (Tokyo Institute of Technology, Japan)
Tutorial Co-Chairs	**Makoto Ikeda** (University of Tokyo) **Takashi Sato** (Kyoto University)
Design Contest Co-Chairs	**Noriyuki Miura** (Kobe University) **Hiroyuki Ito** (Tokyo Institute of Technology)
Designer's Forum Co-Chairs	**Masaitsu Nakajima** (socionext) **Koji Inoue** (Kyushu University)
Finance Co-Chairs	**Hiroyuki Tomiyama** (Ritsumeikan University) **Hideki Takase** (Kyoto University)
Publication Co-Chairs	**Shinobu Nagayama** (Hiroshima City University) **Masashi Imai** (Hirosaki University)
Publicity Co-Chairs	**Taeko Matsunaga** (Nippon Bunri University) **Yasuhiro Takashima** (University of Kitakyushu) **Kotaro Shimamura** (Hitachi) **Izumi Nitta** (Fujitsu Laboratories)
Web Publicity Co-Chairs	**Yuko Hara-Azumi** (Tokyo Institute of Technology) **Takeshi Matsumoto** (National Institute of Technology, Ishikawa College)
Promotion Co-Chairs	**Yuichi Nakamura** (NEC) **Takashi Takenaka** (NEC)
ASP-DAC Liaison at SIGDA Student Research Forum	**Yukihide Kohira** (The University of Aizu)
JEITA EDA-TC Liaison	**Kazutoshi Wakabayashi** (NEC)
Secretariat	**Yoshinori Ishizaki** (Japan Electronics Show Association) **Mieko Mori** (Japan Electronics Show Association) **Kohei Torikai** (Japan Electronics Show Association) **Kayoko Oda** (Japan Electronics Show Association)

Technical Program Committee

Technical Program Chair

David Z. Pan (University of Texas at Austin, USA)

Technical Program Vice Chairs

Atsushi Takahashi (Tokyo Institute of Technology, Japan)
Tohru Ishihara (Kyoto University, Japan)

Secretaries

Zili Shao (Hong Kong Polytechnic University, Hong Kong)
Jason Xue (City University of Hong Kong, Hong Kong)
Bei Yu (The Chinese University of Hong Kong, Hong Kong)
Wei Zhang (Hong Kong University of Science and Technology, Hong Kong)
Shimpei Sato (Tokyo Institute of Technology, Japan)

Subcommittees and Subcommittee Chairs (* : Subcommittee Chairs)

[1] System-Level Modeling and Design Methodology

* **Soonhoi Ha** (Seoul National University, Korea)
Preeti Ranjan Panda (IIT Delhi, India)
Liang Shi (Chongqing University, China)
Qi Zhu (UC Riverside, USA)
Ing-Jer Huang (National Sun Yat-sen University, Taiwan)
Hoeseok Yang (Ajou University, Korea)
Jing-Jia Liou (National Tsing Hua University, Taiwan)
Sungchan Kim (Chonbuk National University, Korea)
Masashi Tawada (Waseda University, Japan)

[2] Embedded System Architecture and Design

* **Wei Zhang** (Hong Kong University of Science and Technology, Hong Kong)
Hyung Gyu Lee (Daegu University, Korea)
Weichen Liu (Chongqing University, China)
Lars Bauer (Karlsruhe Institute of Technology, Germany)
Chun-Yi Lee (National Tsing Hua University, Taiwan)
Yongpan Liu (Tsinghua University, China)
Ji-Hoon Kim (Seoul National University of Science and Technology, Korea)
Wujie Wen (Florida International University, USA)
Yaoyao Ye (Shanghai Jiao Tong University, China)
Eric Liang (Peking University, China)
Ha Yajun (Institute for Infocomm Research, Astar, Singapore)
Chengmo Yang (University of Delaware, USA)
Yuan Xie (UC Santa Barbara, USA)

[3] On-chip Communication and Networks-on-Chip

* **Mehdi Tahoori** (Karlsruhe Institute of Technology, Germany)
Yoshinori Takeuchi (Osaka University, Japan)
Koushik Chakraborty (Utah State University, USA)
Yi-Jung Chen (National Tsing Hua University, Taiwan)
Romain Lemaire (CEA-LETI, France)

[4] Embedded Software

* **Zili Shao** (Hong Kong Polytechnic University, Hong Kong)
Sungjoo Yoo (Seoul National University, Korea)
Jingtong Hu (Oklahoma State University, USA)
Chung-Ta King (National Tsing Hua University, Taiwan)
Jalil Boukhobza (University of Western Brittany, France)
Yuko Hara-Azumi (Tokyo Institute of Technology, Japan)

[5] Device/Circuit-Level Modeling, Simulation and Verification

* **Jaijeet Roychowdhury** (UC Berkeley, USA)
Rajit Manohar (Cornell University, USA)
Soumyajit Mandal (Case Western Reserve University,USA)
Alper Demir (Koc University, Turkey)
Jason Verley (Sandia National Laboratory, USA)

[6] Analog, RF and Mixed Signal

* **Ibrahim (Abe) Elfadel** (Masdar Institute of Science and Technology, United Arab Emirates)
Quan Chen (University of Hong Kong, Hong Kong)
Zhuo Feng (Michigan Technical University, USA)
Zuochang Ye (Tsinghua University, China)
Markus Olbrich (University of Hannover, Germany)

[7] Cross-layer Power Analysis, Low Power Design, and Thermal Management

* **Chia-Lin Yang** (National Taiwan University, Taiwan)
Donghwa Shin (Yeungnam University, Korea)
Koji Inoue (Kyushu University, Japan)
Jae-Joon Kim (Pohang University of Science and Technology, Korea)
Tsung-Te Liu (National Taiwan University, Taiwan)
Dongrui Fan (Chinese Academy of Sciences, China)
Guihai Yan (Chinese Academy of Sciences, China)
Yu Wang (Tsinghua University, China)
Zhuo Cheng (Zhejiang University, China)
Masaaki Kondo (University of Tokyo, Japan)
Li Shang (University of Colorado, USA)

[8] Logic/Behavioral/High-Level Synthesis and Optimization

* **Zhiru Zhang** (Cornell University, USA)
Anupam Chattopadhyay (Nanyang Technological University, Singapore)
Fabrizio Ferrandi (Politecnico di Milano, Italy)
Benjamin Carrion Schafer (Hong Kong Polytechnic University, Hong Kong)
Seiya Shibata (NEC Corp., Japan)
Shouyi Yin (Tsinghua University, China)

[9] Physical Design

* **Taewhan Kim** (Seoul National University, Korea)
Seokhyeong Kang (Ulsan National Institute of Science and Technology, Korea)
Hyung-Ock Kim (Samsung Electronics, Korea)
Tung-Chieh Chen (Synopsys, Taiwan)
Yasuhiro Takashima (University of Kitakyushu, Japan)
Wai Kei Mak (National Tsing Hua University, Taiwan)
Sheqin Dong (Tsinghua University, China)
Masato Inagi (Hiroshima City University, Japan)

[10] Design for Manufacturability and Reliability

* **Xuan Zeng** (Fudan University, China)
Yukihida Kohira (Aizu University, Japan)
Evangeline Young (The Chinese University of Hong Kong, Hong Kong)
Ting-Chi Wang (National Tsing Hua University, Taiwan)
Hai Zhou (Northwestern University, USA)
Shao-Yun Fang (National Taiwan University, Taiwan)
Tetsuaki Matsunawa (Toshiba, Japan)

[11] Timing and Signal/Power Integrity

* **Masanori Hashimoto** (Osaka University, Japan)
Bong Hyun Lee (Samsung, Korea)
Guoyong Shi (Shanghai Jiao Tong University, China)
Takashi Sato (Kyoto University, Japan)
Ngai Wong (University of Hong Kong, Hong Kong)

[12] Test and Design for Testability

* **Jin-Fu Li** (National Central University, Taiwan)
Satoshi Ohtake (Oita University, Japan)
Hua-Wei Li (Chinese Academy of Sciences, China)
Huaguo Liang (Hefei University of Technology, China)
Kohei Miyase (Kyushu Institute of Technology, Japan)

[13] Security and Fault-Tolerant System

* **Yier Jin** (University of Central Florida, USA)
Jakub Szefer (Yale University, USA)
Qiang Xu (The Chinese University of Hong Kong, Hong Kong)
Ahmad-Reza Sadeghi (TU-Darmstadt, Germany)
Chip Hong Chang (Nanyang Technological University, Korea)
Fareena Saqib (Florida Institute of Technology, USA)
Xiaoxiao Wang (Beihang University, China)
Kang Li (Cyber Immunity Inc., USA)

[14] Emerging Technology

* **Yiran Chen** (University of Pittsburgh, USA)
Shigeru Yamashita (Ritsumeikan University, Japan)
Duo Liu (Chongqing University, China)
Jongeun Lee (Ulsan National Institute of Science and Technology, Korea)
Danghui Wang (Northwestern Polytechnical University, USA)
Weisheng Zhao (Beihang University, China)
Yuan-Hao Chang (Academia Sinica, Taiwan)

[15] Emerging Application

* **Tohru Ishihara** (Kyoto University, Japan)
Yasushi Sugama (Fujitsu, Japan)
Younghyun Kim (University of Wisconsin-Madison, USA)
Xiaojun Guo (Shanghai Jiao Tong University, China)
Ittetsu Taniguchi (Ritsumeikan University, Japan)
Hailong Yao (Tsinghua University, China)
Juinn-Dar Huang (National Chiao Tung University, Taiwan)

University LSI Design Contest Committee

Co-Chairs **Noriyuki Miura** (Kobe University, Japan)
Hiroyuki Ito (Tokyo Institute of Technology, Japan)

Members **Po-Hung Chen** (National Chiao-Tung University, Taiwan)
Louis Alarcon (University of the Philippines Diliman, Philippines)
Hiroaki Hoshino (Toshiba, Japan)
Mitsuru Tomono (Fujitsu, Japan)
Kousuke Miyaji (Shinshu University, Japan)
Akira Tsuchiya (Kyoto University, Japan)
Mikyu Je (KAIST, Korea)
Ikjoon Chang (Kyunghee University, Korea)

Designers' Forum Committee

Co-Chairs **Masaitsu Nakajima** (socionext, Japan)
Koji Inoue (Kyushu Univ., Japan)

Members **Hiroe Iwasaki** (NTT, japan)
Shinichi Shibahara (Renesas Electronics, Japan)
Masaru Kokubo (Hitachi, Japan)
Koichiro Yamashita (Fujitsu Laboratories, Japan)
Akihiko Inoue (Panasonic, Japan)
Tatsuo Shiozawa (Toshiba, japan)
Yusuke Oike (Sony, Japan)
Sunao Torii (ExaScaler, Japan)

Steering Committee

Chair	**Hidetoshi Onodera** (Kyoto University)
Vice Chair	**Shinji Kimura** (Waseda University)
Secretaries	**Yutaka Tamiya** (Fujitsu Laboratories) **Nozomu Togawa** (Waseda University)
Past Chair	**Hiroto Yasuura** (Kyusyu University)
ASP-DAC 2017 General Chair	**Naofumi Takagi** (Kyoto University)
ASP-DAC 2016 General Chairs	**Rui Paulo da Silva Martins** (University of Macau)
ACM SIGDA Representative	**Yiran Chen** (University of Pittsburgh)
IEEE CAS Representative	**Atsushi Takahashi** (Tokyo Institute of Technology)
IEEE CEDA Representative	**Masanori Hashimoto** (Osaka University)
DAC Representative	**Naehyuck Chang** (Korea Advanced Institute of Science and Technology)
DATE Representative	**Jörg Henkel** (Karlsruhe Institute of Technology)
ICCAD Representative	**Shih-Chieh Chang** (National Tsing Hua University)
International Members	**Kiyoung Choi** (Seoul National University) **Oliver C.S. Choy** (the Chinese University of Hong Kong) **Yajun Ha** (National University of Singapore) **Yuchun Ma** (Tsinghua University) **Sri Parameswaran** (The University of New South Wales) **Ren-Song Tsay** (National Tsing Hua University) **Xiaoyang Zeng** (Fudan University)
Advisory Members	**Kunihiro Asada** (University of Tokyo) **Satoshi Goto** (Waseda University) **Fumiyasu Hirose** (Cadence Design Systems, Japan) **Masaharu Imai** (Osaka University) **Takashi Kambe** (Kinki University) **Tokinori Kozawa** **Chong-Min Kyung** (Korea Advanced Institute of Science and Technology) **Youn-Long Steve Lin** (National Tsing Hua University) **Isao Shirakawa** (University of Hyogo) **TingAo Tang** (Fudan University) **Kazutoshi Wakabayashi** (NEC) **Kenji Yoshida** (D2S KK)

University LSI Design Contest

The University LSI Design Contest has been conceived as a unique program at ASP-DAC. The purpose of the contest is to encourage research in LSI design at universities and its realization on a chip by providing opportunities to present and discuss the innovative and state-of-the-art design. The scope of the contest covers circuit techniques for (1) Analog / RF / Mixed-Signal Circuits, (2) Digital Signal Processer, (3) Microprocessors, and (4) Custom Application Specific Circuits / Memories, and methodologies for (a) Full-Custom / Cell-Based LSIs, (b) Gate Arrays, and (c) Field Programmable Devices.

This year, the University LSI Design Contest Committee received 25 designs from five countries/areas, and selected 20 designs out of them. The selected designs will be disclosed in Session 1S at three-minute presentations, followed by interactive discussions in front of their posters with light meals. For two outstanding designs, The Best Design Award and The Special Feature Award will be presented in the opening session. We sincerely acknowledge the other contributions to the contest, too. It is our earnest belief to promote and enhance research and education in LSI design in academic organizations. Please come to the University LSI Design Contest and enjoy the stimulating discussions.

Date: Tuesday, January 17, 2017
Place: Makuhari Messe International Convention Complex, International Conference Hall, 1F

Oral Presentation: Room 103 (11:05-12:20)
Poster Presentation: Lobby [Food will be served] (12:20-13:50)

University LSI Design Contest Committee Co-Chairs:

Noriyuki Miura
(Kobe University)

Hiroyuki Ito
(Tokyo Institute of Technology)

Designers' Forum

The Designers' Forum is a unique program that will share design experience and solutions of actual product designs of the industries. This year's program includes the invited talks on the advanced devices and networks for IoT applications, advanced automotive security, and advanced image sensing and processing. The forum also includes a panel discussion relating to the future of AI technologies.

Oral Sessions:	(5S) Advanced Devices and Networks for IoT Applications
	(8S) Advanced Automotive Security
	(9S) Advanced Image Sensing and Processing
Panel Discussions:	(6S) What is future AI we will create ? - "Doraemon" or "Terminator" ? -

Session 5S (13:50-15:30, Jan. 18th)

[Advanced Devices and Networks for IoT Applications]

In order to realize the system for various IoT applications, it must be considered the overall element technologies from the sensor-front to the cloud via the network. In this session, for the specified concrete IoT applications, it will introduce a distinctive technology to realize it. In details, the first presentation of this session describes an autonomous mesh networking technology that allows a maintenance-free deployment of the sensor node for the infrastructural monitoring system. The second is the small, high-performance and low- power CPU technology for the wearable devices used in the wellness applications. The third is the ultra-low- power circuit techniques for energy-harvesting which realizes a millimeter-size sensors strewn as a dust computing applications. The final presentation is DFS (dynamic frequency selection) technology that is an advanced network devices to communicate the huge amount of data generated from a various IoT applications.

Session 6S (15:50-17:30, Jan. 18th)

[What is future AI we will create? - "Doraemon" or "Terminator" ? -]

Nowadays, Artificial Intelligence (AI) research and development is in third boom. The driving force behind this advancement is deep learning technology. Its high level feature extraction ability was adopted in AI GO application "AlphaGO", and accomplished a great feat that AlphaGO overthrow human champion. But emergence of strong AI is now stirring up controversy simultaneously. Our job is just maybe replaced with AI power !! Is it true? What should we do, if autonomous AI has consciousness and has hostility toward human? These concerns is too excessive assumption, but we cannot ignore. So, in this panel session, we will discuss about real situation of current AI and think about future AI. Key word is "Doraemon" and "Terminator."

Session 8S (13:50-15:30, Jan. 19th)

[Advanced Automotive Security]

The security implementation for automotive is getting hot and essential toward autonomous driving. This session will visit its trend, hardware implementation, hardware attack and its countermeasure. The first talk presents recent threats in automotive systems and their countermeasures with security applications. The next presentation shows the actual implementation of hardware security module for microcontrollers. The third one demonstrates the hardware attack experience in academia and proposes the key management method. The final talk shares physical and logical attacks previously being used for smart card and their countermeasures.

Session 9S (15:50-17:30, Jan. 19th)

[Advanced Image Sensing and Processing]

Four advanced design examples of image sensors and processors are described. For designing better image quality and intelligent functionality on image sensing and processing, this session covers circuit techniques on analog-to-digital conversion, 3-D stacked device integration, system architecture integrating computational vision, and FPGA implementation efficiently accelerating partial image retrieval. The first talk presents a 250M-pixel CMOS image sensor employing column-parallel dual-gain amplifiers, followed by a back- illuminated stacked CMOS image sensor achieving multi-functional modes. The third presentation forecasts the next trend on machine vision beyond human eyes. The final talk demonstrates an FPGA-accelerated partial image-matching engine for massive media-data searching systems.

Designers' Forum Co-Chairs:

Masaitsu Nakajima
(socionext, Japan)

Koji Inoue
(Kyushu University, Japan)

ACM SIGDA Student Research Forum at ASP-DAC 2017

The Student Research Forum at the ASP-DAC is renovated from a traditional poster session hosted by ACM SIGDA for Ph.D. students to present and discuss their dissertation research with experts in system design and design automation community. Starting from 2015, the forum includes both Ph.D. and M.S. students, offering great opportunity for the students to establish contacts for their future career. In addition, the forum helps the companies and academic institutes to get an overview of the latest research and discover the extraordinary candidates for their employment. The forum is open to all students of the relevant research community and is free-of-charge.

Date and Time: 18:00-20:00, January 17th, 2017
Location: Room 201 [Food will be served.]

We would like to thank the following committee members for their support and contribution to this forum.

Technical committee:
Yiran Chen (University of Pittsburgh)
Yukihide Kohira (The University of Aizu)
Xin Li (Carnegie Mellon University)
Duo Liu (Chongqing University)
Shinobu Nagayama (Hiroshima City University)
Qinru Qiu (Syracuse University)
Muhammad Shafique (Vienna University of Technology)
Seiya Shibata (NEC)
Chun-Yao Wang (National Tsing Hua University)
Hai Wang (Univ. of Electronic Science & Technology of China)
Yu Wang (Tsinghua University)
Jason Xue (City University of Hong Kong)
Haibo Zeng (Virginia Tech)

ASP-DAC liaison:
Yukihide Kohira (University of Aizu)

The sponsors of this forum are ACM SIGDA and Cadence Design Systems, Inc. We would also like to thank ASP-DAC 2017 for supporting this forum.

ACM SIGDA Student Research Forum Chair:

Zili Shao
(The Hong Kong Polytechnic Univ.)

ACM SIGDA Student Research Forum Co-Chair:

Jingtong Hu
(Oklahoma State University)

Best Paper Award

Award Winners

9C-1: **"Classification Accuracy Improvement for Neuromorphic Computing Systems with One-level Precision Synapses "**

Yandan Wang, Wei Wen, Linghao Song, Hai Li (Univ. of Pittsburgh, U.S.A.)

8B-1: **"Spendthrift: Machine Learning Based Resource and Frequency Scaling for Ambient Energy Harvesting Nonvolatile Processors"**

Kaisheng Ma, Xueqing Li, Srivatsa Rangachar Srinivasa (Penn State Univ., U.S.A.), Yongpan Liu (Tsinghua Univ., China), John (Jack) Sampson (Penn State Univ., U.S.A.), Yuan Xie (UCSB, U.S.A.), Vijaykrishnan Narayanan (Penn State Univ., U.S.A.)

Candidates

1A-1: **"AGARSoC: Automated Test and Coverage-Model Generation for Verification of Accelerator-Rich SoCs"**

Biruk Mammo, Doowon Lee, Harrison Davis, Yijun Hou, Valeria Bertacco (Univ. of Michigan, U.S.A.)

2C-2: **"Workload-aware Static Aging Monitoring of Timing-critical Flip-flops"**

Arunkumar Vijayan, Saman Kiamehr, Fabian Oboril (Karlsruhe Inst. of Tech., Germany), Krishnendu Chakrabarty (Duke Univ., U.S.A.), Mehdi Tahoori (Karlsruhe Inst. of Tech., Germany)

3B-1: **"Efficient Parallel Verification of Galois Field Multipliers"**

Cunxi Yu, Maciej Ciesielski (Univ. of Massachusetts, Amherst, U.S.A.)

3C-1: **"Algorithm for Synthesis and Exploration of Clock Spines"**

Youngchan Kim, Taewhan Kim (Seoul National Univ., Republic of Korea)

4C-1: **"Network Flow Based Cut Redistribution and Insertion For Advanced 1D Layout Design"**

Ye Zhang, Wai-Shing Luk, Fan Yang, Changhao Yan (Fudan Univ., China), Hai Zhou (Northwestern Univ., U.S.A.), Dian Zhou (Univ. of Texas, Dallas, U.S.A.), Xuan Zeng (Fudan Univ., China)

5B-1: **"An Artificial Neural Network Approach for Screening Test Escapes"**

Fan Lin (Univ. of California, Santa Barbara, U.S.A.), Kwang-Ting Tim Cheng (Hong Kong Univ. of Science and Tech., Hong Kong)

7A-1: **"Improving LDPC Performance Via Asymmetric Sensing Level Placement on Flash Memory"**

Qiao Li, Liang Shi (Chongqing Univ., China), Chun Jason Xue (City Univ. of Hong Kong, Hong Kong), Qingfeng Zhuge, Edwin H.-M. Sha (Chongqing Univ., China)

7B-1: **"Trojan Localization using Symbolic Algebra"**

Farimah Farahmandi, Yuanwen Huang, *Prabhat Mishra (Univ. of Florida, U.S.A.)

7C-1: **"Towards Scalable and Efficient GPU-Enabled Slicing Acceleration for Continuous 3D Printing"**

Aosen Wang, Chi Zhou (State Univ. of New York at Buffalo, U.S.A.), Zhanpeng Jin (State Univ. of New York, Binghamton, U.S.A.), Wenyao Xu (State Univ. of New York at Buffalo, U.S.A.)

University LSI Design Contest Award

Best Design Award

1S-1: **"W-Band Ultra-High Data-Rate 65nm CMOS Wireless Transceiver"**
Korkut Kaan Tokgoz, Shotaro Maki, Seitarou Kawai, Noriaki Nagashima (Tokyo Inst. of Tech., Japan), Yoichi Kawano, Toshihide Suzuki, Taisuke Iwai (Fujitsu Labs., Japan), Kenichi Okada, Akira Matsuzawa (Tokyo Inst. of Tech., Japan)

Special Feature Award

1S-20: **"Design of High-Frequency Piezoelectric Resonator-Based Cascaded Fractional-N PLL with Sub-ppb-Order Channel Adjusting Technique"**
Yosuke Ishikawa, Sho Ikeda, Hiroyuki Ito (Tokyo Inst. of Tech., Japan), Akihumi Kasamatsu (NICT, Japan), Takayoshi Obara, Naoki Noguchi, Koji Kamisuki, Yao Jiyang (Tokyo Inst. of Tech., Japan), Shinsuke Hara, Ruibing Dong (NICT, Japan), Shiro Dosho, Noboru Ishihara, Kazuya Masu (Tokyo Inst. of Tech., Japan)

10-Year Retrospective Most Influential Paper Award

Award Winner

(ASP-DAC 2007)

8B-1: **"Thermal-Aware 3D IC Placement Via Transformation"**
Jason Cong, Guojie Luo, Jie Wei, Yan Zhang (Univ. of California, Los Angeles, United States)

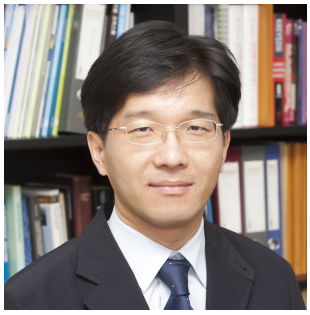
Candidates

2A-2: **"FastPlace 3.0: A Fast Multilevel Quadratic Placement Algorithm with Placement Congestion Control"**
Natarajan Viswanathan, Min Pan, Chris Chu (Iowa State Univ., United States)

3A-2: **"FastRoute 2.0: A High-quality and Efficient Global Router"**
Min Pan, Chris Chu (Iowa State Univ., United States)

9C-1: **"Multithreaded SAT Solving"**
Matthew Lewis, Tobias Schubert, Bernd Becker (Albert-Ludwigs-Univ. of Freiburg, Germany)

Invitation to ASP-DAC 2018



On behalf of the Organizing Committee, it is my great pleasure and honor to invite you to the 23rd ASP-DAC, to be held in Jeju Island, Korea, January 22-24, 2018. Jeju Island (also known as Jejudo or Jeju) is the largest island which lies on the southern side off the coast of the Korean Peninsula.

Jeju is famous for its natural scene of breathtaking beauty. It is a popular vacation spot and remains one of the top honeymoon destinations for newlyweds. There are many sightseeing points in Jeju such as: Mount Hallasan (the island's central dominant peak), Manjanggul Lava Tube, Sunrise Peak, to name just a few. In 2007, the volcanic island and lava tube cave systems were designated as UNESCO World Natural Heritage Sites. Jeju features pleasant weather all year round, from low 6°C (42°F) to high 27°C (80°F). Jeju can conveniently be reached from many cities in Asian countries through direct flight; the flight from Seoul, the capital city of Korea which is directly reachable from all over the world, to Jeju is about an hour.

Conference venue is International Convention Center Jeju (ICCJEJU), the facility famous for hosting many conferences and international meetings, e.g. ASEAN-KOREA Commemorative Summit 2009. It is located in the Jungmun Tourist Complex with the Ocean right on the south and Mount Hallasan in the north. It is close to a wide range of hotels, resorts, tourist attractions, restaurants, which probably will bring ASP-DAC 2018 participants a wonderful experience.

Jeju is not just famous for its tourist attractions. It is a hub of many IT companies. Holding ASP-DAC 2018 in Jeju will help the local academia and the worldwide academia and semiconductor industry to get closer and exchange electronic design knowledge and experience in Jeju and learn from the ASP-DAC community.

We warmly welcome participants from all around the world to meet and exchange our visions in the future design automation and embedded system design related technologies. Your active submissions are highly appreciated in order to contribute for an excellent technical program of ASP-DAC 2018.

We hope to see you all in Jeju Island with ASP-DAC 2018!

Youngsoo Shin
General Chair, ASP-DAC 2018

Tutorials

ASP-DAC 2017 offers attendees a set of two-hour intense introductions to specific topics. Each tutorial will be presented twice a day to allow attendees to cover multiple topics. If you register for tutorials, you have the option to select three out of the six topics.

	Monday, January 16			
	Room 102	Room 103	Room 104	Room 105
9:30	**Tutorial-1:** Silicon Photonics for Computing Systems: Opportunities, Challenges, and Implementations	**Tutorial-2:** Towards Energy-Efficient Intelligence in Power-/Area-Constrained Hardware	**Tutorial-3:** Post-Silicon Validation and Emulation-Based Validation Using Exercisers	**Tutorial-4:** Quick Start Guide of Digital PLL for Digital Designers
11:30	Lunch Break [coupon]			
12:45	**Tutorial-1:** Silicon Photonics for Computing Systems: Opportunities, Challenges, and Implementations	**Tutorial-2:** Towards Energy-Efficient Intelligence in Power-/Area-Constrained Hardware	**Tutorial-5:** The Emergence of Hardware Oriented Security and Trust	**Tutorial-6:** Cross-Layer Reliability Aware Design, Optimization and Dynamic Management
14:45	Break			
15:15	**Tutorial-3:** Post-Silicon Validation and Emulation-Based Validation Using Exercisers	**Tutorial-4:** Quick Start Guide of Digital PLL for Digital Designers	**Tutorial-5:** The Emergence of Hardware Oriented Security and Trust	**Tutorial-6:** Cross-Layer Reliability Aware Design, Optimization and Dynamic Management
17:15				

Tutorial-1 Monday, January 16, 9:30 - 11:30, 12:45 - 14:45@Room 102

Silicon Photonics for Computing Systems: Opportunities, Challenges, and Implementations

Organizers:

Jiang Xu (Hong Kong University of Science and Technology), **Yuichi Nakamura** (NEC)

Speakers:

Jiang Xu (Hong Kong University of Science and Technology), **Shigeru Nakamura** (NEC)

Tutorial Outline:

Computing systems, from HPC and data center to automobile and cellphone, are integrating growing numbers of processors, accelerators, memories, and peripherals to meet the burgeoning performance requirements of new applications under tight energy and thermal constraints. Recent advances in silicon photonics technologies promise ultra-high bandwidth, low latency, and great energy efficiency to alleviate the inter-rack, intra-rack, intra-board, and intra-chip communication bottlenecks in computing systems. Silicon photonics technologies piggyback onto developed silicon fabrication processes to provide viable and cost-effective solutions. Industry and academia have been actively developing silicon photonics technologies for the last decade. A large number of silicon photonics devices and circuits have been demonstrated in CMOS-compatible fabrication processes. Silicon photonics technologies open up new opportunities for architectures, design techniques, and EDA tools to fully explore new approaches and address the challenges of next-generation computing systems. This tutorial reviews the latest progresses and provides insights into the challenges and future developments, and covers the following topics.

- Implementation examples
- Optical and electrical interconnects and OE interfaces
- Integrated optical switches
- Inter/intra-chip optical networks
- High-radix optical switching fabric
- Optical thermal effects
- Optical crosstalk noises
- Modeling, analysis, and simulation platforms

Tutorial-2 Monday, January 16, 9:30 - 11:30, 12:45 - 14:45@Room 103

Towards Energy-Efficient Intelligence in Power-/Area-Constrained Hardware

Organizer:

Jae-sun Seo (Arizona State Univ.)

Speakers:

Zhengya Zhang (U. Michigan, Ann Arbor), **Mingoo Seok** (Columbia Univ.), **Jae-sun Seo** (Arizona State Univ.)

Tutorial Outline:

In recent years, machine learning algorithms (e.g. deep neural networks) have become widespread across a broad range of vision, speech, and biomedical applications. For similar cognitive tasks, there also has been a surge of interest in neuromorphic computing (e.g. spiking neural networks), which more closely follow biological nervous systems.

While state-of-the-art deep learning algorithms keep advancing designs of large-scale network models (e.g., 1000-layer networks) for incremental accuracy improvement, many embedded hardware applications face limitations on their scale in terms of cost, power, and area. Several special purpose hardware solutions (e.g., IBM TrueNorth, DaDianNao, MIT Eyeriss) have been previously proposed to help bring expensive algorithms to a low-power processor; however, limitations still exist in homogeneous architecture, memory footprint, on-chip communication, and online learning capability. It is a challenging task to enable essential machine learning and neuromorphic processors in mobile, wearable, internet of things (IoT), and in extreme implantable devices, due to their divergent constraints in low power and small footprint. Efficient hardware implementation on these different platforms thus require substantial and holistic system enhancements that include computation (e.g., low-precision/approximate computing), memory (e.g., weight/network compression), and communication (e.g., processor-in-memory, spatial architecture).

In this context, this tutorial will present a range of recent algorithm/architecture/circuit/device co-design techniques that can advance the hardware implementation of learning and classification algorithms for various embedded applications, such as computer vision, speech recognition, personal health monitoring, brain-computer interface, etc. We will present results of recent CMOS ASIC prototype designs, as well as technology beyond CMOS, which employ software-hardware co-design to accomplish substantial improvements in performance, energy efficiency and form factor. The proposed and demonstrated techniques include model/memory compression, architecture optimization, novel circuit design, incorporation of emerging devices, and neuro-inspired learning. These techniques will effectively reduce the computation complexity, memory footprint, and communication energy, thereby improving the overall mapping of machine learning and neuromorphic algorithms to energy- and size-constrained embedded platforms. This tutorial will help shed light on the tremendous potential and research needs towards energy- efficient intelligence in ubiquitous resource-constrained hardware systems.

Tutorial-3 Monday, January 16, 9:30 - 11:30@Room 104, 15:15 - 17:15@Room 102

Post-Silicon Validation and Emulation-Based Validation Using Exercisers

Organizers:

Ronny Morad (IBM Research - Haifa), **Vitali Sokhin** (IBM Research - Haifa)

Speakers:

Ronny Morad (IBM Research - Haifa), **Vitali Sokhin** (IBM Research - Haifa)

Tutorial Outline:

A study conducted by Wilson Research Group and Mentor Graphics in 2014 reveals that 70% of the designs don't make it to first silicon success and require re-spins. Various chip vendors reported that more than 1% of their bugs escape to silicon. Also 57% of the verification projects that involve big designs (>80M gates) use emulation. More and more companies realize that simulation alone is just not enough for ensuring that their design is clean of bugs and turn to a fast platform, whether silicon or emulation or both. However, the unique characteristics of the fast platforms (on the one hand speed, on the other hand, limited observability and controllability) make it very challenging to use them efficiently. Simply re-using tests from simulation won't give the desired benefit. A bare-metal exerciser is a technology which is increasingly used by various chip vendors for validation on emulation and silicon. An exerciser is basically a program which generates a test, executes it and then checks for correctness, all on the Design Under Test itself without any communication with a host machine. This enables high utilization of the fast platform. In addition light-weight generation gives variability without sacrificing performance. The fact that an exerciser is bare-metal means that it does not rely on an operating system, and therefore it's easier to debug a failure. The collective experience of various chip vendor companies (IBM and others) show that bare-metal exercisers are very efficient in finding unique and severe bugs that no other tool or environment were able to find.

In this two hours tutorial we'll cover the motivation for post-silicon and emulation-based validation. We'll go over existing practices and discuss their advantages as well as limitations. We'll then turn to describing bare-metal exercisers in details. We'll explain the concept, the requirements from an exerciser, and analyze the software architecture of a state-of-the-art exerciser. We'll also cover a recommended methodology for using exercisers and share experience of several companies that use exercisers. We'll conclude with presenting open problems and research directions in this domain.

This tutorial is intended for practitioners from the industry who would like to learn more about post-silicon in general and about the role of exercisers in particular as well as for academics who are looking to extend their knowledge about post-silicon validation and the research challenges it presents.

Tutorial-4 Monday, January 16, 9:30 - 11:30@Room 105, 15:15 - 17:15@Room 103

Quick Start Guide of Digital PLL for Digital Designers

Organizer:

Kenichi Okada (Tokyo Institute of Technology)

Speakers:

Kenichi Okada (Tokyo Institute of Technology), **Salvatore Levantino** (Politecnico di Milano)

Tutorial Outline:

This tutorial will introduce the fundamentals of digital phased-locked loops (PLL's) for clock generation in Systems on Chip (SoC's). Nowadays, tens of PLLs are integrated into a single large SoC. So, jitter, area/power utilization, and design effort of clock generators are key parameters. Though PLLs have been typically designed by analog designers, fully- or mostly-synthesized digital PLLs in scaled CMOS processes are taking over traditional designs. They consist of only logic gates taken from the digital standard-cell library, so that their netlist and layout can be automatically generated by commercial digital EDA tools. After reviewing the basic architectures of digital PLLs, the tutorial will discuss the design of the main building blocks such as digitally-controlled variable delay line, digitally-controlled oscillator, divider chain, frequency locked loop, and digital loop filter. The second part of the tutorial will deal with more advanced architectures of synthesizable clock generators, such as bang-bang digital PLLs, injection locking PLLs, and multiplying delay-locked loops (MDLLs). Finally, we will move to fractional-N clock generation reviewing the most advanced techniques such as those based on digital/time converters (DTCs). By the end of this tutorial, the attendee will be able to start the design of a synthesizable digital PLL.

Tutorial-5 Monday, January 16, 12:45 - 14:45, 15:15 - 17:15@Room 104

The Emergence of Hardware Oriented Security and Trust

Organizer:

Chip-Hong Chang (Nanyang Technological Univ.)

Speakers:

Chip-Hong Chang (Nanyang Technological Univ.), **Yier Jin** (Univ. of Central Florida)

Tutorial Outline:

Hardware has long been touted as dependable and trustable entity than the software running on it. The illusion that attackers cannot easily access the isolated integrated circuit (IC) supply chain has once and again been invalidated by remotely activated hardware Trojan and untraceable break-ins of networking systems running on fake and subverted chips reported by businesses and military strategists, and confirmed by forensic security experts analysing recent incidents. The situation was aggravated by the geographical dispersion of chip design activities and the heavy reliance on third-party hardware intellectual properties (IPs). Counterfeit chips (such as unauthorized copies, remarked/recycled dice, overproduced and subverted chips or cloned designs) pose a major threat to all stakeholders in the IC supply chain, from designers, manufacturers, system integrators to end users, in view of the severe consequence of potentially degraded quality, reliability and performance that they caused to the electronic equipment and critical infrastructure. Unfortunately, tools that can analyse the circuit netlist for malicious logic detection and full functionality recovery are lacking to prevent such design backdoors, counterfeit and malicious chips from infiltrated into the integrated circuit (IC) design and fabrication flow. This tutorial addresses and reviews recent development in preventive countermeasures, post-manufacturing diagnosis techniques and emerging security-enhanced primitives to avert these hardware security threats. This tutorial will also cover the emerging topics where hardware platforms are playing an active role in system protection and intrusion detection. It aims to create an awareness of the ultimate challenges and solutions in addressing hardware security issues in the new age of Internet of Things (IoT), where the intense interactions between devices and devices, and devices and humans have introduced new vulnerabilities of embedded devices and integrated electronic systems.

Tutorial-6 Monday, January 16, 12:45 - 14:45, 15:15 - 17:15@Room 105

Cross-Layer Reliability Aware Design, Optimization and Dynamic Management

Organizer:

Sheldon Tan (UC Riverside)

Speakers:

Sheldon Tan (UC Riverside), **Mehdi Tahoori** (Karlsruhe Inst. Tech.), **Hai-Bao Chen** (Shanghai Jiao Tong Univ.)

Tutorial Outline:

Reliability has become a significant challenge for design of current nanometer integrated circuits (ICs). It was expected that the future chips will show signs of reliability-induced age much faster than the previous generations. It is predicted that the mean time between failure (MTBF) for the future exascale computing will be around 30 minutes using today's devices and computing platforms. Furthermore, long-term reliability degradation caused by aging effects are becoming a limiting constraint in 3D ICs and emerging FinFET devices due to increased failure rates. Semiconductor industry faces new challenges to maintain the reliability in the reality of ever- continued increase in the die size and number of transistors accompanying by the performance driven down-scaling in transistor size. This has led the International Technology Roadmap For Semiconductor (ITRS) to predict the onset of significant reliability problems in the future, and at a pace that has not been seen in the past. Existing technologies for ensuring reliability will not be able to satisfy the competing requirements for future ICs as they typically operate in one layer under worst-case assumptions about other layers in the design stacks. This potentially leads to inefficiencies that will make these techniques impractical in future fabrication processes.

The first part of the tutorial will describe novel approach and techniques for recently proposed physics-based electromigration (EM) modeling and assessment methods. We will present a newly proposed a physics-based model for both void nucleation phase and void growth phase and show how this new model can be applied for full-chip power grid EM analysis to account the essential redundancy of on-chip power grid networks. We then present a novel method to calculate the hydrostatic stress evolution inside a multi-branch interconnect tree that allows to avoid over optimistic prediction of the time to failure (TTF) made with the Blech-Black analysis of individual branches of interconnect tree. We further show how to extend the new physics- based model to consider the time-varying current and temperature stressing conditions, which are common working chip conditions. We finally show a recently proposed novel voltage-based EM immortality check algorithm for general interconnect trees and a new EM-signoff flow, which consists of fast EM immortality check and detailed numerical FFT analysis and its potential engagement with EM-aware physical design.

The second part of this tutorial targets device aging and in particular bias temperature instability (BTI) and hot carrier injection (HCI) which affect transistor performance over time. These aging mechanisms degrade the threshold voltage of transistors and lead to timing failures in logic paths and reduced signal to noise margin (SNM) in memories. We will cover various static (design time) as well as dynamic (based on runtime monitoring) techniques to analyze, monitor and mitigate aging effects in both logic and memory components. The effective solutions are cross- layer, meaning that they cover a wide range of abstraction levels and design stacks to be able to tackle this problem with minimum costs. The design time solutions prolog the lifetime of the circuit by minimizing the amount of aging stress on timing critical components of the design and maximizing the duration of aging relaxation for better aging recovery. Moreover, we show how aging-awareness can be integrated during logic synthesis. The runtime solutions monitor the amount of critical stress on the circuit and try to use proactive fine-grain aging mitigation to balance performance, power and aging during system operation.

In the third part of this tutorial, we will focus on the dynamic reliability management (DRM) technique based on the newly proposed electromigration models. First we will present a resource based EM model, which model the reliability or FFT of a wire due to EM effects as resources at the system level. Then we present a novel task migration method to explicitly balance consumption of EM resources for all the cores. The new method aims at the equal chance of failure of these cores, which will maximize the lifetime of the whole multi/many core system. Second, we present new DRM techniques for emerging many-core dark silicon processors. We employ the dynamic voltage and frequency scaling (DVFS) and dark silicon core on/off status as the controling knots. We show how the energy or lifetime of cores can be optimized subject to performance, temperature and lifetime constraints. On top of this, we show if soft errors and hard reliability like EM are considered at the same time, reliability constrained energy or performance optimization will become more challenging due to conflicting impacts of powers on those reliability effects. Finally, we show how the relativity modeling and management can be done at the datacenter level. We will present a new combined datacenter power and reliability compact model using a learning based approach in which a feed-forward neural network (FNN) is trained to predict energy and long term reliability for each processor under datacenter scheduling and workloads.

At a glance

Tuesday, January 17

	S (Room 103)	A (Room 102)	B (Room 104)	C (Room 105)
8:30	**Opening & Keynote I** (International Conference Room [2F])			
10:35	Coffee Break			
11:05	1S: University Design Contest	1A: Design Assurance and Reliability	1B: New Frontiers of Hardware Accelerator Synthesis	1C: Analysis Techniques for Reliability and Manufacturability
12:20	Lunch Break / **University Design Contest Poster Discussion** (Lobby)			
13:50	2S: **(Special Session)** Neuromorphic Computing and Low-Power Image Recognition	2A: System-level Techniques for Energy and Performance Optimization	2B: Pushing the Limits of Logic Synthesis	2C: Design Techniques for Reliability Enhancement
15:30	Coffee Break			
15:50	3S: **(Special Session)** Let's Secure the Physics of Cyber-Physical Systems	3A: Novel Techniques to Improve the Simulation Performance	3B: Formal and Informal Verification	3C: Pursuing System to Circuit Level Optimality in Timing and Power Integrity
17:30	Break			
18:00	ACM SIGDA Student Research Forum at ASP-DAC 2017 (Room 201 [2F])			
20:00				

Wednesday, January 18

	S (Room 103)	A (Room 102)	B (Room 104)	C (Room 105)
9:00	**Keynote II** (International Conference Room [2F])			
9:50	Coffee Break			
10:15	4S: **(Special Session)** Emerging Technologies for Biomedical Applications: Artificial Vision Systems and Brain Machine Interface	4A: Power and Thermal Management	4B: Emerging Topics in Hardware Security	4C: Manufacturability and Emerging Techniques
12:20	Lunch Break / **Supporters' Session** (Room 201 [2F])			
13:50	5S: **(Designers' Forum)** Advanced Devices and Networks for IoT Applications	5A: Approximate Computation for Energy Efficiency	5B: Advance Test and Fault Tolerant Technologies	5C: Advanced Placement and Routing Techniques
15:30	Coffee Break			
15:50	6S: **(Designers' Forum)** Panel Discussion: What is future AI we will create ? - "Doraemon" or "Terminator" ? -	6A: Recent Advances in Circuit Simulation and Optimization	6B: Application-Aware Embedded Architecture Design	6C: Advances in Microfluidic Biochips
17:30	Break			
18:00	**Banquet** (Convention Hall A [2F])			
20:00				

Thursday, January 19

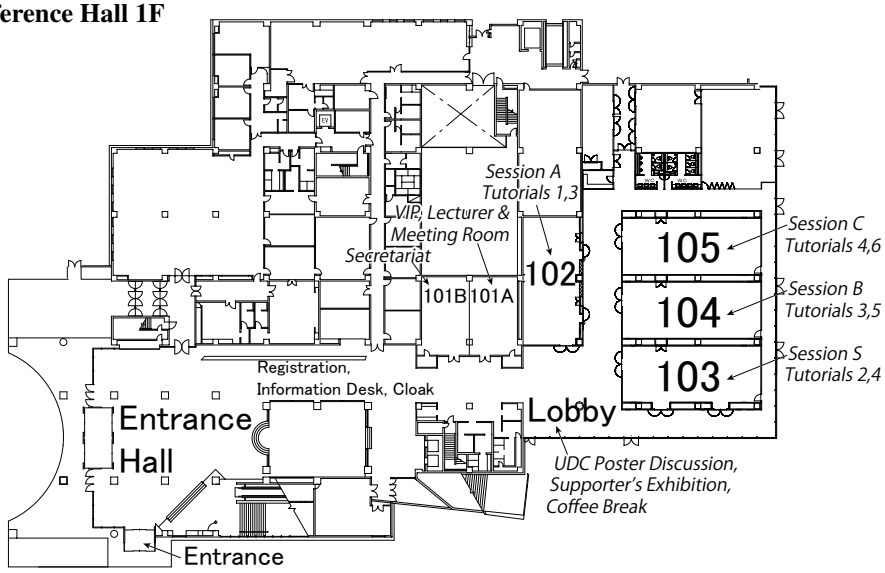
	S (Room 103)	A (Room 102)	B (Room 104)	C (Room 105)
9:00	**Keynote III** (International Conference Room [2F])			
9:50	Coffee Break			
10:15	7S: **(Special Session)** When Backend Meets Frontend: Cross-Layer Design & Optimization for System Robustness	7A: NVM/Flash: From Advanced Storage Design to Emerging Applications	7B: Hardware Diversity and Hardware Trojan	7C: Hardware Accelerator for Emerging Applications
12:20	Lunch Break			
13:50	8S: **(Designers' Forum)** Advanced Automotive Security	8A: Scheduling, Resource Management, and Simulation for Multi-Core Systems	8B: Machine Learning: Acceleration and Application	8C: Design Automation and Modeling for Emerging Technologies
15:30	Coffee Break			
15:50	9S: **(Designers' Forum)** Advanced Image Sensing and Processing	9A: New Directions in Networks on Chip	9B: Memory Architecture: Now and Future	9C: Intelligent Computing with Memristor Technologies
17:30				

Room Assignment

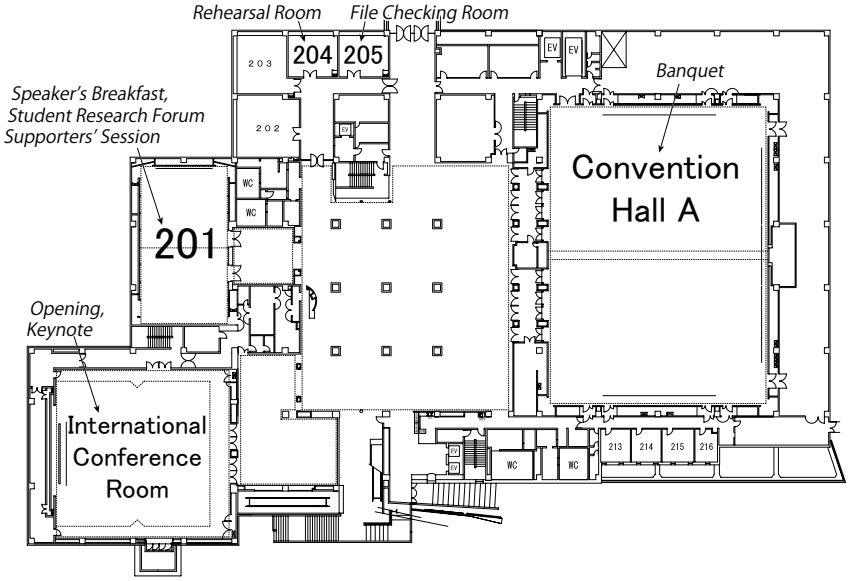
Room Assignment

Location	Event
Entrance Hall (1F)	Registration, Information Desk, and Cloak
International Conference Room (2F)	Opening and Keynote I,II,III
103 (1F)	Session S, Tutorials 2,4, and University Design Contest
102 (1F)	Session A and Tutorials 1,3
104 (1F)	Session B and Tutorials 3,5
105 (1F)	Session C and Tutorials 4,6
Lobby (1F)	Poster Discussion, Supporter's Exhibition, and Coffee Break
Convention Hall A (2F)	Banquet
201 (2F)	Speaker's Breakfast, ACM SIGDA Student Research Forum, and Supporters' Session
204 (2F)	Rehearsal Room
205 (2F)	File Checking Room

International Conference Hall 1F



International Conference Hall 2F



Keynote Addresses

Keynote I

Tuesday, January 17, 9:00-10:35

"In Memory of Edward J. McCluskey: The Next Wave of Pioneering Innovations"

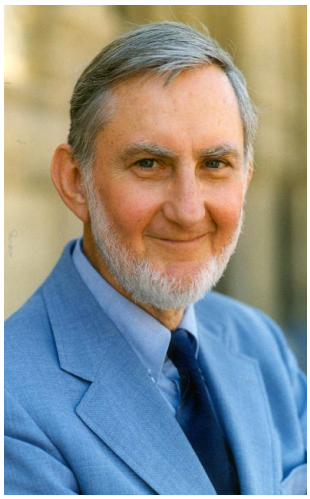
Organizers:

Prof. Subhasish Mitra (Stanford University)

Prof. Deming Chen (University of Illinois at Urbana-Champaign)

This special plenary session will celebrate Prof. McCluskey (who passed away in 2016) through three keynote speeches by world-renowned scholars on the next wave of pioneering innovations, starting with a memorial speech by Prof. Jacob Abraham of University of Texas at Austin.

Memories of Professor Edward J. McCluskey

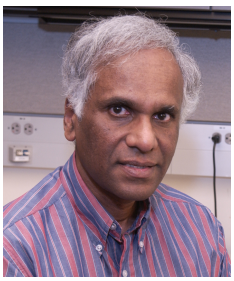


Prof. Edward J. McCluskey was a giant who shaped the design and testing of digital systems for over half a century. He sustained a relentless pace of fundamental contributions for efficient and robust design, high-quality testing, and reliable operation of digital systems. He was also a pioneer in establishing and fostering computer engineering as a profession.

Many consider him as the father of modern digital design. Many of his contributions to logic design, testing and fault-tolerant computing are classics: the Quine-McCluskey logic minimization procedure (which marked the beginning of Electronic Design Automation), hazards in logic circuits and fundamental-mode sequential circuits, algebraic fault properties, Murphy and ELF experiments establishing test metrics (rather than fault models) as key to high-quality testing, Very Low Voltage testing, and many key concepts in fault-tolerant computing that are even more essential for safety in future applications such as self-driving cars.

Prof. McCluskey was one of the world's leading educators. His textbooks on logic design defined the discipline. Computer Engineering and the IEEE Computer Society owe their current status to Ed in a major way. He was first president of the IEEE Computer Society. At Stanford, he founded the Digital Systems Lab (renamed Computer Systems Lab) that uniquely cultivated collaboration between EE and CS. In addition to shaping the development of digital systems, he was a great educator, producing an incredible group of 75 PhD graduates, many of whom have gone on to become industry leaders. He founded the Center for Reliable Computing (CRC) at Stanford. CRC played a major role in advancing the fields of computer reliability and testing from ad hoc pursuits to frontline academic and industrial research.

Ed received numerous awards and honors including the IEEE Emanuel R. Piore Award "for pioneering and fundamental contributions to design automation and fault tolerant computing," the IEEE John von Neumann Medal for "fundamental contributions that shaped the design and testing of digital systems," and the IEEE Computer Society's Computer Pioneer Award "for seminal contributions to the design and synthesis of digital systems over five decades, including the first algorithm for logic synthesis (the Quine-McCluskey method)."



Memorial Speech: **Tribute to Professor Edward J. McCluskey**

Prof. Jacob Abraham
University of Texas at Austin

Keynote I-1: **Heterogeneous Integration of X-tronics: Design Automation and Education**

Prof. K.-T. Tim Cheng
Hong Kong University of Science and Technology

Advances in photonics, flexible electronics, emerging memories, etc. and Si electronics' integration with these devices have enabled new classes of integrated circuits and systems with enhanced functionality, higher performance, or lower power consumption. Driving greater integration of such heterogeneous X-tronics can facilitate the continued proliferation of low-cost micro-/nano-systems for a wide range of applications. However, achieving their large-scale integration will require design ecosystem and design automation tools/methodologies much like those that enabled electronic integration in previous decades. In this talk, I will briefly introduce two recent Manufacturing Innovation Institutes, on Integrated Photonics and on Flexible Hybrid Electronics respectively, and a research center on developing 3D Hybrid CMOS-memristor circuits, which bring together academia, industry, and federal partners to increase U.S. manufacturing competitiveness in these areas. I will then focus on their design automation efforts and highlight the needs, challenges and opportunities of developing a robust design ecosystem for X-tronics integration. I will also share the educational challenges of talent development for X-tronics design automation.

Keynote I-2: **Electronics for the Human Body**

Prof. John Rogers
Northwestern University

Biology is soft, curvilinear and transient; modern semiconductor technologies are rigid, planar and everlasting. Electronic and optoelectronic systems that eliminate this profound mismatch in properties create opportunities for devices that can intimately integrate with the body, for diagnostic, therapeutic or surgical function with important, unique capabilities in biomedical research and clinical healthcare. Over the last decade, a convergence of new concepts in mechanical engineering, materials science, electrical engineering and advanced manufacturing has led to the emergence of diverse, novel classes of 'biocompatible' electronic platforms. This talk describes the key ideas, with examples ranging from wireless, skin-like electronic 'tattoos' for continuous monitoring of physiological health, to multiplexed, conformal sensor sheets for mapping cardiac electrophysiology, to bioresorbable intracranial sensors for treating traumatic brain injury.

Keynote I-3: **Design of Society: Beyond Digital System Design**

Prof. Hiroto Yasuura
Kyushu University

The progress of digital system design and production technologies have produced social innovation by Information Communication Technology (ICT). Most social systems and our daily lives are fully supported by ICT. The progress has been accelerated exponentially and destructive innovations have occurred in various fields in industries and societies. Governments emphasize Industry 4.0 or Society 5.0 and people are looking for new businesses with IoT and AI with Big Data. In this talk, I will look back on the growth of ICT and look forward to future society which we will create using ICT. We can say that design technology of digital systems is now expanding to design of societies.

Keynote II

Wednesday, January 18, 9:00-9:50

"Emerging Medical Technologies for Interfacing the Brain: From Deep Brain Stimulation to Brain Computer Interfaces"

Dr. Napoleon Torres-Martinez
CEA LETI

Evolving medical technologies, including stimulators, infusion pumps, and neuroprosthesis, are addressing progressively a wide range of neurological conditions, bringing fresh hope to patients where other solutions have proven to be ineffective. In this context, brain-computer interfaces (BCIs), that allow interaction between neural tissue and an external device, have been developed for a many diverse conditions; in particular, they have allowed severely motor disabled patients to communicate and integrate better within their environment. Further, brain electrical stimulators or deep brain stimulators (DBS) have been in use for several decades for Parkinson disease and others diseases, giving patients new levels of quality of life not possible with more conventional pharmacological therapies. In addition, there are recent reports of various physical optical phenomena that produce a reduction in degeneration within targeted brain areas, opening new avenues for the treatment of neurological debilitating conditions. All these advances are however, limited by the mandatory long process of technological maturation and testing, for the benefit optimization and safety. Our institution has been developing new devices in these key areas, integrating medical teams and engineering expert from the device conception, addressing clear clinical problems from the early steps. New technologies are being made simpler and ever more close to reality and clinical trial than before; the design of innovative solutions to improve implantable devices opens a new era in clinical research.

Keynote III

Thursday, January 19, 9:00-9:50

"All-Programmable FPGAs: More Powerful Devices Require More Powerful Tools"

Dr. Steve Trimberger
Xilinx Research Labs

Since their inception, FPGAs have changed significantly in their capacity and architecture. The devices we use today are called upon to solve problems in mixed-signal, high-speed communications, signal processing and compute acceleration that early devices could not address. The devices continue to grow in capability and complexity. In order for designers to use them effectively, new tools are required. This talk describes the evolution of FPGA devices and tools from the earliest days to the present day, and outlines the devices and tools needed in the coming decade.

1K Opening & Keynote I

Time: 8:30 - 10:35, Tuesday, January 17, 2017
Location: International Conference Room

1S University Design Contest

Time: 11:05 - 12:20, Tuesday, January 17, 2017
Location: Room 103
Chairs: Noriyuki Miura (Kobe Univ., Japan), Hiroyuki Ito (Tokyo Inst. of Tech., Japan)

1A Design Assurance and Reliability

Time: 11:05 - 12:20, Tuesday, January 17, 2017
Location: Room 102
Chairs: Chih-Tsun Huang (National Tsing Hua Univ., Taiwan), Franco Fummi (Univ. of Verona, Italy)

1B New Frontiers of Hardware Accelerator Synthesis

Time: 11:05 - 12:20, Tuesday, January 17, 2017
Location: Room 104
Chairs: Seiya Shibata (NEC, Japan), Takefumi Miyoshi (e-trees.Japan)

1C Analysis Techniques for Reliability and Manufacturability

Time: 11:05 - 12:20, Tuesday, January 17, 2017
Location: Room 105
Chairs: Shao-Yun Fang (National Taiwan Univ. of Science and Tech., Taiwan), Song Chen (Univ. of Science and Tech. of China, China)

2S (Special Session) Neuromorphic Computing and Low-Power Image Recognition

Time: 13:50 - 15:30, Tuesday, January 17, 2017
Location: Room 103
Organizers/Chairs: Yiran Chen (Univ. of Pittsburgh, U.S.A.), Bo Yuan (City Univ. of New York, U.S.A.), Yung-Hsiang Lu (Purdue Univ., U.S.A.), Ying Wang (Chinese Academy of Sciences, China)

2A System-level Techniques for Energy and Performance Optimization

Time: 13:50 - 15:30, Tuesday, January 17, 2017
Location: Room 102
Chairs: Liang Shi (Chongqing Univ., China), Takatsugu Ono (Kyushu Univ., Japan)

2B Pushing the Limits of Logic Synthesis

Time: 13:50 - 15:30, Tuesday, January 17, 2017
Location: Room 104
Chairs: Shouyi Yin (Tsinghua Univ., China), Shinobu Nagayama (Hiroshima City Univ., Japan)

2C Design Techniques for Reliability Enhancement

Time: 13:50 - 15:30, Tuesday, January 17, 2017
Location: Room 105
Chairs: Yukihide Kohira (Aizu Univ., Japan), Tetsuaki Matsunawa (Toshiba, Japan)

3S (Special Session) Let's Secure the Physics of Cyber-Physical Systems

Time: 15:50 - 17:30, Tuesday, January 17, 2017
Location: Room 103
Organizers/Chairs: Mohammad Al Faruque (Univ. of California Irvine, U.S.A.), Anupam Chattopadhyay (Nanyang Technological Univ., Singapore), Francesco Regazzoni (ALaRI - USI, Switzerland)

3A Novel Techniques to Improve the Simulation Performance

Time: 15:50 - 17:30, Tuesday, January 17, 2017
Location: Room 102
Chairs: Ing-Jer Huang (National Sun Yat-sen Univ., Taiwan), Masashi Tawada (Waseda Univ., Japan)

3B Formal and Informal Verification

Time: 15:50 - 17:30, Tuesday, January 17, 2017
Location: Room 104
Chairs: Jason Verley (Sandia National Laboratory, U.S.A.), Rajit Manohar (Cornell Univ., U.S.A.)

3C Pursuing System to Circuit Level Optimality in Timing and Power Integrity

Time: 15:50 - 17:30, Tuesday, January 17, 2017
Location: Room 105
Chairs: Takashi Sato (Kyoto Univ., Japan), Sheldon Tan (Univ. of California, Riverside, U.S.A.)

SRF ACM SIGDA Student Research Forum at ASP-DAC2017

Time: 18:00 - 20:00, Tuesday, January 17, 2017
Location: Room 201
Chair: Zili Shao (The Hong Kong Polytechnic Univ., Hong Kong)

SRF-1: Memory Sleep-Aware Task Allocation and Scheduling Algorithm Design for Energy Efficiency
Chenchen Fu (City University of Hong Kong)

SRF-2: Linearity Enhancements of Receiver Front-end Circuits for Wireless Communication
Mohammed Abdulaziz (Lund University)

SRF-3: Exploiting Process Variation for LDPC Read Performance Improvement on Flash Memory based Storage Systems
Qiao Li (Chongqing University)

SRF-4: Cross-Layer Approach for Power Delivery and System Architecture Co-Exploration
Kassan Unda (University of Notre Dame)

SRF-5: Performance and Reliability Optimization of NoC-based MPSoCs Via Fine-grained Communication Consideration
Lei Yang (Chongqing University)

SRF-6: Real-Time Communication over Wormhole-Switched On-Chip Networks
Meng Liu (Mälardalen University)

SRF-7: Making Frequent Pattern Mining Durable and Scalable
Yi Lin (Chongqing University)

SRF-8: Piracy Prevention of Digital Microfluidic Biochips
Ching-Wei Hsieh (National Tsing Hua University)

SRF-9: Energy-Efficient and Secure Reconfigurable Computing Architecture
Robert Karam (University of Florida)

SRF-10: Consolidating Automotive Applications on Clustered Many-Core Platforms
Matthias Becker (Mälardalen University)

SRF-11: Modeling and calibration of interconnect corners
Daijoon Hyun (KAIST)

SRF-12: A Highly Parallel Query Processor on 65-nm SOTB Process For Fast Data Analytics
Xuan-Thuan Nguyen (The University of Electro-Communications)

SRF-13: Area-Efficient Soft-Error Tolerant Datapath Synthesis Considering Adjacency Constraint between Components
Junghoon Oh (Japan Advanced Institute of Science and Technology)

SRF-14: A Guided Maze-based Length Controllable Router for Signal Delay Matching
Mitsuru Matsushita (Kochi University)

SRF-15: An Arithmetic Processor Using CORDIC Algorithm
Hong-Thu Nguyen (The University of Electro-Communications)

2K Keynote II

Time: 9:00 - 9:50, Wednesday, January 18, 2017
Location: International Conference Room
Chair: Masaharu Imai (Osaka Univ., Japan)

4S (Special Session) Emerging Technologies for Biomedical Applications: Artificial Vision Systems and Brain Machine Interface

Time: 10:15 - 12:15, Wednesday, January 18, 2017
Location: Room 103
Organizer: Masaharu Imai (Osaka Univ., Japan), Moderator: Yoshinori Takeuchi (Osaka Univ., Japan)

4A Power and Thermal Management

Time: 10:15 - 12:20, Wednesday, January 18, 2017
Location: Room 102
Chair: Koji Inoue (Kyushu Univ., Japan)

4B Emerging Topics in Hardware Security

Time: 10:15 - 12:20, Wednesday, January 18, 2017
Location: Room 104
Chairs: Xiaoxiao Wang (Beihang Univ., China), Kazuo Sakiyama (Univ. of Electrical Communications, Japan)

4C Manufacturability and Emerging Techniques

Time: 10:15 - 12:20, Wednesday, January 18, 2017
Location: Room 105
Chairs: Taewhan Kim (Seoul National Univ., Republic of Korea), Wenjing Rao (Univ. of Illinois, U.S.A.)

5S (Designers' Forum) Advanced Devices and Networks for IoT Applications

Time: 13:50 - 15:30, Wednesday, January 18, 2017
Location: Room 103
Organizers: Koichiro Yamashita (Fujitsu Labs., Japan), Tatsuo Shiozawa (Toshiba, Japan), Masaru Kokubo (Hitachi, Japan), Chair: Koichiro Yamashita (Fujitsu Labs., Japan)

5S-3 (Time: 14:40 - 15:05)
(Invited Paper) Ultra-Low-Power Wireless Sensor Nodes with Energy Harvesting, and IoT gateway Technology
Hiroki Morimura (NTT, Japan)

5S-4 (Time: 15:05 - 15:30)
(Invited Paper) Fast Channel Switching Technique for Interference Avoidance with 5 GHz Dual Channel Wireless LAN
Takashi Takeuchi (Hitachi, Japan)

5A Approximate Computation for Energy Efficiency

Time: 13:50 - 15:30, Wednesday, January 18, 2017
Location: Room 102
Chairs: Li Shang (Univ. of Colorado, U.S.A.), Shinobu Miwa (Univ. of Electro-Communications, Japan)

5B Advance Test and Fault Tolerant Technologies

Time: 13:50 - 15:30, Wednesday, January 18, 2017
Location: Room 104
Chairs: Satoshi Ohtake (Oita Univ., Japan), Ying Wang (Chinese Academy of Sciences, China)

5C Advanced Placement and Routing Techniques

Time: 13:50 - 15:30, Wednesday, January 18, 2017
Location: Room 105
Chairs: Seokhyeong Kang (UNIST, Republic of Korea), Wai-Kei Mak (National Tsing Hua Univ., Taiwan)

5C-2 (Time: 14:15 - 14:40)
Floorplan and Placement Methodology for Improved Energy Reduction in Stacked Power-Domain Design 444
*Kristof Blutman, Hamed Fatemi (NXP Semiconductors, Netherlands), Andrew B. Kahng (Univ. of California, San Diego, U.S.A.), Ajay Kapoor (NXP Semiconductors, Netherlands), Jiajia Li (Univ. of California, San Diego, U.S.A.), José Pineda de Gyvez (NXP Semiconductors, U.S.A.)

5C-3 (Time: 14:40 - 15:05)
An Effective Legalization Algorithm for Mixed-Cell-Height Standard Cells 450
*Chao-Hung Wang, Yen-Yi Wu (National Taiwan Univ., Taiwan), Jianli Chen (Fuzhou Univ., China), Yao-Wen Chang, Sy-Yen Kuo (National Taiwan Univ., Taiwan), Wenxing Zhu, Genghua Fan (Fuzhou Univ., China)

5C-4 (Time: 15:05 - 15:30)
Delay-driven Layer Assignment for Advanced Technology Nodes 456
Szu-Yuan Han (National Tsing Hua Univ., Taiwan), Wen-Hao Liu (Cadence Design Systems, U.S.A.), Rickard Ewetz (Univ. of Central Florida, U.S.A.), Cheng-Kok Koh (Purdue Univ., U.S.A.), Kai-Yuan Chao (Intel, U.S.A.), *Ting-Chi Wang (National Tsing Hua Univ., Taiwan)

6S (Designers' Forum) Panel Discussion: What is future AI we will create ? - "Doraemon" or "Terminator" ? -

Time: 15:50 - 17:30, Wednesday, January 18, 2017
Location: Room 103
Organizers: Hiroe Iwasaki (NTT, Japan), Sunao Torii (ExaScaler, Japan), Akihiko Inoue (Panasonic, Japan), Chair: Satoshi Kurihara (Univ. of Electro-Communications, Japan)

6S-1 (Time: 15:50 - 17:30)
(Panel Discussion) What is future AI we will create? - "Doraemon" or "Terminator" ? -
Panelists: Hiroshi Yamakawa (dwango, Japan), Luca Rigazio (Panasonic Silicon Valley Lab, Japan), Takeshi Yamada (NTT, Japan), Akira Naruse (NVIDIA, Japan), Shinji Nakadai (NEC, Japan)

6A Recent Advances in Circuit Simulation and Optimization

Time: 15:50 - 17:30, Wednesday, January 18, 2017
Location: Room 102
Chairs: Markus Olbrich (Univ. of Hannover, Germany), Ibrahim (Abe) Elfadel (Masdar Inst. of Science and Tech., United Arab Emirates)

6A-1 (Time: 15:50 - 16:15)
STEAM: Spline-based Tables for Efficient and Accurate Device Modelling 463
*Archit Gupta, Tianshi Wang, Ahmet Gokcen Mahmutoglu, Jaijeet Roychowdhury (UC Berkeley, U.S.A.)

6A-2 (Time: 16:15 - 16:40)
A Time Domain Behavioral Model for Oscillators Considering Flicker Noise 469
*Hui Zhang, Bo Wang (Peking Univ. Shenzhen Graduate School, China)

6A-3 (Time: 16:40 - 17:05)
Parasitic-Aware GP-based Many-objective Sizing Methodology for Analog and RF Integrated Circuits 475
*Tuotian Liao, Lihong Zhang (Memorial Univ. of Newfoundland, Canada)

6A-4 (Time: 17:05 - 17:30)
High-Speed Stochastic Circuits Using Synchronous Analog Pulses 481
*M. Hassan Najafi, David J. Lilja (Univ. of Minnesota, twin cities, U.S.A.)

6B Application-Aware Embedded Architecture Design

Time: 15:50 - 17:30, Wednesday, January 18, 2017
Location: Room 104
Chairs: Chun-Yi Lee (NTHU, Taiwan), Shao-Yun Fang (National Taiwan Univ. of Science and Tech., Taiwan)

6B-1 (Time: 15:50 - 16:15)
Throughput Optimization for Streaming Applications on CPU-FPGA Heterogeneous Systems 488
*Xuechao Wei, Yun Liang (Peking Univ., China), Tao Wang (Peking Univ./PKU-UCLA Joint Research Institute in Science and Engineering, China), Songwu Lu, Jason Cong (Peking Univ./UCLA/PKU-UCLA Joint Research Institute in Science and Engineering, U.S.A.)

6B-2 (Time: 16:15 - 16:40)
Dark Silicon-Aware Hardware-Software Collaborated Design for Heterogeneous Many-Core Systems 494
Lei Yang, *Weichen Liu (Chongqing Univ., China), Nan Guan (Hong Kong Polytechnic Univ., Hong Kong), Mengquan Li, Peng Chen, Edwin H. M. Sha (Chongqing Univ., China)

6C Advances in Microfluidic Biochips

Time: 15:50 - 17:30, Wednesday, January 18, 2017
Location: Room 105
Chairs: Juinn-Dar Huang (National Chiao Tung Univ., Taiwan), Weikang Qian (Shanghai Jiao Tong Univ., China)

3K Keynote III

Time: 9:00 - 9:50, Thursday, January 19, 2017
Location: International Conference Room
Chair: Kazutoshi Kobayashi (Kyoto Inst. of Tech., Japan)

7S (Special Session) When Backend Meets Frontend: Cross-Layer Design & Optimization for System Robustness

Time: 10:15 - 12:15, Thursday, January 19, 2017
Location: Room 103
Organizers/Chairs: Cheng Zhuo (Zhejiang Univ.), Masanori Hashimoto (Osaka Univ., Japan)

7A NVM/Flash: From Advanced Storage Design to Emerging Applications

Time: 10:15 - 12:20, Thursday, January 19, 2017
Location: Room 102
Chairs: Sungjoo Yoo (Seoul National Univ., Republic of Korea), Ya-Shu Chen (National Taiwan Univ. of Science and Tech., Taiwan)

7B Hardware Diversity and Hardware Trojan

Time: 10:15 - 12:20, Thursday, January 19, 2017
Location: Room 104
Chairs: Wujie Wen (Florida International Univ., U.S.A.), Chip Hong Chang (Nanyang Technological Univ., Singapore)

7C Hardware Accelerator for Emerging Applications

Time: 10:15 - 12:20, Thursday, January 19, 2017
Location: Room 105
Chairs: Tohru Ishihara (Kyoto Univ., Japan), Yongpan Liu (Tsinghua Univ., China)

8S (Designers' Forum) Advanced Automotive Security

Time: 13:50 - 15:30, Thursday, January 19, 2017
Location: Room 103
Organizers: Shinichi Shibahara (Renesas System Design, Japan), Akihiko Inoue (Panasonic, Japan), Chair: Shinichi Shibahara (Renesas System Design, Japan)

8S-2 (Time: 14:15 - 14:40)
(Invited Paper) An Embedded Hardware Security Module for Automotive ECUs
Yasuhisa Shimazaki (Renesas Electronics, Japan)

8S-3 (Time: 14:40 - 15:05)
(Invited Paper) Security Hardware for Automotive Applications
Takeshi Fujino (Ritsumeikan Univ., Japan)

8S-4 (Time: 15:05 - 15:30)
(Invited Paper) Physical and Logical Attacks against LSI Chips and Their Countermeasures
Shinichi Kawamura (Toshiba, Japan)

8A Scheduling, Resource Management, and Simulation for Multi-Core Systems

Time: 13:50 - 15:30, Thursday, January 19, 2017
Location: Room 102
Chairs: Yuko Hara-Azumi (Tokyo Inst. of Tech., Japan), Yi Wang (Shenzhen Univ., China)

8B Machine Learning: Acceleration and Application

Time: 13:50 - 15:30, Thursday, January 19, 2017
Location: Room 104
Chairs: Weichen Liu (Chongqing Univ., China), Nan Guan (Hong Kong Polytechnic Univ., Hong Kong)

8C Design Automation and Modeling for Emerging Technologies

Time: 13:50 - 15:30, Thursday, January 19, 2017
Location: Room 105
Chair: Yiran Chen (Univ. of Pittsburgh, U.S.A.)

8C-1 (Time: 13:50 - 14:15)
Reservoir and Mixer Constrained Scheduling for Sample Preparation on Digital Microfluidic Biochips 702
*Varsha Agarwal, Ananya Singla (Indian Inst. of Tech. Roorkee, India), Mahammad Samiuddin (Indian Inst. of Tech. Kharagpur, India), Sudip Roy (Indian Inst. of Tech. Roorkee, India), Tsung-Yi Ho (National Tsing Hua Univ., Taiwan), Indranil Sengupta (Indian Inst. of Tech. Kharagpur, India), Bhargab B. Bhattacharya (Indian Statistical Institute Kolkata, India)

8C-2 (Time: 14:15 - 14:40)
Exact Routing for Micro-Electrode-Dot-Array Digital Microfluidic Biochips 708
*Oliver Keszocze (Univ. of Bremen, Germany), Zipeng Li (Duke Univ., U.S.A.), Andreas Grimmer, Robert Wille (Johannes Kepler Univ., Austria), Krishnendu Chakrabarty (Duke Univ., U.S.A.), Rolf Drechsler (Univ. of Bremen and DFKI GmbH, Germany)

8C-3 (Time: 14:40 - 15:05)
Majority Logic Circuits Optimisation by Node Merging 714
Chun-Che Chung (National Tsing Hua Univ., Taiwan), Yung-Chih Chen (Yuan Ze Univ., Taiwan), Chun-Yao Wang, *Chia-Cheng Wu (National Tsing Hua Univ., Taiwan)

8C-4 (Time: 15:05 - 15:30)
A Statistical STT-RAM Retention Model for Fast Memory Subsystem Designs 720
Zihao Liu, *Wujie Wen (Florida International Univ., U.S.A.), Lei Jiang (Indiana Univ. Bloomington, U.S.A.), Yier Jin (Univ. of Central Florida, U.S.A.), Gang Quan (Florida International Univ., U.S.A.)

9S (Designers' Forum) Advanced Image Sensing and Processing

Time: 15:50 - 17:30, Thursday, January 19, 2017
Location: Room 103
Organizers: Yusuke Oike (Sony Semiconductor Solutions, Japan), Masaitsu Nakajima (Socionext, Japan), Yusuke Oike (Sony Semiconductor Solutions, Japan)

9S-1 (Time: 15:50 - 16:15)
(Invited Paper) An APS-H-Size 250Mpixel CMOS Image Sensor Using Column Single-Slope ADCs with Dual-Gain Amplifiers
Hirofumi Totsuka (Canon, Japan)

9S-2 (Time: 16:15 - 16:40)
(Invited Paper) A 1/1.7-inch 20Mpixel Back-Illuminated Stacked CMOS Image Sensor
Chihiro Okada (Sony Semiconductor Solutions, Japan)

9S-3 (Time: 16:40 - 17:05)
(Invited Paper) Emerging Applications Based on High-speed Computational Vision
Yoshihiro Watanabe (Univ. of Tokyo, Japan)

9S-4 (Time: 17:05 - 17:30)
(Invited Paper) Acceleration of Partial Image Matching on FPGA Platforms Using OpenCL
Noboru Yoneoka (Fujitsu Labs., Japan)

9A New Directions in Networks on Chip

Time: 15:50 - 17:30, Thursday, January 19, 2017
Location: Room 102
Chair: Kun-Chih Chen (National Sun Yat-Sen Univ., Taiwan)

9A-1 (Time: 15:50 - 16:15)
DLPS: Dynamic Laser Power Scaling for Optical Network-on-Chip 726
*Fan Lan (Zhejiang Univ., China), Rui Wu, Chong Zhang (Univ. of Californis, Santa Barbara, U.S.A.), Yun Pan (Zhejiang Univ., China), Kwang-ting Cheng (Univ. of Californis, Santa Barbara, U.S.A.)

9A-2 (Time: 16:15 - 16:40)
Adaptive Load Distribution in Mixed-Critical Networks-On-Chip 732
*Adam Kostrzewa, Sebastian Tobuschat, Leonardo Ecco, Rolf Ernst (TU Braunschweig, Germany)

9A-3 (Time: 16:40 - 17:05)
BoDNoC: Providing Bandwidth-on-Demand Interconnection for Multi-Granularity Memory Systems 738
*Shiqi Lian, Ying Wang, Yinhe Han, Xiaowei Li (Chinese Academy of Sciences, China)

9B Memory Architecture: Now and Future

Time: 15:50 - 17:30, Thursday, January 19, 2017
Location: Room 104
Chairs: Hyung Gyu Lee (Daegu Univ., Republic of Korea), Shimpei Sato (Tokyo Inst. of Tech., Japan)

9C Intelligent Computing with Memristor Technologies

Time: 15:50 - 17:30, Thursday, January 19, 2017
Location: Room 105
Chair: Yuan-Hao Chang (Academia Sinica, Taiwan)

Supporter's Exhibition

Supporter's exhibition is held by six companies which support ASP-DAC 2017 and have exhibition booths. The supporter's exhibition is presented at International Conference Hall 1F Lobby from January 17 through January 19.

Exhibit Hours: **10:00 – 17:30, January 17 / 10:00 – 17:30, January 18 / 10:00 – 16:00, January 19**
Location: **1F Lobby**

Baum Co.	Baum is an electronic design automation (EDA) company specialized in automatic generation of fast high-level power models. Baum's ground-breaking automatic high-level power modeling technology enables tens to hundreds of times faster power analysis than conventional power analysis technology. Baum's power models can be used at various design abstraction levels including electronic system level (ESL), register-transfer level (RTL), and gate-level. Automatic generation of fast and accurate power models from the digital circuit descriptions at low-levels such as RTL or gate-level is essential to enable industrial practices for power-aware hardware-software partitioning. Elevating the levels of design abstractions is a history-proven strategy to push design productivity up higher. With the high-level power models, designers can quickly estimate the power hot spots and take actions to eliminate them. In addition, the power models can be implemented as a hardware intellectual property (IP) circuit that can serve as a power models for emulators or a thermal sensors for fine-grained thermal management.
Easy-Logic Technology Ltd. http://www.easylogic.hk/	Easy DataEC – The world's only Formal Verification tool for Data-Path Missing complete verifications could cost billion-dollar lost in case of errors (e.g. Intel Cougar Point bug, Pentium bug,..), thus Formal Verification is a must-do for IC designs. However, since today's EDA tools running traditional formal methods (SAT, OBDD) for Data-Path circuitries (DSP, ALU) might take exponential run time, these circuitries were often "silently" treated as "black-boxes" (e.g. "unverified points") with formal verification skipped. Improved from a 3 times ICCAD CAD contest winner technique (Complementary Coupling algorithm), the Data-EC of Easy-Logic can formally verify most industrial Arithmetic blocks within seconds or minutes. (http://ieeexplore.ieee.org/document/7428002/)
Keysight Technologies	Keysight EDA is the leading supplier of electronic design automation software for communications product design. RF and Microwave circuit, high-speed, signal integrity, device modeling, power electronics, and signal-processing design engineers accelerate the development of better products using design flows built on our device modeling, electro-thermal, electromagnetic, circuit and system design and simulation tools.
NEC Corporation http://www.nec.com/ CyberWorkBench (R) www.cyberworkbench.com	CyberWorkBench (R) is a C-based High level synthesis and verification tool suite, which allows both hardware and software designer to generate high quality RTL for ASIC and/or FPGA from their ANSI-C or SystemC program. NEC is a pioneer company of High Level Synthesis, and it succeeded to generate commercial ASICs and FPGAs since 1993. CWB can be used for both control dominated and data intensive pipeline circuits, and has unique C-level verification capability such as C source code level cycle accurate timing debugger, C level assertion checker, C and RTL cross probing, etc. For more information, visit us at (http://www.cyberworkbench.com/)
OneSpin Solutions http://www.onespin.com/	OneSpin Solutions is a pioneer of advanced formal techniques to solve practical verification challenges. The company's award winning, leading technology enables a versatile range of verification solutions. These solutions include agile design evaluation for designers, advanced, coverage-driven assertion based verification, and automated apps for a range of design verification tasks. In addition, the company provides a safety critical formal solution for high reliability applications, a SystemC/C++ capability for algorithmic analysis, and Equivalency Checking to improve FPGA quality of results. OneSpin solutions may be found at many of the leading electronics companies worldwide.
Springer Email: charles.glaser@springer.com	Springer is part of Springer Nature, which has over 8,000 employees in over 30 countries. Springer publishes a wide variety of scientific and technical book and journal content, including over 8,000 book titles per year and over 2,500 journals. Our content is distributed globally, via our online portal known as Springerlink, as well as in-print via springer.com and a variety of retail outlets, e.g., amazon.com. Our book publishing includes a variety of content types, including textbooks, professional books, research monographs, and major reference works. Since Springerlink has authorized users at over 6,000 institutions around the world, our authors' work has unparalleled global reach. We offer our authors individualized, expert relationships, throughout the lifecycle of their publishing effort. Please visit the Springer exhibit and discuss your next book with Charles Glaser, Editorial Director (charles.glaser@springer.com).

Information

Proceedings:
ASP-DAC 2017 will be producing an authority to access the download site for the conference proceedings. The site will be open on Jan. 16, 2017. Please note that neither CD-ROM nor USB memory are provided.

Banquet:
Conference registrants are invited to attend a banquet to be held on January 18, 2017. The banquet will be held from 18:00 to 20:00 at the Convention Hall A. Regular Member and Non-member Conference registrants receive a ticket to the banquet when they register at the conference. Full-time students, Designers' Forum-only registrants, and Tutorial-only registrants wishing to attend the banquet will be required to pay 5,000 yen for a ticket when they register on site.

Duty free import:
Personal effects and professional equipment can be brought into Japan duty free as long as their contents and quantities are deemed reasonable by the customs officer. You can also bring in 400 cigarettes, 500 grams of tobacco or 100 cigars; 3 bottles of alcoholic beverages; 2 ounces of perfume; and gifts and souvenirs whose total market price is less than 200,000 yen or its equivalent. There is no allowance for tobacco or alcoholic beverages for persons aged 19 years or younger. Firearms and other types of weapons, and narcotics are strictly prohibited.

Currency Exchange:
Only Japanese yen (JPY, ¥) is acceptable at regular stores and restaurants. Certain foreign currencies may be accepted at a limited number of hotels, restaurants and souvenir shops. You can buy yen at foreign exchange banks and other authorized money exchangers on presentation of your passport.

Travelers checks and credit cards:
Travelers checks are accepted only by leading banks and major hotels in principal cities, and the use of travelers checks in Japan is not as popular as in some other countries. VISA, MasterCard, Diners Club, and American Express are widely accepted at hotels, department stores, shops, restaurants and nightclubs.

Tipping:
In Japan, tips are not necessary anywhere, even at hotels and restaurants.

Electricity:
Electric voltage is uniformly 100 volts, AC, throughout Japan, but with two different cycles: 50 in Eastern Japan*, and 60 in Western Japan**. Leading hotels in major cities have two outlets of 100 and 220 volts but their sockets usually accept a two-leg plug only.
*Eastern Japan :**Tokyo, Chiba**, Yokohama, Tohoku, Hokkaido
**Western Japan :Nagoya, Osaka, Kyoto, Hiroshima, Shikoku, Kyushu

Shopping:
Shops and other sales outlets in Japan are generally open on Saturdays, Sundays and national holidays as well as weekdays from 10:00 to 20:00. Department stores, however, are closed on one weekday, differing by store, and certain specialty shops may not open on Sundays and national holidays.

Other Information:
Participants can get sightseeing information at the JTB Travel desk in the Conference site during the Conference period.

Welcome to Chiba Official Tourism Website
http://www.chiba-tour.jp/html/sight_tokatsu_en.html/
JAPAN NATIONAL TOURISM ORGANIZATION
http://www.jnto.go.jp/
NARITA AIRPORT
http://www.narita-airport.jp/en/
HANEDA AIRPORT
http://www.haneda-airport.jp/en/
GO TOKYO
http://www.gotokyo.org/en/

Author Index

D

E

F

G

H

I

J

K

L

M

N

O

P

Q

R

S

T

Z

Call for Papers
ASP-DAC 2018

http://www.aspdac.com/
January 22-25, 2018
Jeju Island, Korea

Aims of the Conference:
ASP-DAC 2018 is the 23rd annual international conference on VLSI design automation in Asia and South Pacific regions, one of the most active regions of design and fabrication of silicon chips in the world. The conference aims at providing the Asian and South Pacific CAD/DA and Design community with opportunities of presenting recent advances and with forums for future directions in technologies related to Electronic Design Automation (EDA). The format of the meeting intends to cultivate and promote an instructive and productive interchange of ideas among EDA researchers/developers and system/circuit/device designers. All scientists, engineers, and students who are interested in theoretical and practical aspects of VLSI design and design automation are welcomed to ASP-DAC.

Areas of Interest:
Original papers in, but not limited to, the following areas are invited.

[1] System-Level Modeling and Design Methodology:
1.1. HW/SW co-design, co-simulation and co-verification
1.2. System-level design exploration, synthesis and optimization
1.3. Model- and component-based embedded system/software design
1.4. System-level formal verification
1.5. System-level modeling, simulation and validation tools/methodology

[2] Embedded System Architecture and Design:
2.1. Many- and multi-core SoC architecture
2.2. Reconfigurable and self-adaptive SoC architecture
2.3. IP/platform-based SoC design
2.4. Domain-specific architecture
2.5. Dependable architecture
2.6. On-chip memory architecture
2.7. Cyber physical system
2.8. Storage system architecture
2.9. Internet of things

[3] On-chip Communication and Networks-on-Chip:
3.1. On-chip communication network
3.2. Networks-on-chip
3.3. Interface and I/O design
3.4. Optical and RF on-chip communication

[4] Embedded Software:
4.1. Kernel, middleware and virtual machine
4.2. Compiler and toolchain
4.3. Real-time system
4.4. Resource allocation for heterogeneous computing platform
4.5. Storage software and application
4.6. Human-computer interface
4.7. System verification and analysis

[5] Device/Circuit-Level Modeling, Simulation and Verification:
5.1. Device/circuit/interconnect modeling and analysis
5.2. Device/circuit-level simulation tool and methodology
5.3. RTL and gate-leveling modeling, simulation and verification
5.4. Circuit-level formal verification

[6] Analog, RF and Mixed Signal:
6.1. Analog/mixed-signal/RF synthesis
6.2. Analog layout, verification and simulation techniques
6.3. Noise analysis
6.4. High-frequency electromagnetic simulation of circuit
6.5. Mixed-signal design consideration
6.6. Power-aware analog circuit/system design
6.7. Analog/mixed-signal modeling and simulation techniques
6.8. CAD for memory circuits

[7] Power Analysis, Low Power Design, and Thermal Management:
7.1. Power modeling, analysis and simulation
7.2. Low-power design and methodology
7.3. Thermal aware design
7.4. Architectural low-power design technique
7.5. Energy harvesting and battery management

[8] Logic/High-Level Synthesis and Optimization:
8.1. High-level synthesis tool and methodology
8.2. Combinational, sequential and asynchronous logic synthesis
8.3. Logic synthesis and physical design technique for FPGA
8.4. Technology mapping

[9] Physical Design:
9.1. Floorplanning, partitioning and placement
9.2. Interconnect planning and synthesis
9.3. Placement and routing optimization
9.4. Clock network synthesis
9.5. Post layout and post-silicon optimization
9.6. Package/PCB/3D-IC routing

[10] Design for Manufacturability and Reliability:
10.1. Reticle enhancement, lithography-related design and optimization
10.2. Resilience under manufacturing variation
10.3. Design for manufacturability, yield, and defect tolerance
10.4. Reliability, aging and soft error analysis
10.5. Design for reliability, aging, and robustness

[11] Timing and Signal/Power Integrity:
11.1. Deterministic/statistical timing and performance analysis and optimization
11.2. Power/ground and package modeling, analysis and optimization
11.3. Signal/power integrity, EM modeling and analysis
11.4. Extraction, TSV and package modeling
11.5. 2D/3D on-chip power delivery network analysis and optimization

[12] Test and Design for Testability:
12.1. ATPG, BIST and DFT
12.2. Fault modeling and simulation
12.3. System test and 3D IC test
12.4. Online test and fault tolerance
12.5. Memory test and repair
12.6. Analog and mixed-signal/RF test

[13] Security and Fault-Tolerant System:
13.1. Security modeling and analysis
13.2. Architecture, tool and methodology for secure hardware
13.3. Design for security and security primitive
13.4. Cross-layer security
13.5. Fault analysis, detect and tolerance

[14] Emerging Technology:
14.1. New transistor/device and process technology: spintronic, phase-change, single-electron etc.
14.2. CAD for nanotechnology, MEMS, 3D IC, quantum computing etc.

[15] Emerging Application:
15.1. Biomedical application
15.2. Big data application
15.3. Advanced multimedia application
15.4. Energy-storage/smart-grid/smart-building design and optimization
15.5. Datacenter optimization
15.6. Automotive system design and optimization
15.7. Electromobility

It is mandatory that at least one co-author per accepted paper registers the conference at the speaker's registration rate and attends the conference to present the work. ACM and IEEE reserve the right to exclude a paper from distribution after the conference (e.g., removal from ACM Digital Library and IEEE Xplore) if the paper is not presented at the conference by the author of the paper. ASP-DAC does not allow double and/or parallel submissions of similar work to any other conferences, symposia, and journals.

Submission of Papers:

Deadline for submission:	**5 PM AOE (Anywhere on earth)**	**July 7 (Fri), 2017**
Notification of acceptance:		**Sep. 11 (Mon), 2017**
Deadline for final version:	**5 PM AOE (Anywhere on earth)**	**Nov. 6 (Mon), 2017**

For detailed instructions for submission, please refer to the "Authors' Guide" at: **http://www.aspdac.com/**

ASP-DAC 2018 Chairs

General Chair:	**Youngsoo Shin (KAIST, Korea)**
Technical Program Chair:	**Atsushi Takahashi (Tokyo Institute of Technology, Japan)**
Technical Program Vice Chairs:	**Taewhan Kim (Seoul National University, Korea)**
	Tohru Ishihara (Kyoto University, Japan)

Panels, Special Sessions, and Tutorials: Suggestions and proposals are welcome and have to be addressed to the Conference Secretariat (sec@aspdac18.com) no later than July 7 (Fri), 2017.
Contact: Conference Secretariat: sec@aspdac18.com TPC Secretariat: tpc@aspdac18.com

Call for Designs

University LSI Design Contest
ASP-DAC 2018
http://www.aspdac.com/
January 22-25, 2018
Jeju Island, Korea

ASIA SOUTH PACIFIC DESIGN AUTOMATION CONFERENCE

Aims of the Contest:

As a unique feature of ASP-DAC 2018, the University LSI Design Contest will be held. The aim of the contest is to encourage education and research on VLSI design at universities and other educational organizations. We solicit designs that fit in one or more of the following categories:

(1) Designs implemented on chips in universities or other educational organizations during the last two years;
(2) Designs that report measurement results from actual implementations;
(3) Innovative design prototypes.

Excellent designs will be selected and honored by providing the opportunities for presentation in a special session at the conference. Award(s) will be given to a few outstanding designs, selected from those presented at the conference.

Areas of Design:

Application areas or types of the original LSI circuit designs include (but are not limited to):
(1) Analog, RF and Mixed-Signal Circuits, (2) Digital Signal Processors, (3) Microprocessors, (4) Custom ASIC.
Methods or technologies used for implementation include:
(a) Custom ASIC and Cell-Based LSIs, (b) Gate Arrays, (c) FPGA/PLDs.

Submission of Design Descriptions:

A camera-ready summary is requested to be prepared within 2 pages including figures, tables, and references. It is strongly recommended that measured experimental results and chip micrographs are included in the summary. Please do not submit the same paper as a regular paper.
Specification of the submission format will be available at **http://www.aspdac.com/**

Deadline for summary:	5 PM AOE (Anywhere on earth) July 7 (Fri), 2017
Notification of acceptance:	Sep. 11 (Mon), 2017
Deadline for camera-ready:	5 PM AOE (Anywhere on earth) Nov. 6 (Mon), 2017

Review:

Submitted designs will be reviewed by the Design Contest Committee through a process similar to the review process for the technical papers. The following criteria will be applied in the selection of designs:
(1) Reliability of design and implementation, (2) Quality of implementation, (3) Performance of the design,
(4) Novelty of application, algorithm, and architecture, (5) Others.
Excellent designs will be selected for presentation at a special session of the conference.

Presentation:

An author of each selected design will be required to make a short presentation at a special session of ASP-DAC 2018. It is mandatory that at least one co-author per accepted paper registers for the conference at the registration rate of speakers or full-time students. A digest of each design presented will be included in the conference proceedings.

Contact Email: udc@aspdac18.com

ASP-DAC 2018 Chairs

General Chair:	**Youngsoo Shin (KAIST, Korea)**
Technical Program Chair:	**Atsushi Takahashi (Tokyo Institute of Technology, Japan)**
Technical Program Vice Chair:	**Taewhan Kim (Seoul National University, Korea)**
	Tohru Ishihara (Kyoto University, Japan)
Design Contest Co-Chairs:	**Minkyu Je (KAIST, Korea)**
	Ik-Joon Chang (Kyung Hee University, Korea)

Prospective Sponsors: ACM SIGDA, IEEE CEDA, IEEE CASS