



# A Lifetime-aware Mapping Algorithm to Extend MTTF of Network-on-Chips

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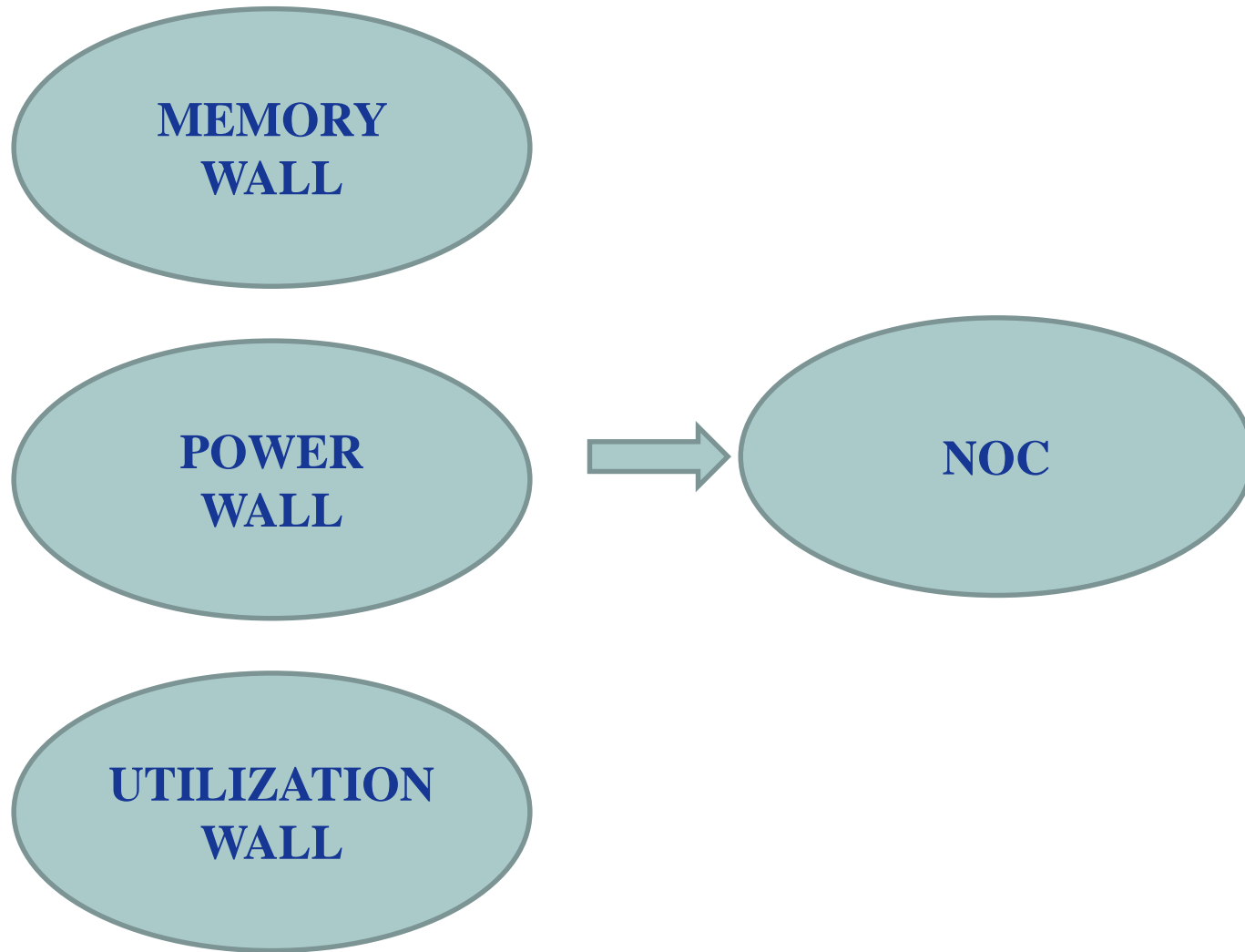
# Outline

- ❖ BACKGROUND
- ❖ MOTIVATION
- ❖ AGING EVALUATION
- ❖ THE PROPOSED ALGORITHM
- ❖ RESULT
- ❖ CONCLUSION

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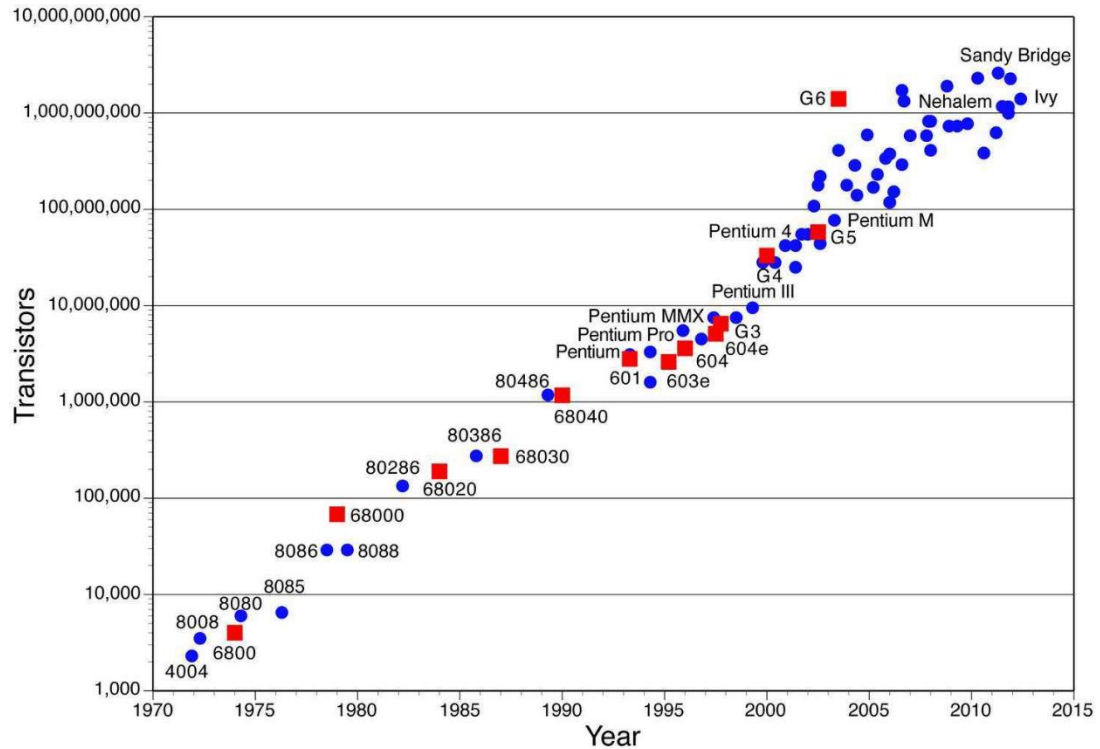
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# Background



# Background

## Moore's law



- ✓ when scaling feature sizes  $< 65$  nm, thereby making **system lifetime** a **critical issue** for all designs

# Previous Research

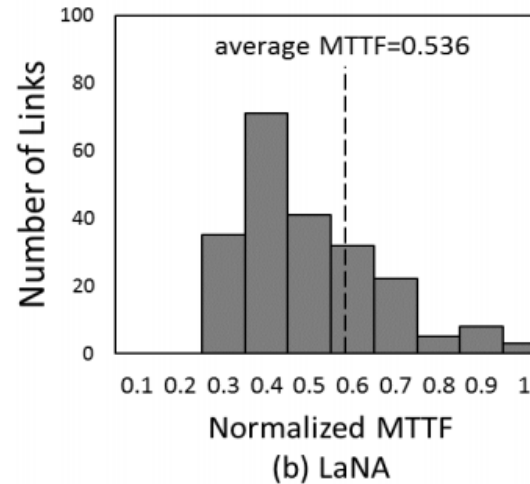
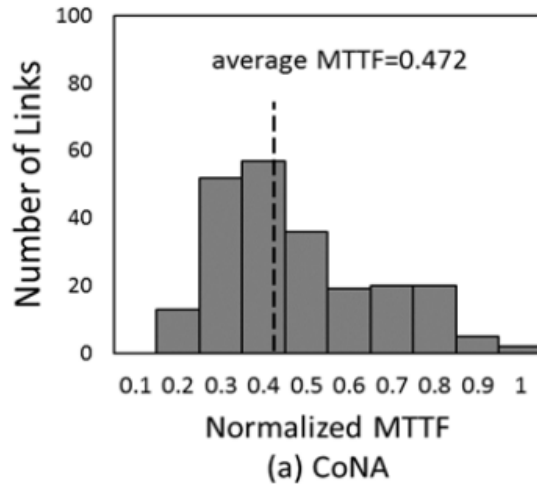
The existing aging-aware task mapping techniques suffer from the following limitations:

- 1、 the reliability of system highly depends on temperature, these methods neglect other factors of reliability such as switching activity and operating frequency
- 2、 previous works have completely ignored the role of routers/links in their reliability analysis, focusing only on the cores

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# Motivation



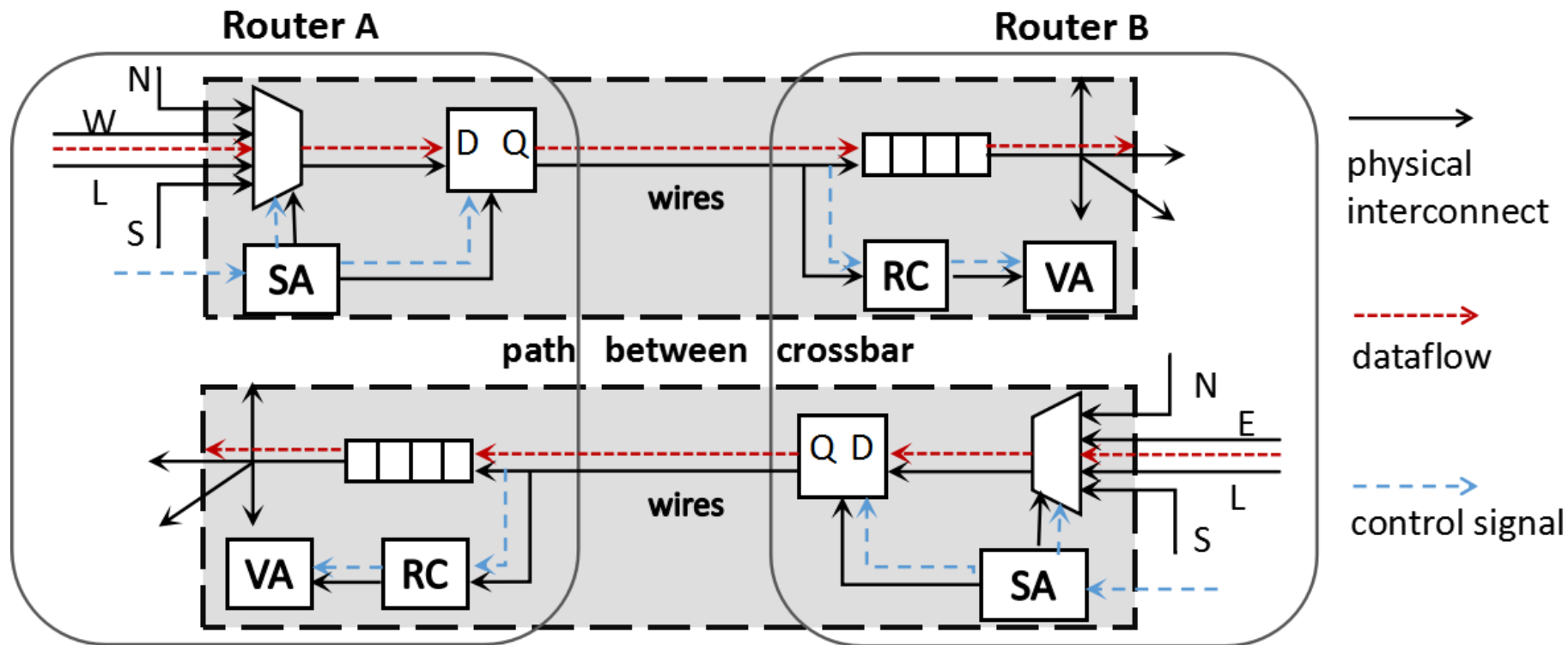
- ✓ in CoNA, the minimum MTTF is 0.2 while the maximum is 1 which means that the paths with minimum MTTF are aging 5 times faster than the paths with maximum MTTF.
- ✓ **The unbalanced MTTF distribution** would become a bottleneck for system reliability.



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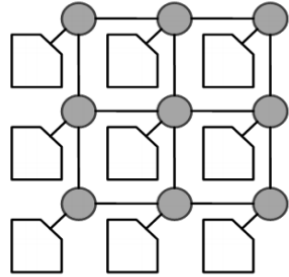
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# Aging Evaluation

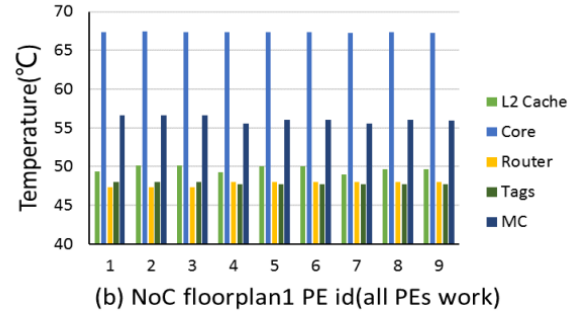


**The definition of paths between routers**

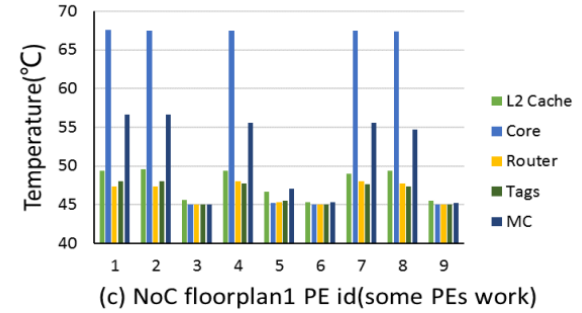
# Aging Evaluation



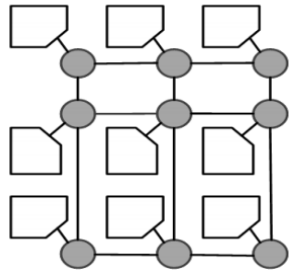
(a) NoC floorplan1



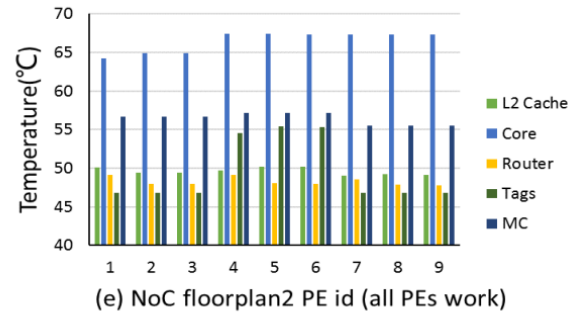
(b) NoC floorplan1 PE id (all PEs work)



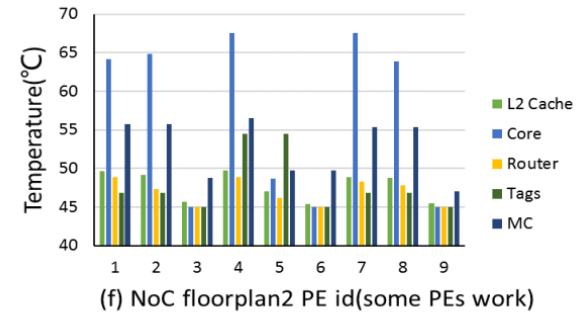
(c) NoC floorplan1 PE id (some PEs work)



(d) NoC floorplan2



(e) NoC floorplan2 PE id (all PEs work)



(f) NoC floorplan2 PE id (some PEs work)

the temperature of simulation

- ✓ This research consider **the router temperature** which is nearly a **constant value** close to 47°C.

# Aging Formulation

the aging rate:  $r(t) = j(t) \left( \frac{\exp(\frac{-Q}{kT_t})}{kT_t} \right)$

the current:  $j(t) = \frac{CV_{dd}}{WH} \times f \times p$

MTTF:  $T^f = \frac{A}{E[r(n)]}$

lifetime budget:  $LB(n) = \begin{cases} 0 & \text{if } n \text{ is } 0 \\ LB(n-1) + r_n - r(n) & \text{otherwise} \end{cases}$

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# The Proposed Algorithm

Lifetime-aware Neighborhood Allocation (LaNA)

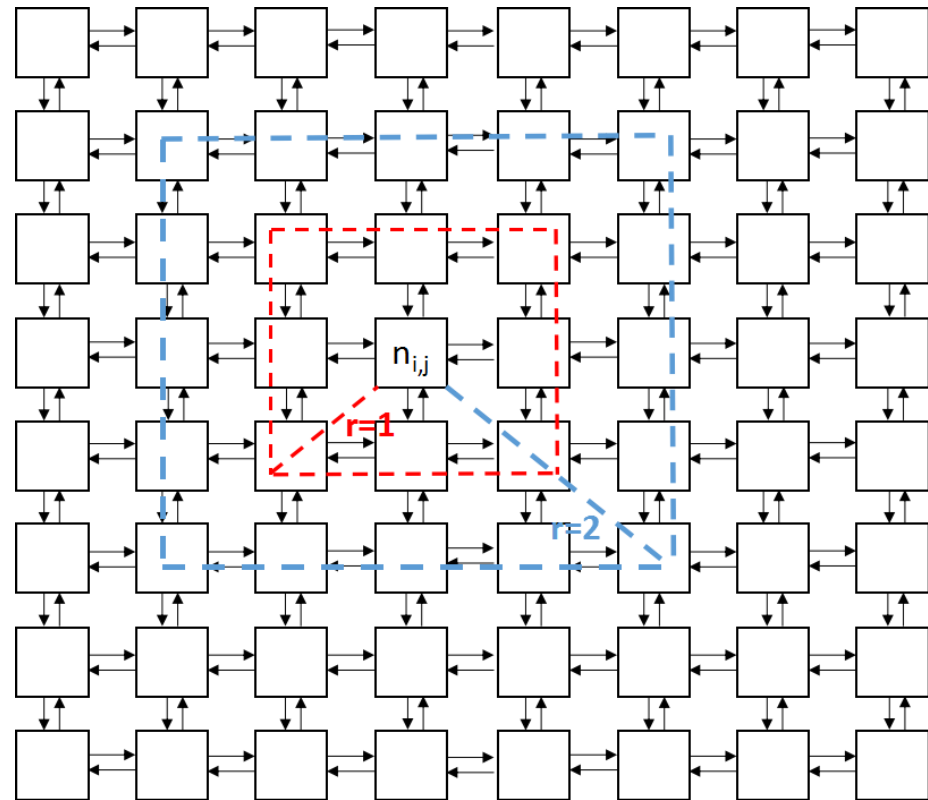
- ✓ STEP1:First-Node Selection Strategy
- ✓ STEP2:LaNA Mapping Algorithm

# The Proposed Algorithm

## ✓ STEP1:First-Node Selection Strategy

$$PLB = \sum_{i \in \text{Square}} LB_i$$

- A higher PLB indicates a longer service lifetime.
- The first node → node with the **maximum PLB** in the square area.



# The Proposed Algorithm

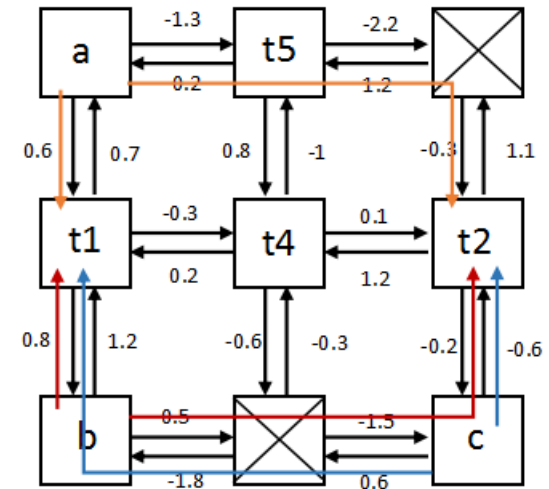
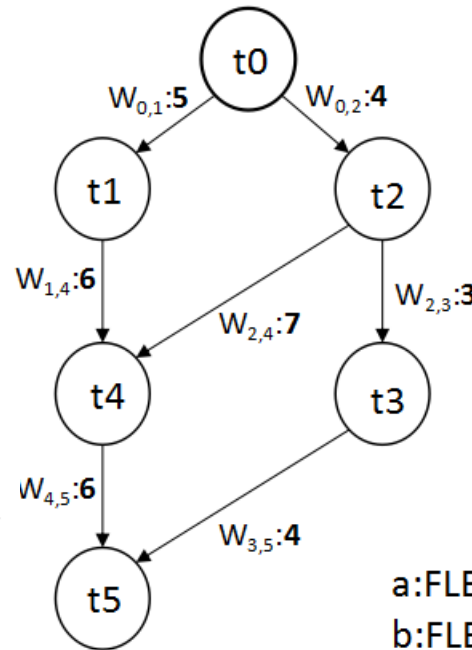
## ✓ STEP2: LaNA Mapping Algorithm

$$FLB_{s,d} = \min_{i=\{s,\dots,d\}} \{LB_i\}$$

- FLB is to select the fastest aging link of the flow

$$PELB_m = \min_{s,d} \{FLB_{s,m}, FLB_{m,d}\}$$

- A higher PELB indicates a longer service lifetime, so select the PE with maximum PELB.



a:  $FLB_{t_0,t_1} = 0.6$ ,  $FLB_{t_0,t_2} = -2.2$ ,  $PELB_a = -2.2$   
 b:  $FLB_{t_0,t_1} = 1.2$ ,  $FLB_{t_0,t_2} = -1.5$ ,  $PELB_b = -1.5$   
 c:  $FLB_{t_0,t_1} = -1.8$ ,  $FLB_{t_0,t_2} = -0.6$ ,  $PELB_c = -1.8$



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# Result

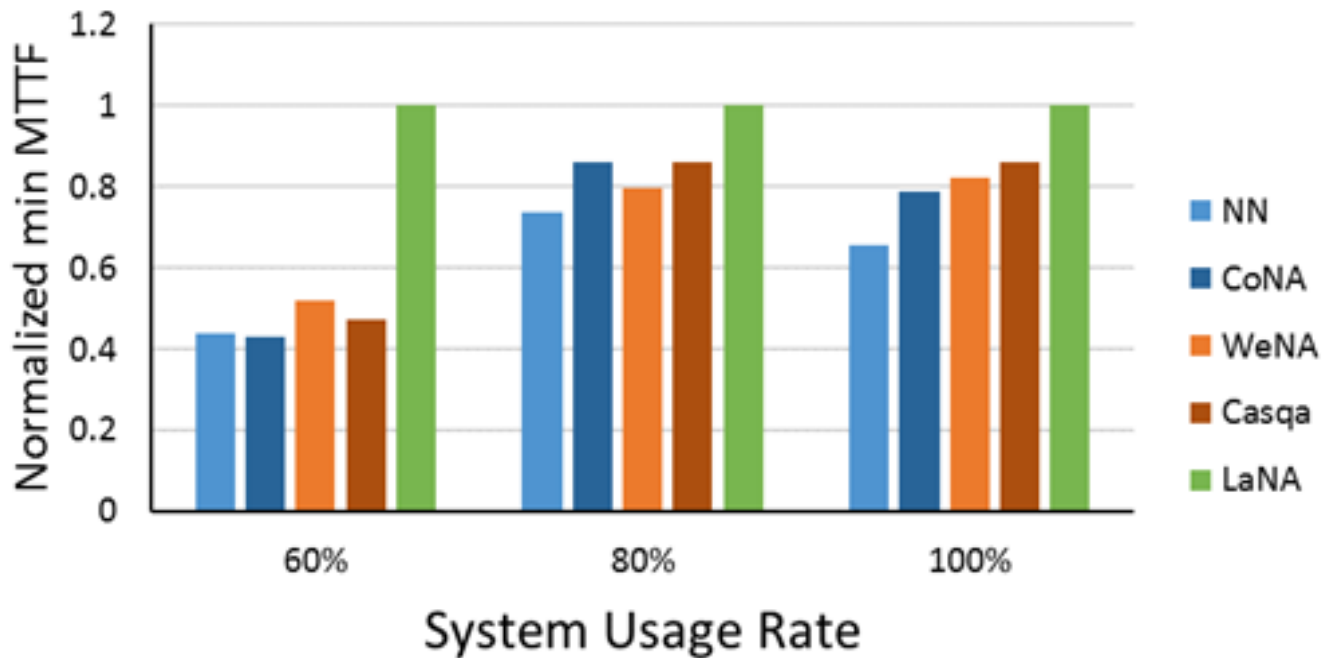
## ● Setup

- In- house many-core simulator: ESY-sim
- compare with NN,CoNA,WeNA,CASqA

Parameters	Values
NoC size	$8 \times 8$
NoC frequency	1GHz
Packet size	5 flits
Buffer size	12 flits
Routing algorithm	XY
Total time of the simulation	10 million cycles

# Result

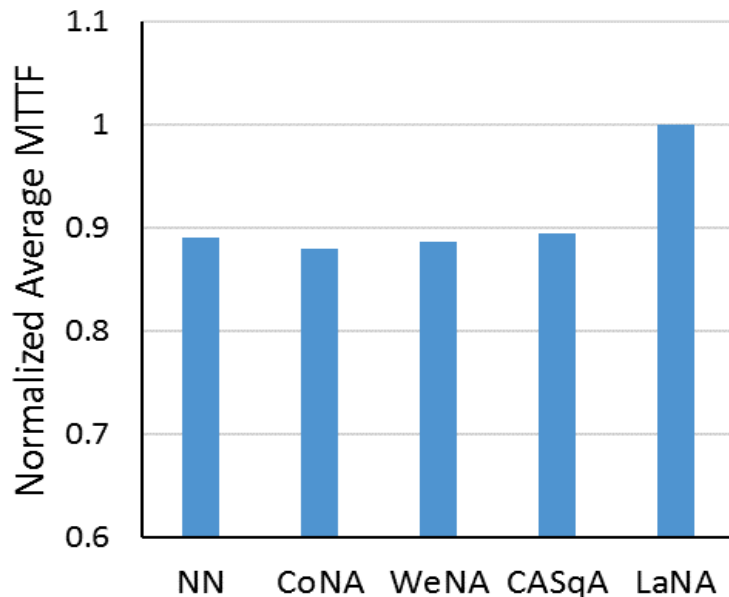
- Minimum MTTF Evaluation
  - Three configurations are as the different system utilization of 60%,80%, 100% where the unallocated cores are powered off dynamically over the execution run.



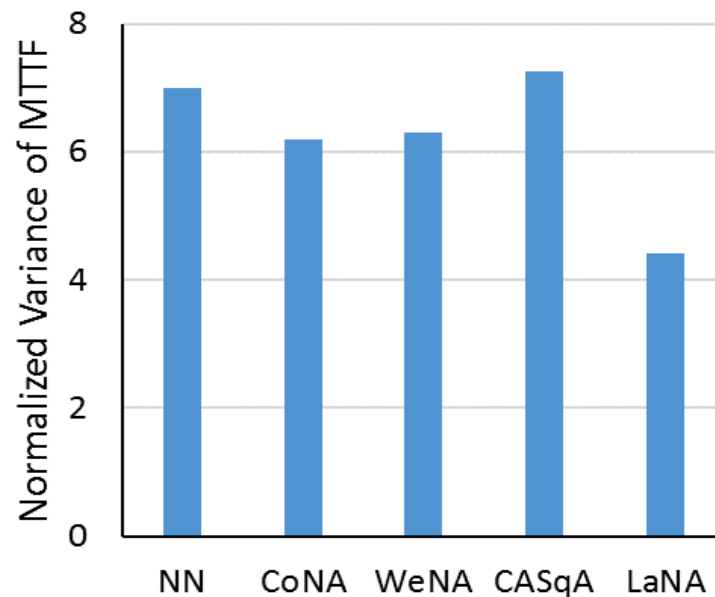
# Result

- Average MTTF Evaluation

- (a) shows the average MTTF over all NoC wires
- (b) shows the variance of MTTF over all NoC wires



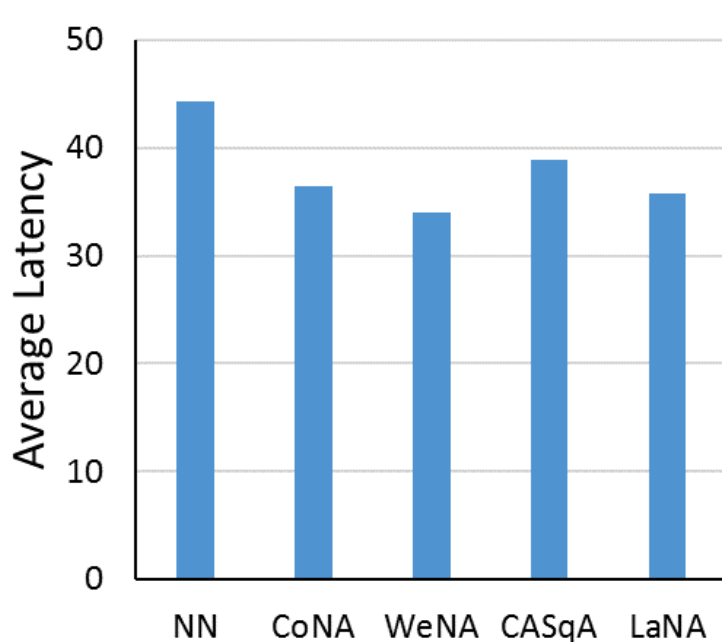
(a)



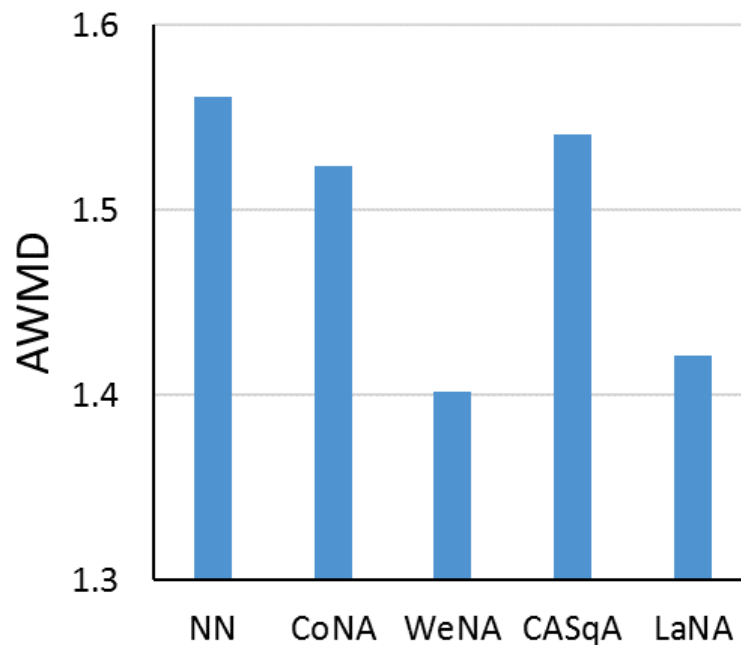
(b)

# Result

- Average MTTF Evaluation
  - (a) shows the average latency
  - (b) shows the Average Weighted Manhattan Distance(AWMD) metrics



(a)



(b)

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# Conclusion

- ✓ A mapping algorithm to improve and balance MTTF over the NoC platform
- ✓ Experimental results showed that our mapping algorithm leads to improvements on minimum, average, and variance of MTTF.

# Thank You!

ESYSim Tool QQ Group



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