MTTF-aware Design Methodology of Error Prediction Based Adaptively Voltage-scaled Circuits

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Background : Performance Variation

- Circuit speed is more sensitive to PVTA* variation

  *process, voltage, temperature, and aging

- Conventional countermeasure : Worst case design (WC)
  - Adds timing margin assuming worst PVTA conditions

Performance

Average

Performance degrades
due to timing margin

WC

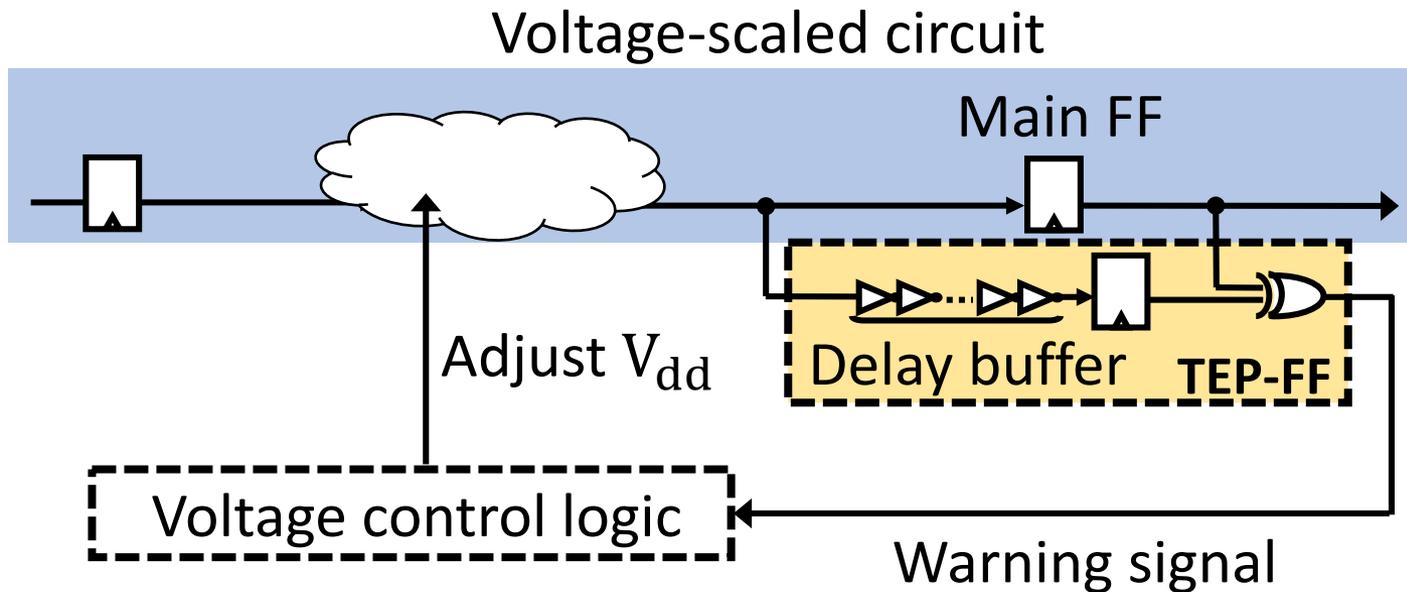Technology node
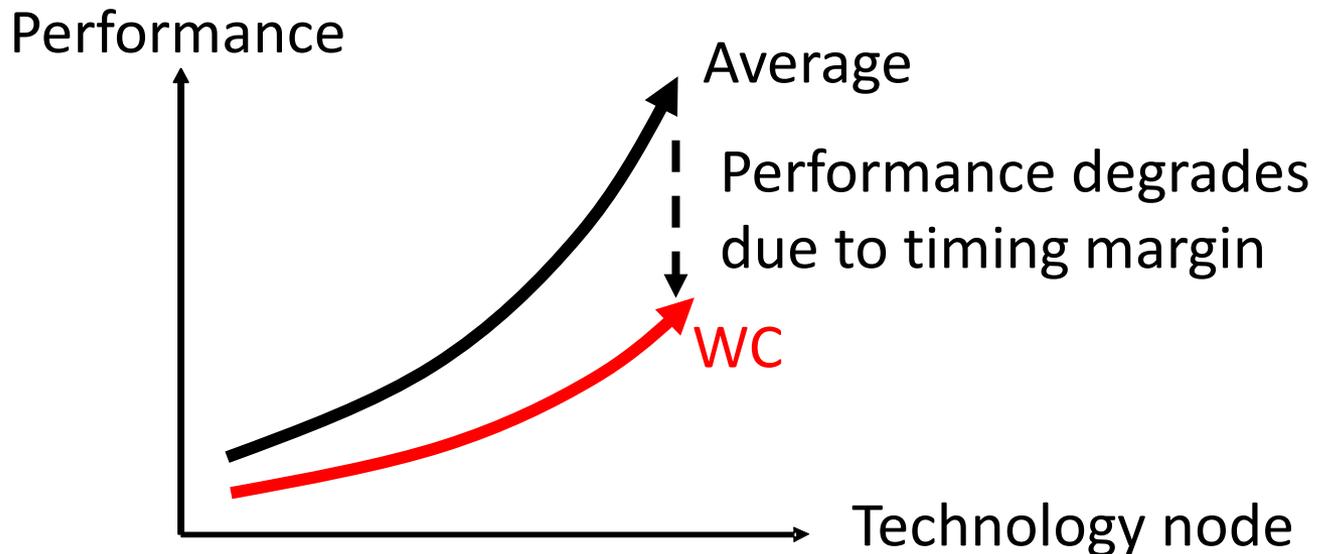
Adaptive Voltage Scaling (AVS)

- Adaptively adjust V_{dd} w/ estimating timing slack
  - Exploit PVTA margin w/ preventing error occurrence
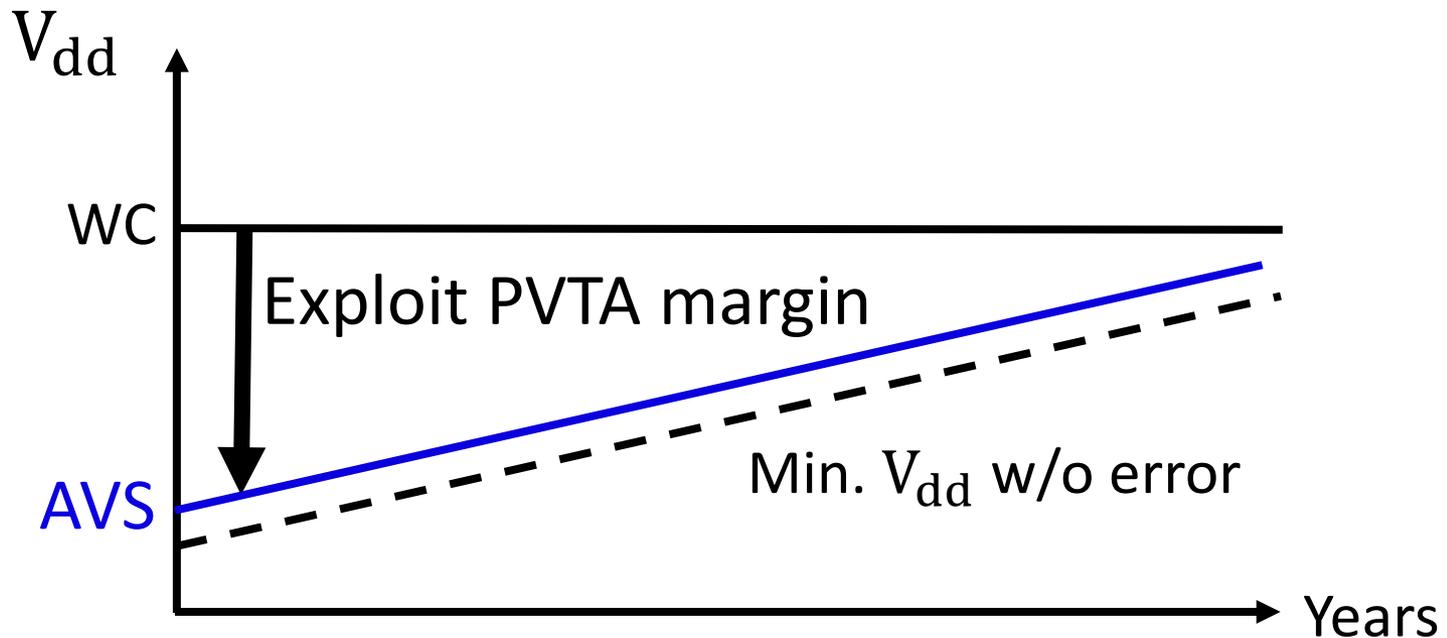
Error Prediction based AVS (EP-AVS)

- Estimate slack $\Rightarrow$ Predict error $\Rightarrow$ Adjust V_{dd}

E.g. TEP-FF (timing error predictive FF)

Voltage-scaled circuit

Main FF

Adjust V_{dd}

Delay buffer **TEP-FF**

Voltage control logic

Warning signal

**Our work focuses on EP-AVS design w/ TEP-FF.**

Conventional Works for EP-AVS

1. **Design : Only for voltage control logic**
   - Voltage-scaled circuit has many critical paths
     - ✓ Utilizing high-Vth/smaller cells for power/area savings.
   - → We may need to observe many paths w/ EP-AVS

2. **Evaluation : Not lifetime-aware**
   - Timing error may happen when long operation, e.g., years.

V_{dd}

EP-AVS

Min. V_{dd} w/o error

Supply voltage noise
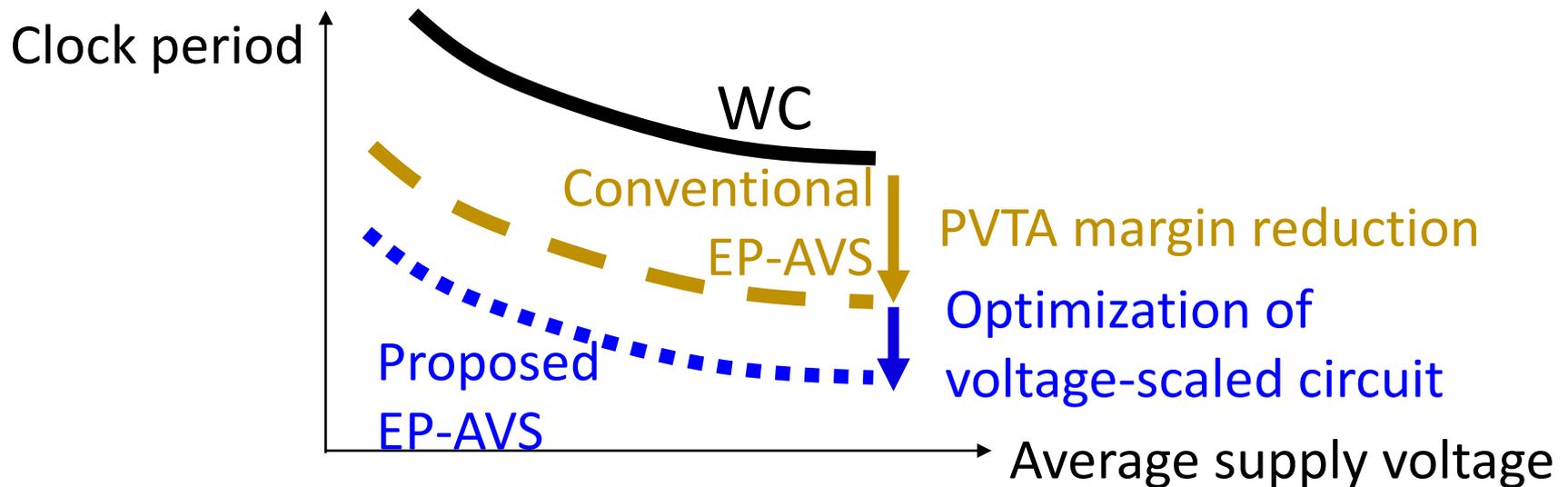
Fail of slack adjustment
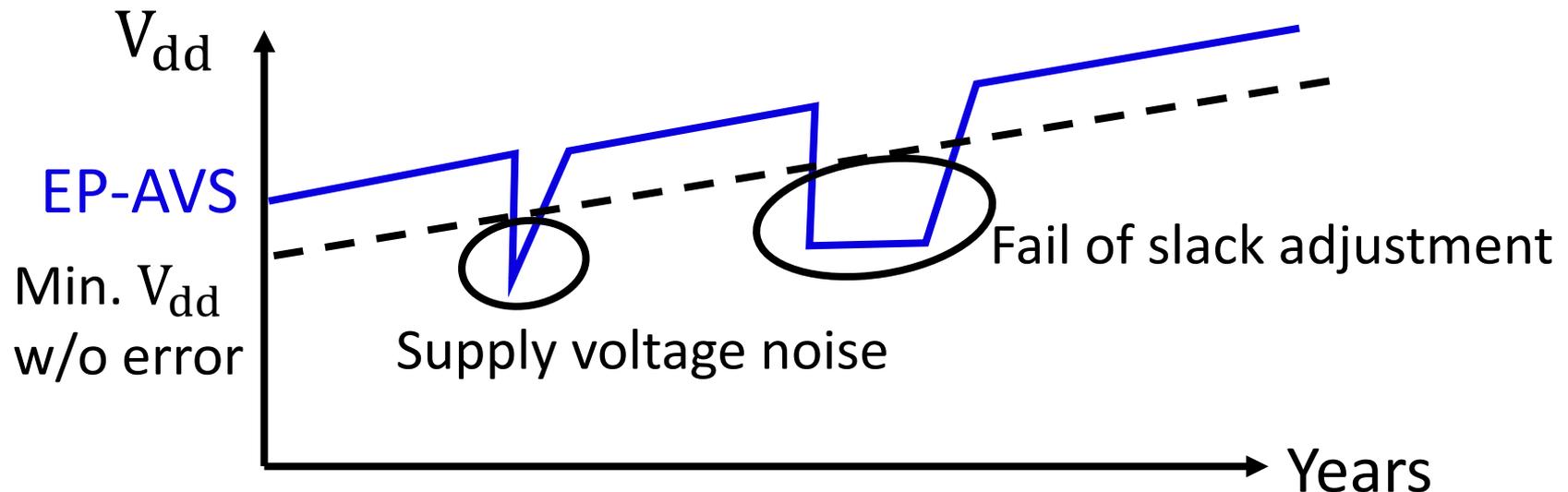
Years

Objective : MTTF-aware Design of EP-AVS

*mean time to failure

1. Design of both voltage-scaled circuit and TEP-FF.

- Extend MTTF and facilitate TEP-FF insertion.

Clock period

WC

Conventional
EP-AVS

PVTA margin reduction

Optimization of
voltage-scaled circuit

Proposed
EP-AVS

Average supply voltage

2. MTTF-aware performance evaluation

- Consider long MTTF, e.g., years.
- Use stochastic error rate estimation method [1].

[1] S. Iizuka, Y. Masuda, M. Hashimoto, and T. Onoye,
"Stochastic Timing Error Rate Estimation under Process and Temporal Variations," in *Proc. ITC*, 2015.
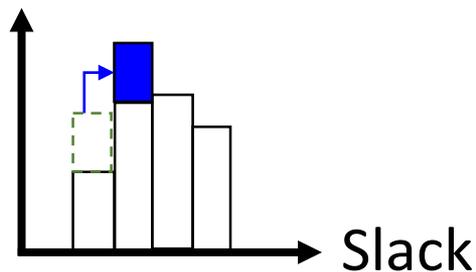
Outline

- Background and objective
- Proposed design methodology of EP-AVS
  - Design of voltage-scaled circuit under AVS
  - TEP-FF insertion to voltage-scaled circuit
- Experimental evaluation
- Conclusion

Design of Voltage-Scaled Circuit

This work applies ASA* [2] to voltage-scaled circuit.
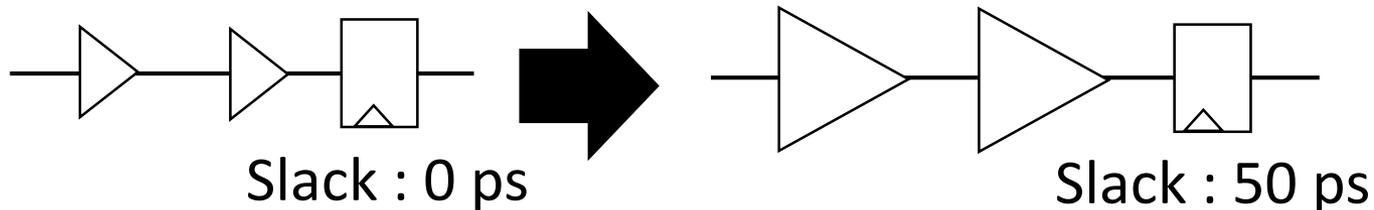
*adaptive slack assignment

Path

Slack

ASA increases setup slack of highly-activated critical paths.
- Extend MTTF
- Facilitate TEP-FF insertion

Two step implementation of ASA

Step1 : Increase setup constraint of FF

Step2 : Perform re-synthesis as ECO and restore setup constraint.
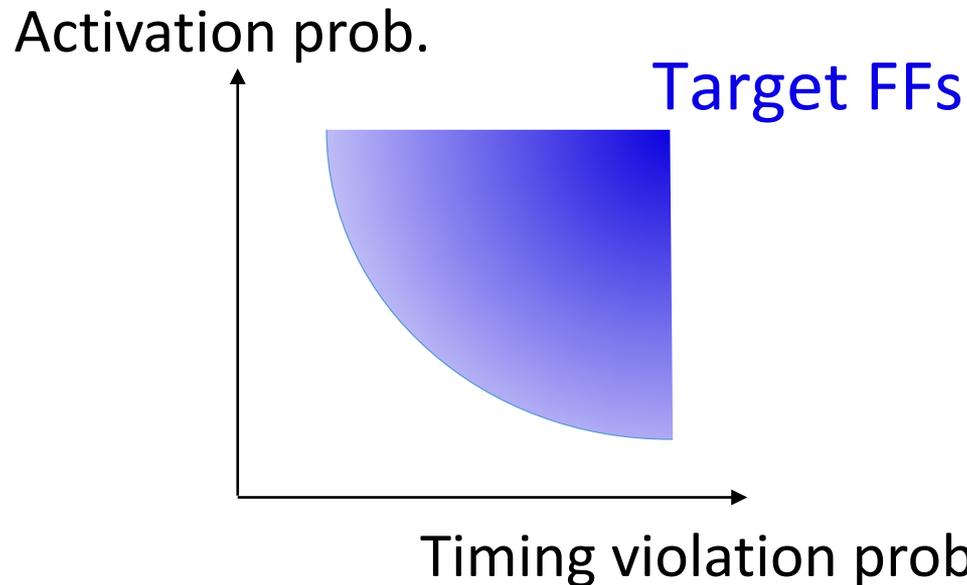

Slack : 0 ps

Slack : 50 ps

[2] Y. Masuda, M. Hashimoto, and T. Onoye,
"Critical path isolation for time-to-failure extension and lower voltage operation," in *Proc. ICCAD*, 2016.

TEP-FF Insertion

This work focuses on failure probability.

- Failure prob. = timing violation prob. $\times$ activation prob.

Activation prob.
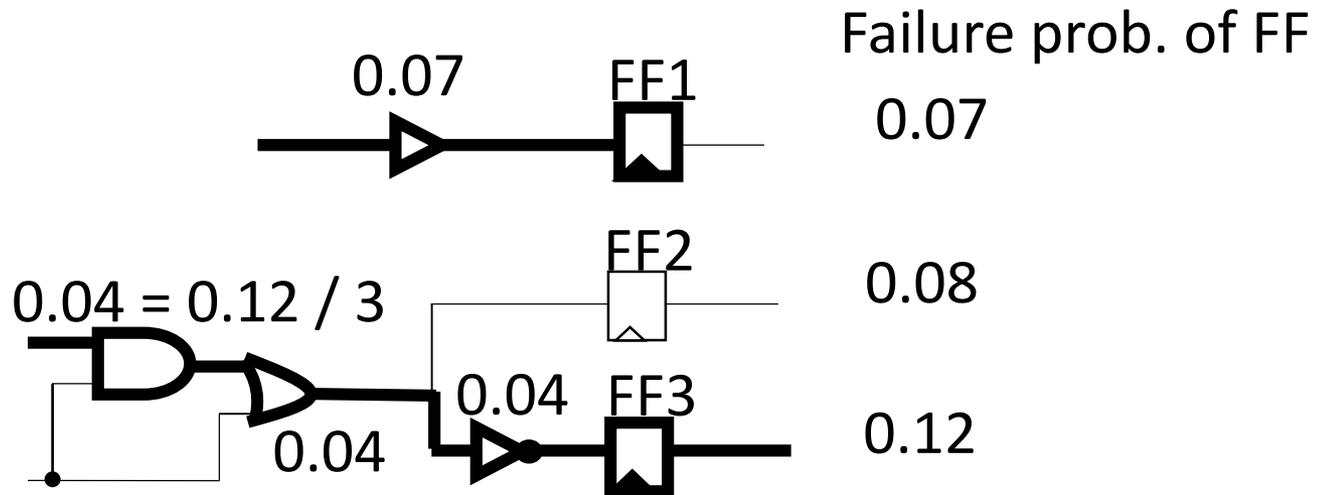
Target FFs

Timing violation prob.

- High act. prob.   : Need to predict timing errors
- Small Slack   : Help to reduce # of buffers in TEP-FF

FF Selection for TEP-FF Insertion

Proposed : Maximize sum of gate-wise failure prob.

E.g. Perform ASA to two FFs

- Proposed selects FF3 and FF1 (not FF3 and FF2)

Failure prob. of FF

0.07 → FF1 — 0.07

0.04 = 0.12 / 3

FF2 — 0.08

0.04 → 0.04 FF3 — 0.12

This work formulates FF selection problem as ILP*.

*integer linear programming

Outline

- Background and objective
- Proposed design methodology of EP-AVS
- Experimental evaluation
  - Evaluation setup
  - Performance improvement thanks to EP-AVS
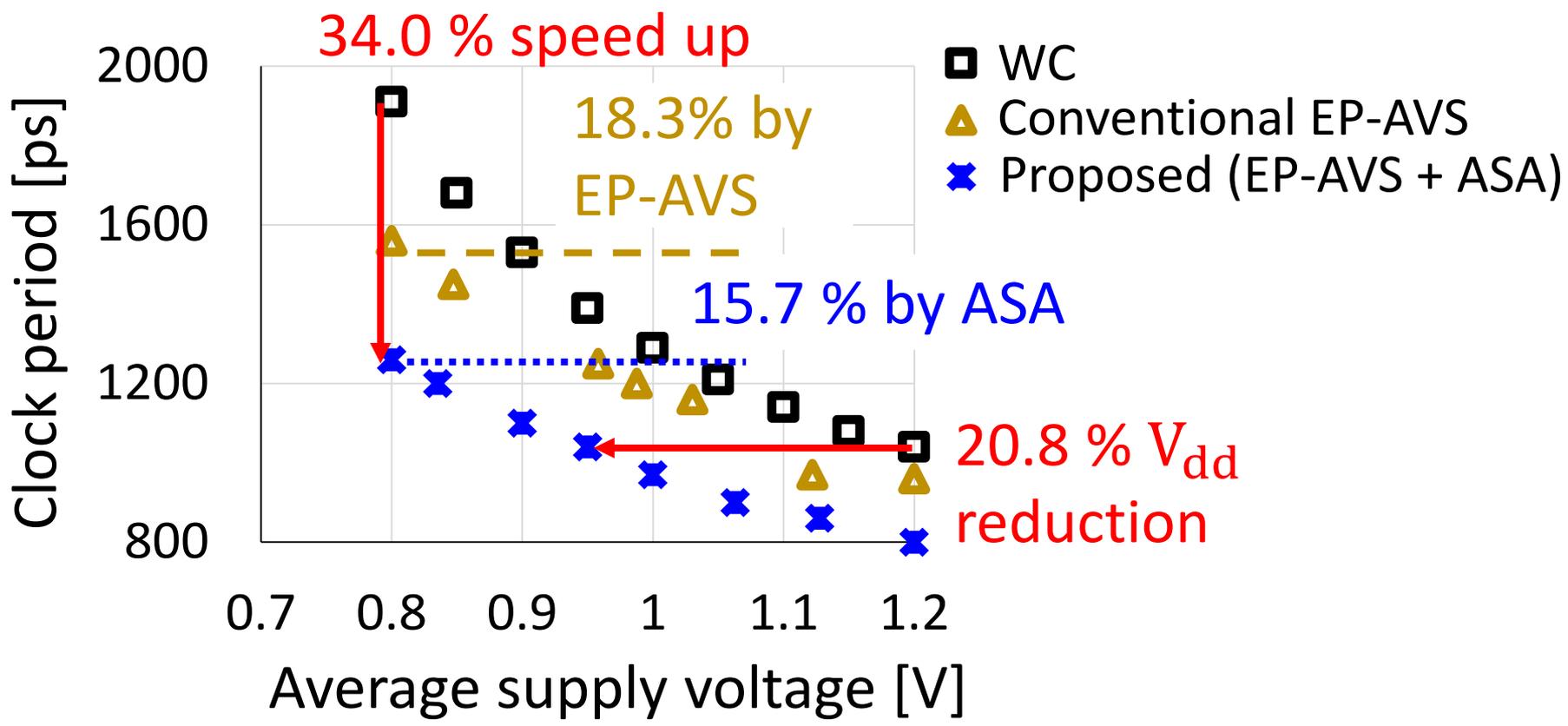 - Discussion : Effectiveness of ASA
- Conclusion

Evaluation Setup

Experiment: Evaluate average V_{dd} and MTTF w/ EP-AVS

- Target circuit : synthesized w/ 45nm NanGATE cell library
    - OpenRISC processor
        - 1.46M gates including 589K latches and 2.5K FFs
        - Workload   : SHA1, CRC, Dijkstra
    - AES (Advanced Encryption Standard) circuits
        - 17K gates including 530 FFs
        - Workload   : 1000 random test patterns
- V_{dd} w/ EP-AVS   : 1.2V to 0.8V w/ 50 mV interval
- Delay variation source
    - Supply noise, NBTI aging and manufacturing variability
- Target MTTF : 10^{17} Cycles (3.3 years in OpenRISC)
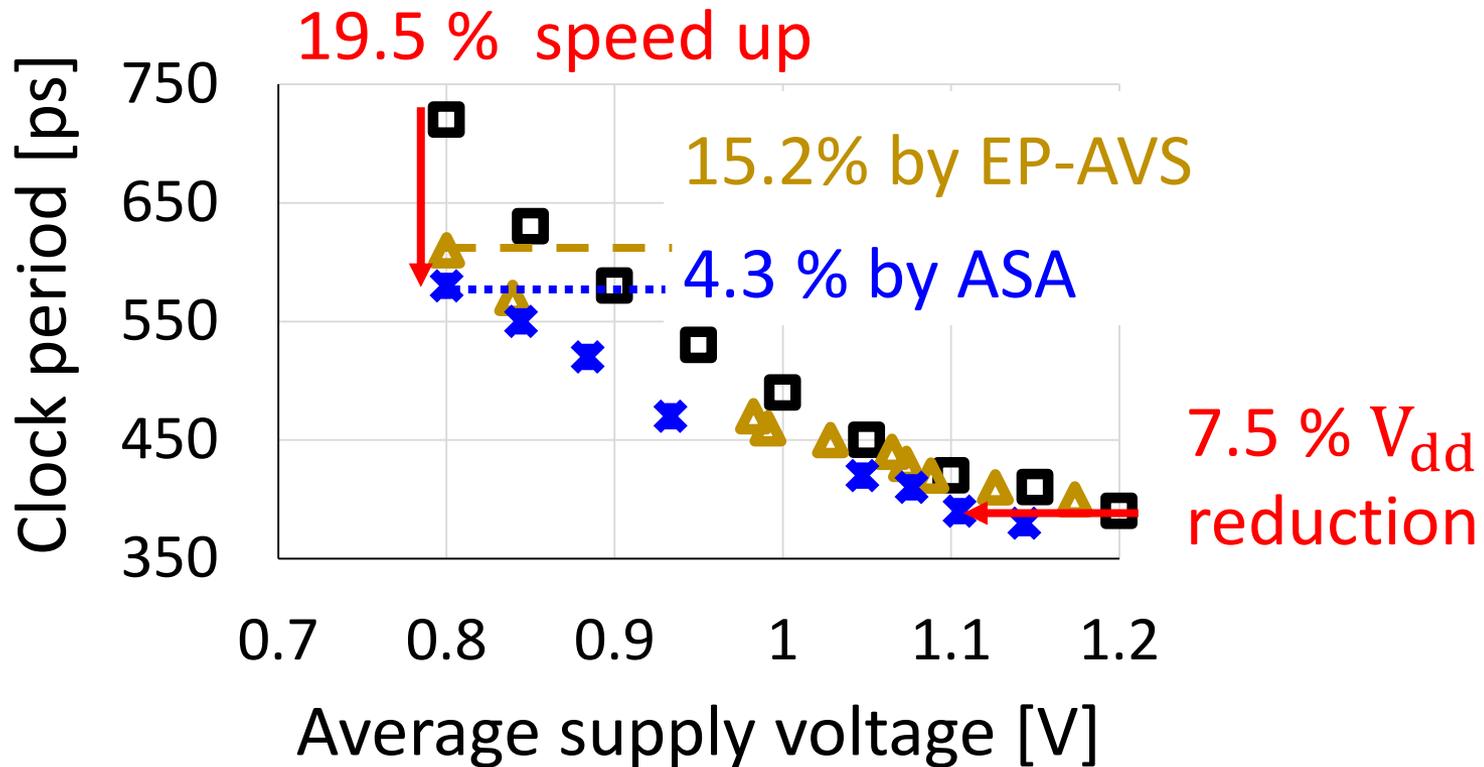
Evaluation Results (OpenRISC)

- 34.0% speed up @ supply voltage of 0.8 V
- 20.8% V_{dd} reduction @ clock period of 1040 ps

Area Overhead : 1.4% (ASA 1.0% + EP-AVS 0.4%)
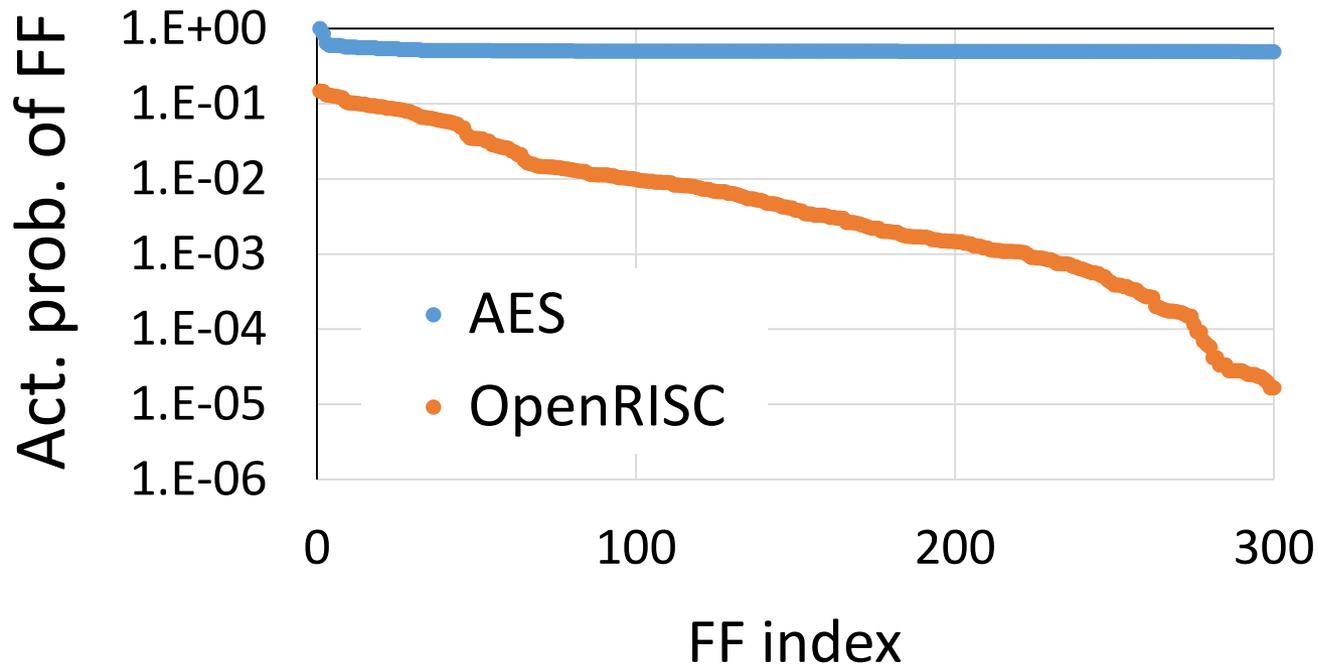
Evaluation Results (AES)

- 19.5% speed up, 7.5% V_{dd} reduction
  - ➤ Effectiveness of ASA is smaller than OpenRISC.

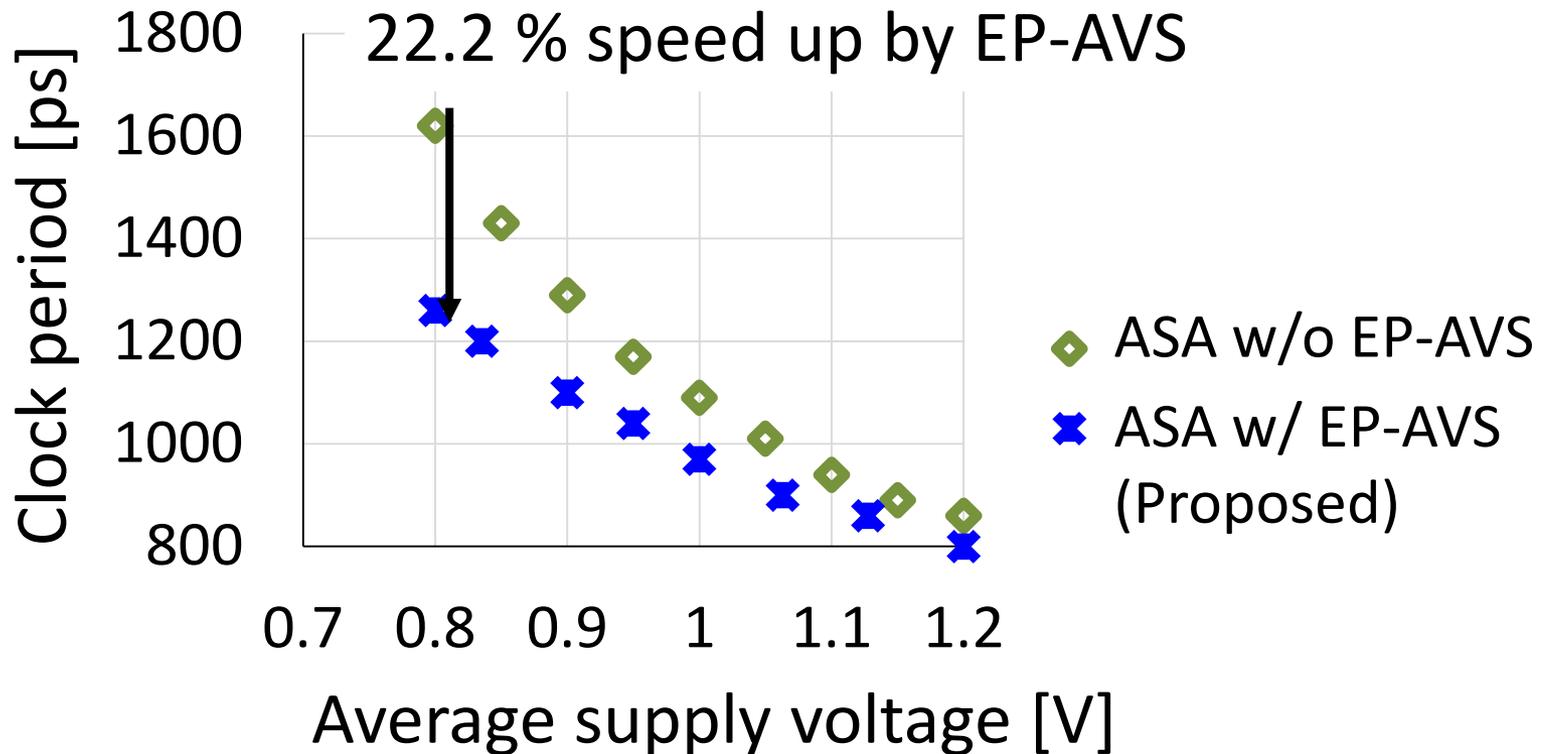Area overhead : 7.0% (ASA 6.0% + EP-AVS 1.0%)

OpenRISC and AES

- AES is highly activated circuit
  - In AES, intrinsic critical paths w/ high act. prob. exist.
- OpenRISC is more suitable to ASA

Compatibility of EP-AVS and ASA

- Even w/ ASA, EP-AVS exploits PVTA margins similarly.
  → EP-AVS and ASA are highly comparable.

22.2 % speed up by EP-AVS

ASA w/o EP-AVS

ASA w/ EP-AVS (Proposed)

Clock period [ps] vs Average supply voltage [V]

Comparison of # of Failure FFs

- ASA reduces # of failure FFs and failure prob. of FFs.
  - ➢ASA helps to facilitate TEP-FF insertion.

(a) OpenRISC

(b) AES

85% reduction

28% reduction
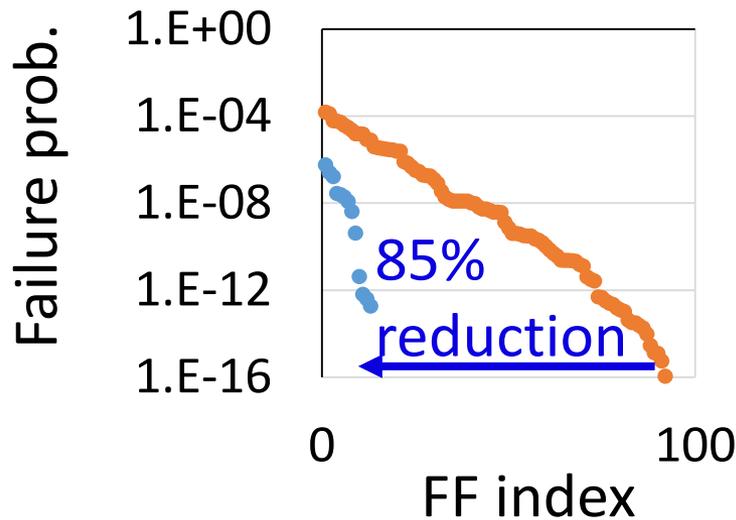
- w/o ASA
- w/ ASA

Outline
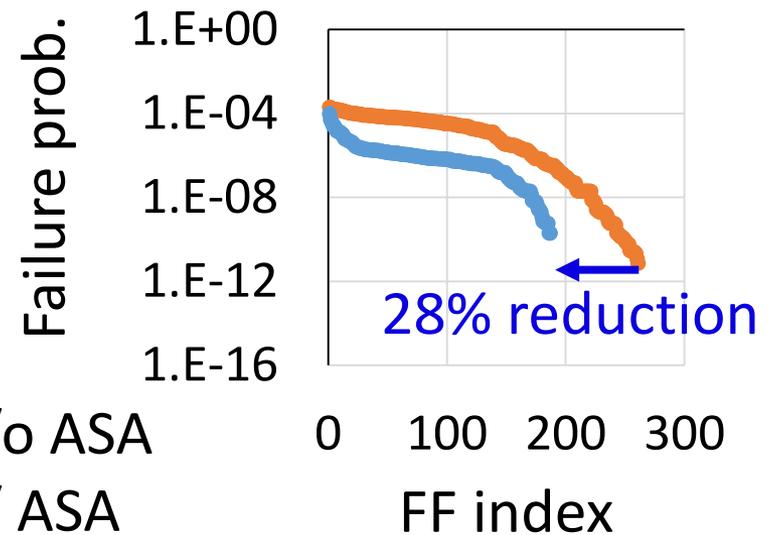
- Background and objective
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Conclusion

- Proposed MTTF-aware design methodology of EP-AVS.
  - ASA to voltage-scaled circuit.
  - Gate-wise failure prob. aware TEP-FF insertion.
  - Consideration of practical long MTTF, e.g., 3 years.

- Performance evaluation results show that
  - 20.8 % V_{dd} reduction in OpenRISC.
  - 7.5 % V_{dd} reduction in AES.

Effectiveness of TEP-FF Insertion

Compare MTTF between proposed and slack-based method

⇒ Only proposed insertion methodology achieves target MTTF.

Target : 10^{17} cycles

- Proposed
- Slack Order

MTTF [Cycle]

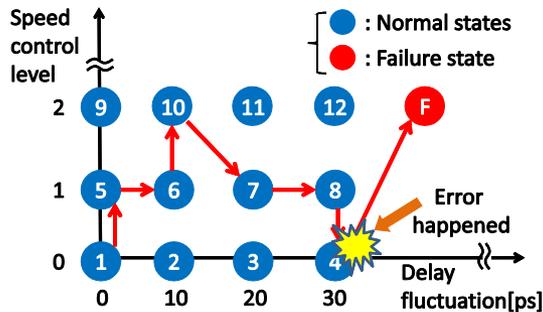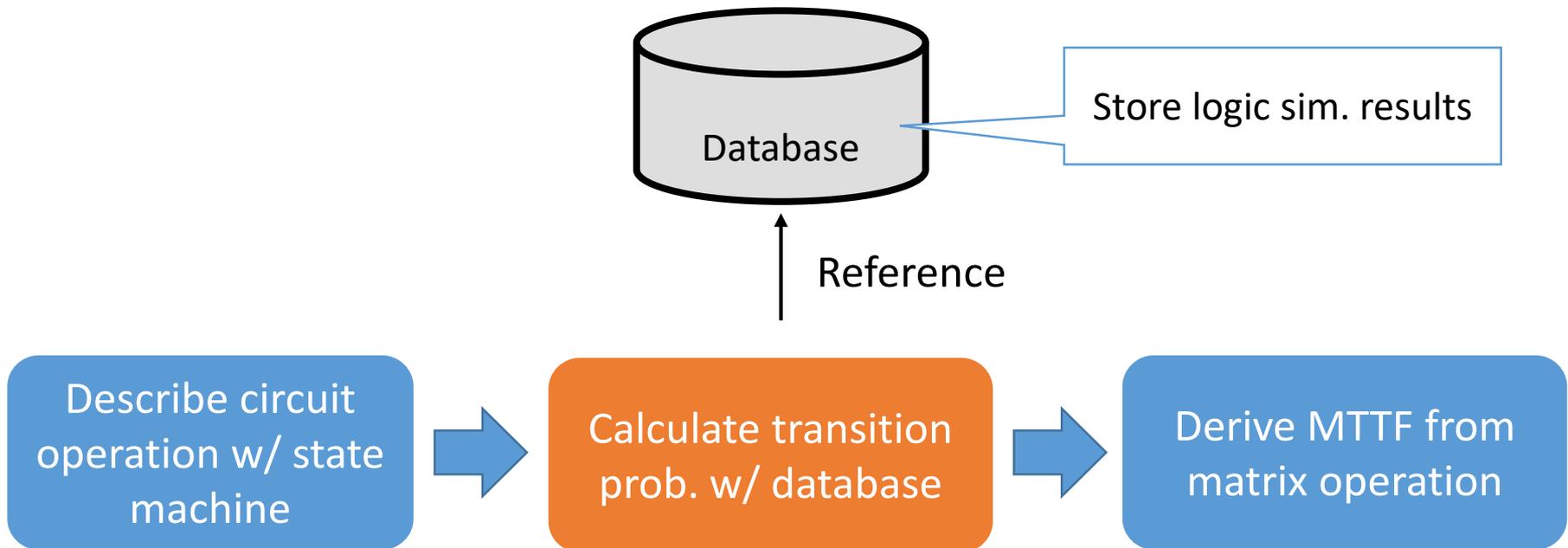Clock period [ps]
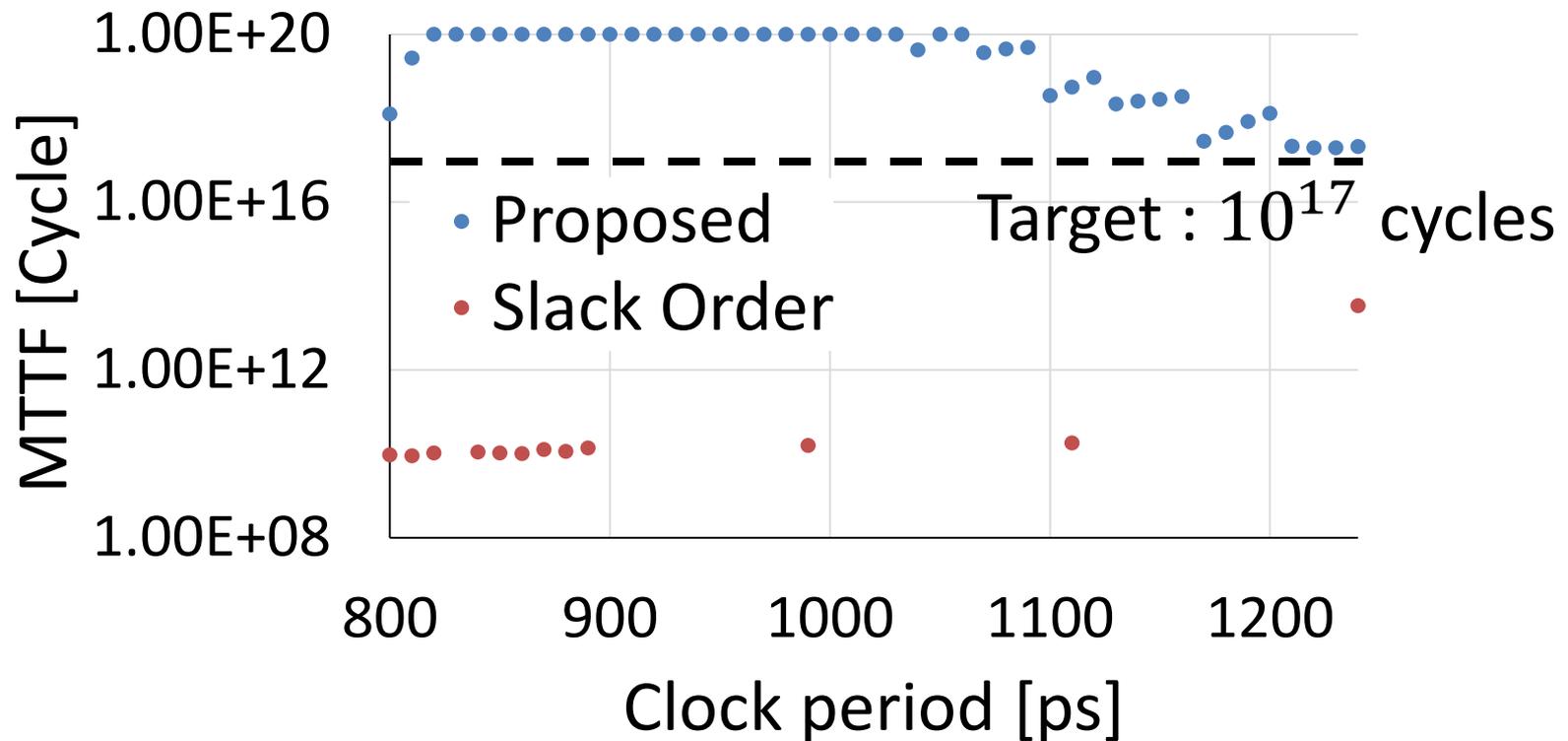
MTTF Estimation

MTTF (Mean Time To Failure)

1. Calculate timing violation and activation probability for all paths in isolated circuit.

2. Calculate transition rate and estimate MTTF (Next Slide).

MTTF Estimation[1] : Markov Chain

Database

Store logic sim. results

Reference

Describe circuit operation w/ state machine

Calculate transition prob. w/ database

Derive MTTF from matrix operation

Speed control level

: Normal states
: Failure state

Error happened

Delay fluctuation[ps]
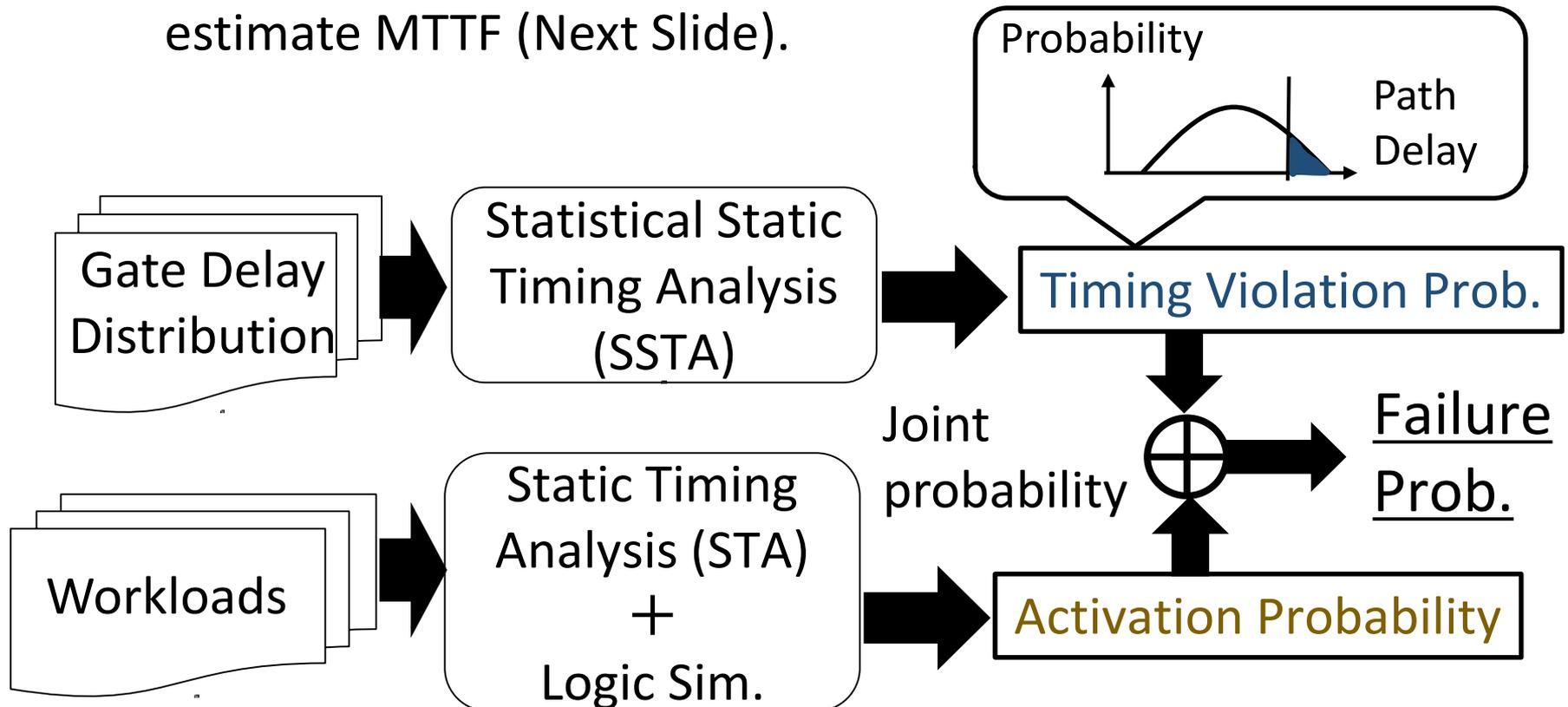
$$A = \begin{bmatrix} -q_1 & q_{12} & \cdots & q_{1N} \\ q_{21} & -q_2 & \cdots & q_{2N} \\ \vdots & \vdots & \ddots & \vdots \\ q_{N1} & q_{N2} & \cdots & -q_N \end{bmatrix}$$

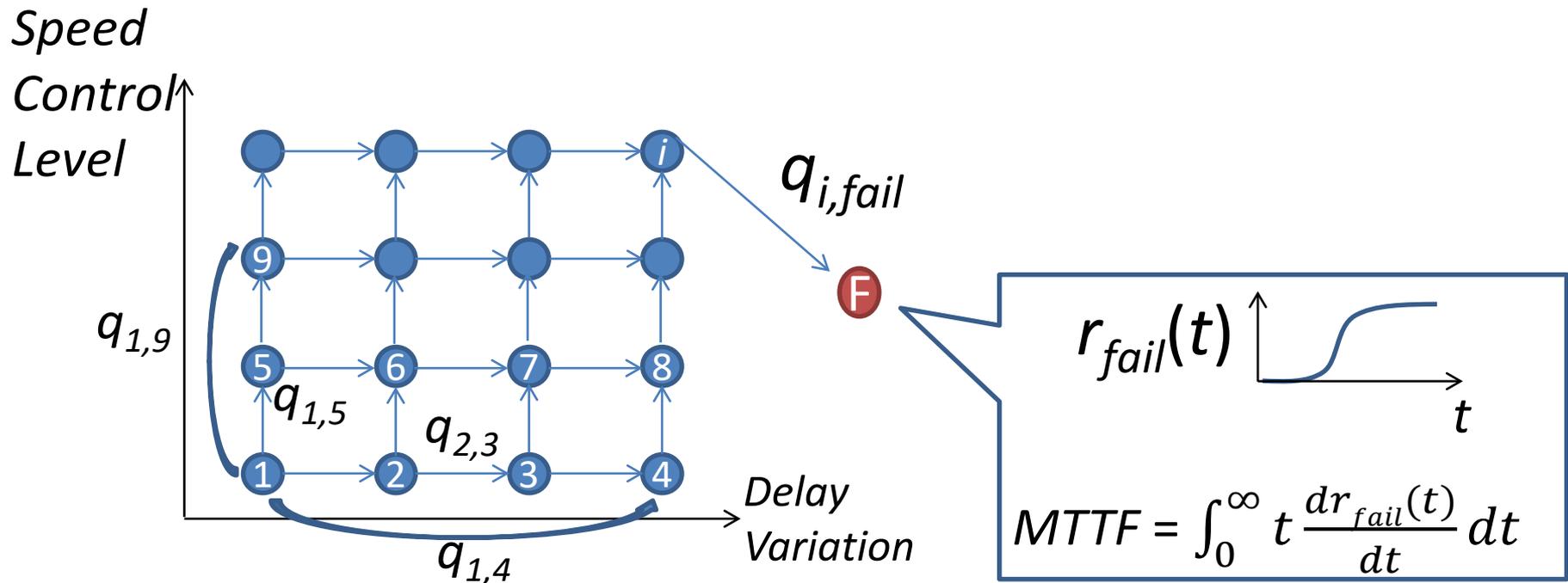$$P(t) = L^{-1}[(sI - A)^{-1}](t)$$

$$MTTF = \int_0^\infty t \, \frac{dp_{init,fail}}{dt} \, dt$$

[1] S. Iizuka, Y. Masuda, M. Hashimoto, and T. Onoye,
"Stochastic Timing Error Rate Estimation under Process and Temporal Variations," in *Proc. ITC*, 2015.

MTTF Estimation [1] : Markov Chain

From transition rate, we can know Time To Failure (TTF).

Speed Control Level

$q_{i,fail}$

$q_{1,9}$

$q_{1,5}$

$q_{2,3}$

$q_{1,4}$

Delay Variation

F

$r_{fail}(t)$

t

$$MTTF = \int_0^\infty t \frac{dr_{fail}(t)}{dt} dt$$

[1] S. Iizuka, Y. Masuda, M. Hashimoto, and T. Onoye, "Stochastic Timing Error Rate Estimation under Process and Temporal Variations," in *Proc. ITC*, 2015.

Markov Model w/ Aging State [1]

- 3-dimensional Markov chain
  - V_{dd}, ΔV_{dd}, Aging

Degradation
State 0

Degradation
State 1

Degradation
State 2

Degrade according to transition rate representing aging effect.

[1] S. Iizuka, Y. Masuda, M. Hashimoto, and T. Onoye,
"Stochastic Timing Error Rate Estimation under Process and Temporal Variations," in *Proc. ITC*, 2015.
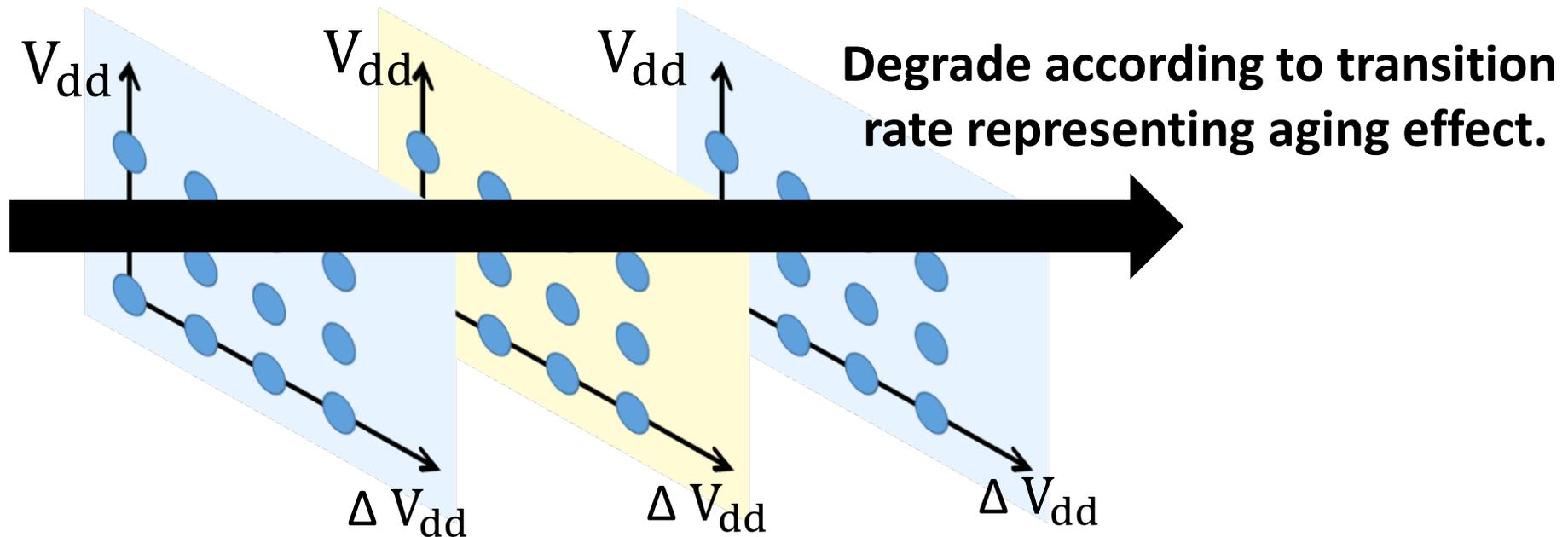
Model of Aging Effect

1. Model aging effect from measured data[3].

    - Average degradation data of 666 transistors and fit to equation representing NBTI aging effect[4] .

        - $\Delta V_{th}(t) = Xe^{V_g} + Ye^{V_g} \log(1 + Zt)$ (T/D model)

            – V_g : Stress Voltage, X, Y, Z : Constants

2. Definition of degradation states

    - 0, 0.5, 1, 5, 10, 15, 20 mV (7 states).

3. Calculate transition rate between each pair of states.

$$p_{trans\_i} = \frac{1}{t_{stay\_i}}$$

p_{trans_i}	: Transition rate to *i+1*-th state.
t_{stay_i}	: # of staying cycle in *i*-th state.

[3] B. J. Velamala, K. B. Sutaria, H. Shimizu, H. Awano, T. Sato, G. Wirth, and Y. Cao, "Compact Modeling of Statistical BTI Under Trapping/Detrapping," IEEE Trans. ED, vol.60, no.11, pp.3645-3654, 2013.

[4] K. B. Sutaria, J. B. Velamala, C. H. Kim, T. Sato, and Y. Cao, "Aging Statistics Based on Trapping/Detrapping: Compact Modeling and Silicon Validation," IEEE Trans. Device and Materials Reliability, vol.14, no.2, pp.607-615, 2014.

Problem Formulation of FF Selection

Maximizing sum of gate-wise failure prob.

- Objective

  - Maximize : $\sum_{k=1}^{N_{inst}}(P_{inst_{k\_fail}} \times B_{inst_k})$

- Constraint   • Variable

  - $0 \leq B_{inst_k} \leq 1\ (1 \leq k \leq N_{inst})$ - $B_{TEP_i}(1 \leq i \leq N_{FF})$

  - $0 \leq B_{TEP_i} \leq 1\ (1 \leq i \leq N_{FF})$

  - $\sum_{k=1}^{N_{FF}} B_{TEP_i} \leq N_{TEP}$

  - $B_{inst_k} = \bigvee_{k=1}^{N_{FF}}(B_{TEP_i} \times B_{FF_{i\_inst_k}}) \leq \sum_{k=1}^{N_{FF}}(B_{TEP_i} \times B_{FF_{i\_inst_k}})$

B_{inst_k}	: It will be 1 when paths ending target FFs include *k*-th instance.
B_{TEP_i}	: It will be 1 when *i*-th FF is selected for TEP-FF insertion.
N_{TEP}	: Maximum # of TEP-FF insertion.
$B_{FF_{i\_inst_k}}$	: It will be 1 when path ending *i*-th FF includes *k*-th instance.