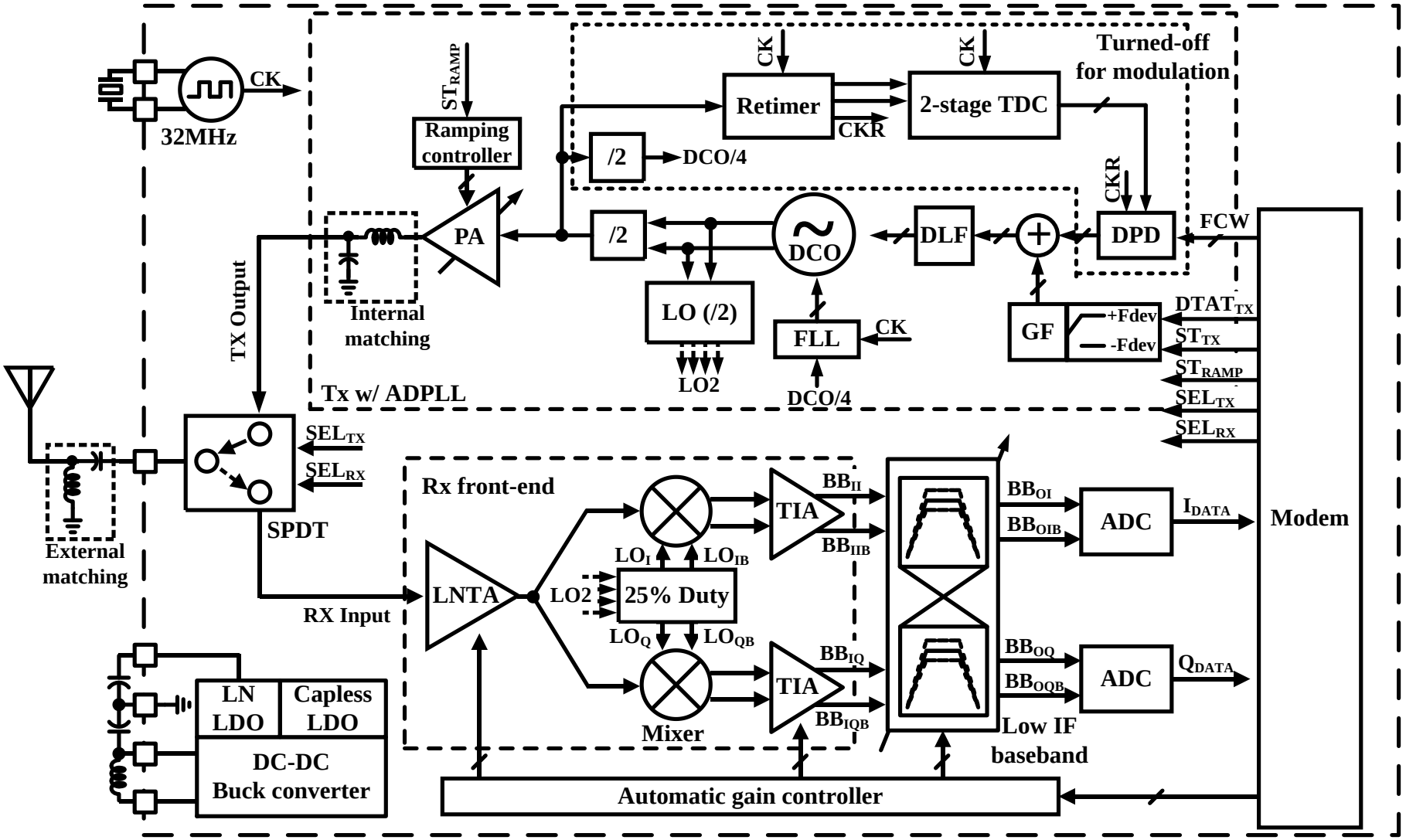
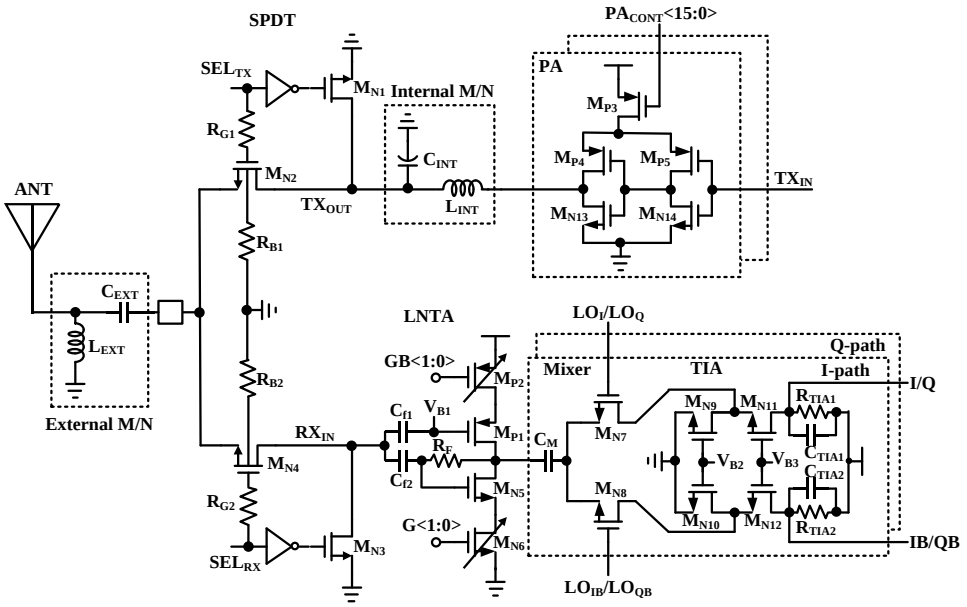
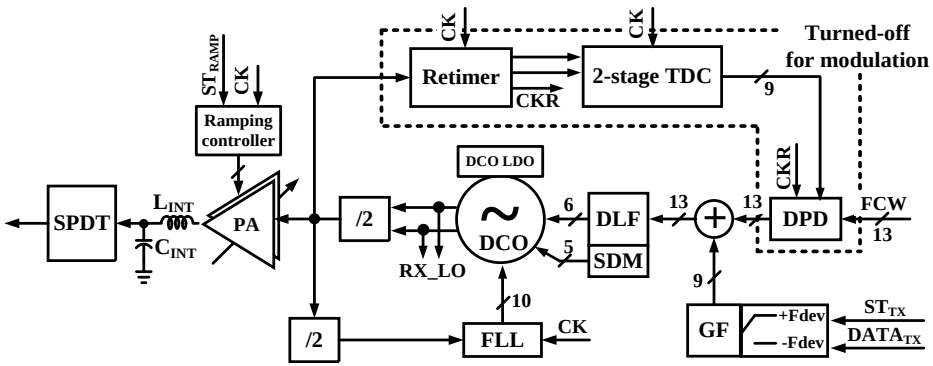
Top block diagram & Key features



Building Blocks



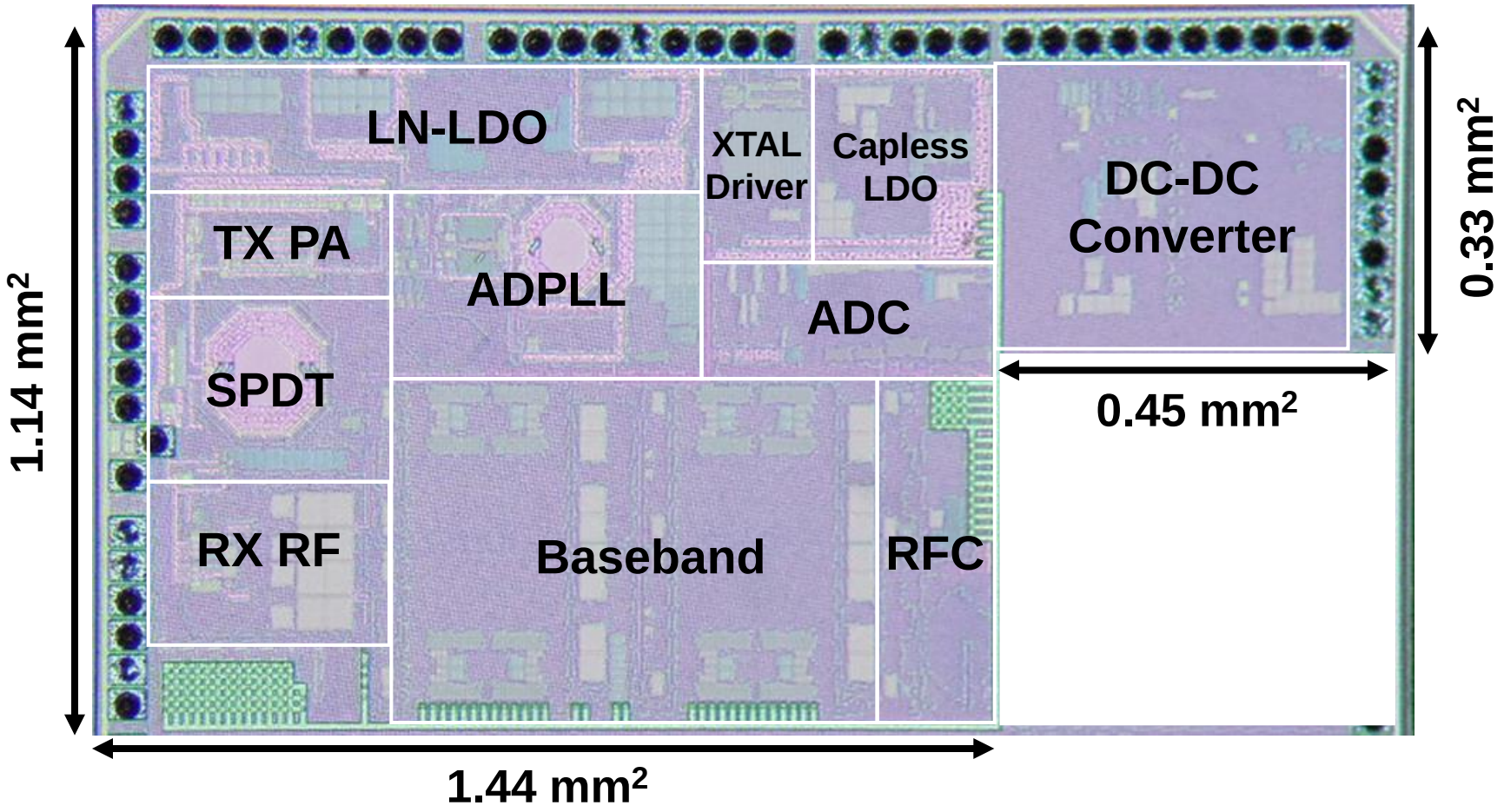
<RX Front-end including SPDT Switch>



<ADPLL based Transmitter>

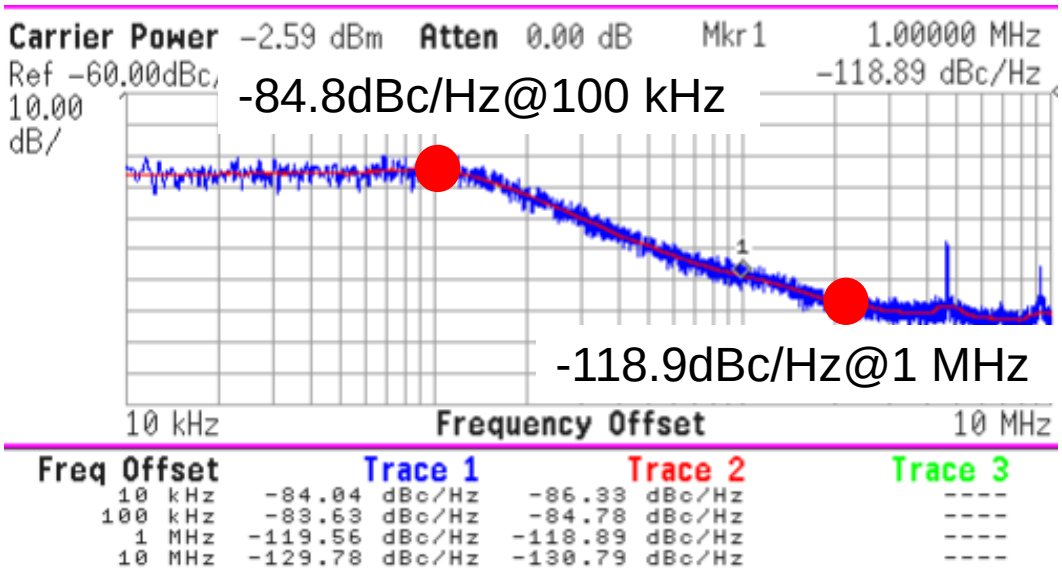
- **Retimer based ADPLL**
- **Direct Modulation Technique**
- **Low Noise figure using 25% duty generator**
  - **Driving Passive mixer**
  - **Current mode operation**

Chip Photograph

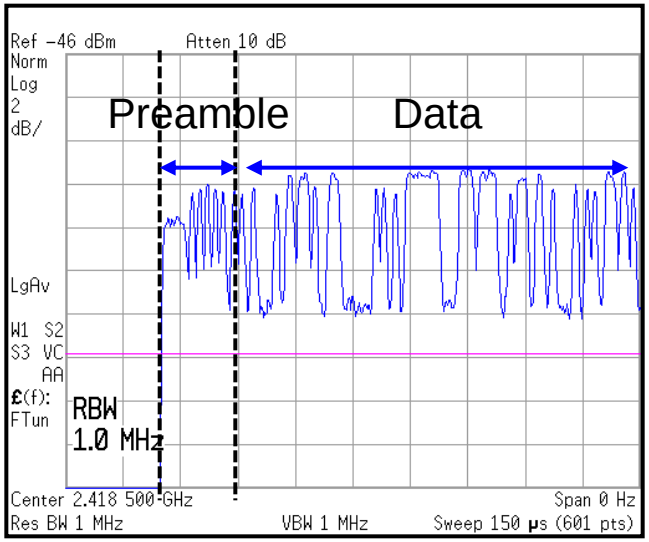


- Process : 1-poly 6-metal 55-nm CMOS
- Area : 1.79 mm² (Transceiver + DC-DC Converter)

Tx Measurement



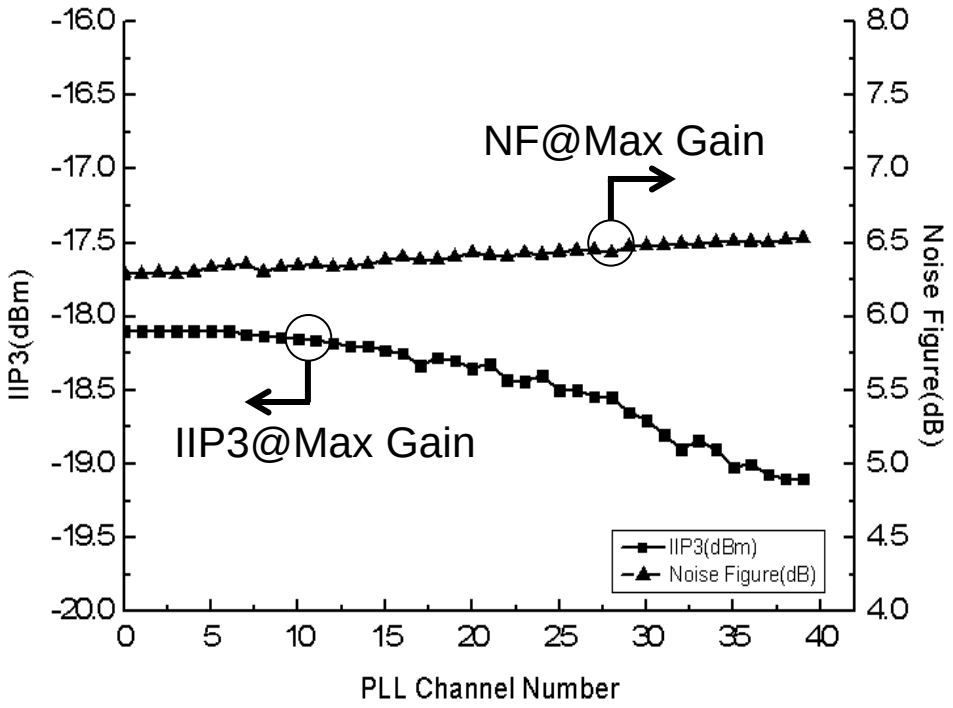
<Phase noise>



<Transient of TX freq.>

- **Fc = 2.44 GHz**
  - **-84.8dBc/Hz @ 100 kHz offset**
  - **-118.9dBc/Hz @ 1 MHz offset**

IIP3, NF / BLE Ch.



<IIP3 and NF>

- **6.2 < NF < 6.8 dB**
- **-19 < IIP3 < -18.2 dBm**

	This Work	*[10] JSSC 2015*	*[11] VLSI 2013*
CMOS technology	55 nm	55 nm	65 nm
Supply voltage (V)	3.0	3.0	3.0
TX output power class	0 dBm	0 dBm	0 dBm
TRX Switch	**Integrated**	Integrated	None
TX power Consumption (mW)	**6 @ 0 dBm**	10.1 @ 0 dBm	10.5 @ 0 dBm
RX architecture	Low-IF	Low-IF	Zero-IF
RX power Consumption (mW)	**5**	11.2	9.3
Noise figure (dB)	*6.8	5.5	6
RX sensitivity (dBm)	-94	-94.5	-94
Area (mm^2)	****1.79**	**2.9	1.1