SIU Southern Illinois University CARBONDALE

Tianjin University of Technology

A 5.8GHz DSRC Digitally Controlled CMOS RF-SoC Transceiver for China Electronic Toll Collection

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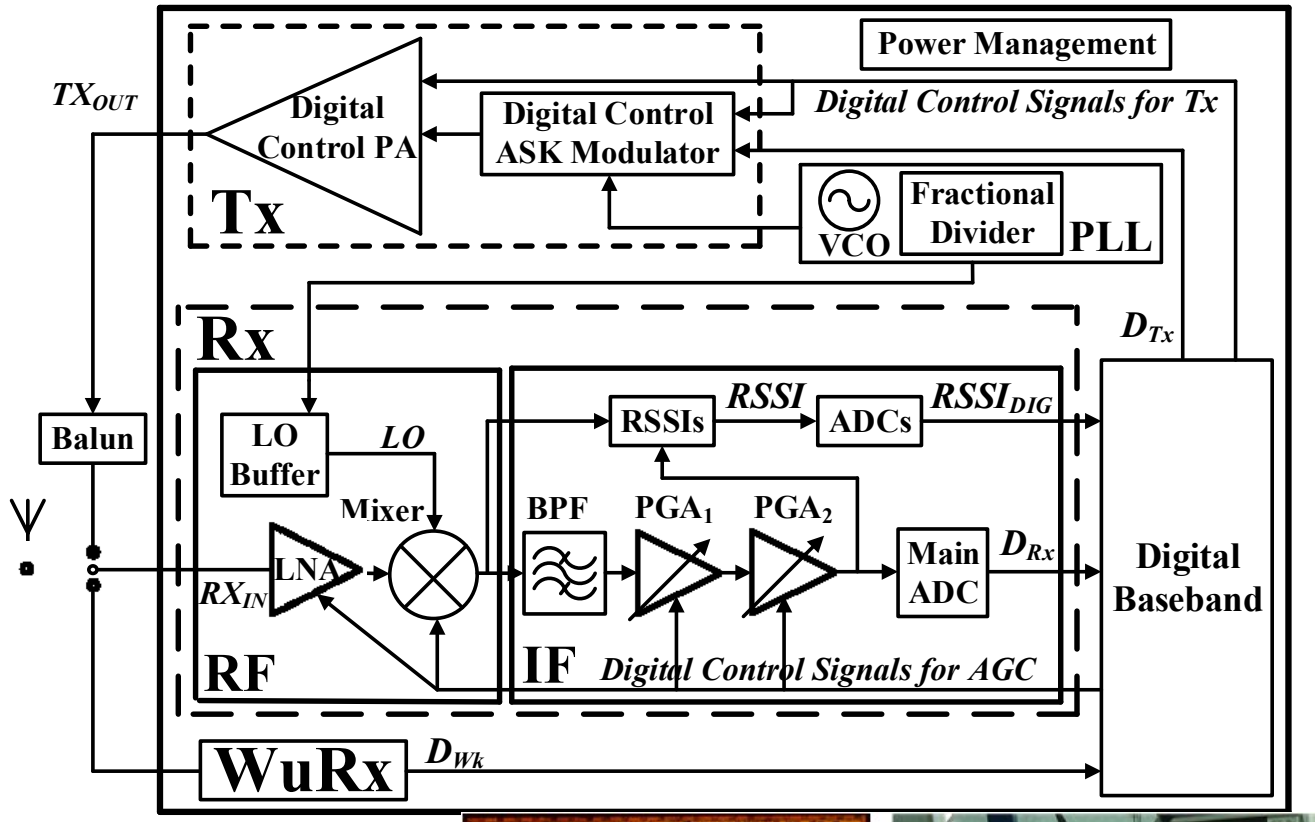
ASP-DAC University Design Contest

Features

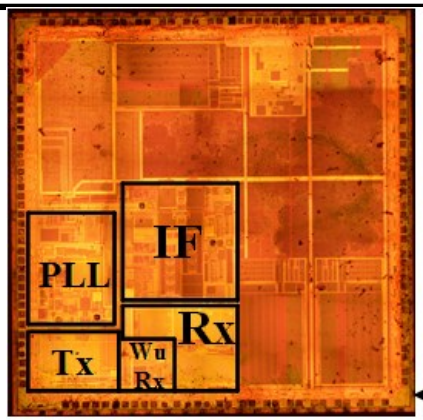
- **Fully integrated transceiver (RF+analog+baseband)**
  - First RF-SoC integration for ETC systems
- **Digital control adjusts operation of RF circuits**
  - Advanced control algorithm, immune to process variation
- **Simplified system architecture**
  - Eliminate non-essential analog blocks (e.g. filters, DAC, voltage-current converter)
- **Significant performance improvement**
  - 37% in peak output power, 12% in dynamic operation range, 34% in area savings, etc.

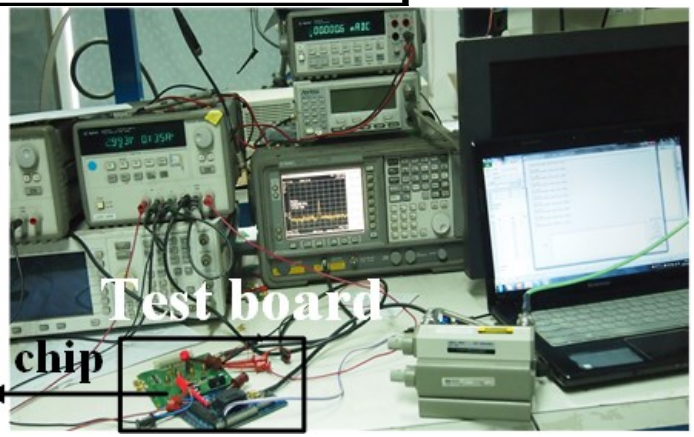
4A-24 Architecture and Implementation



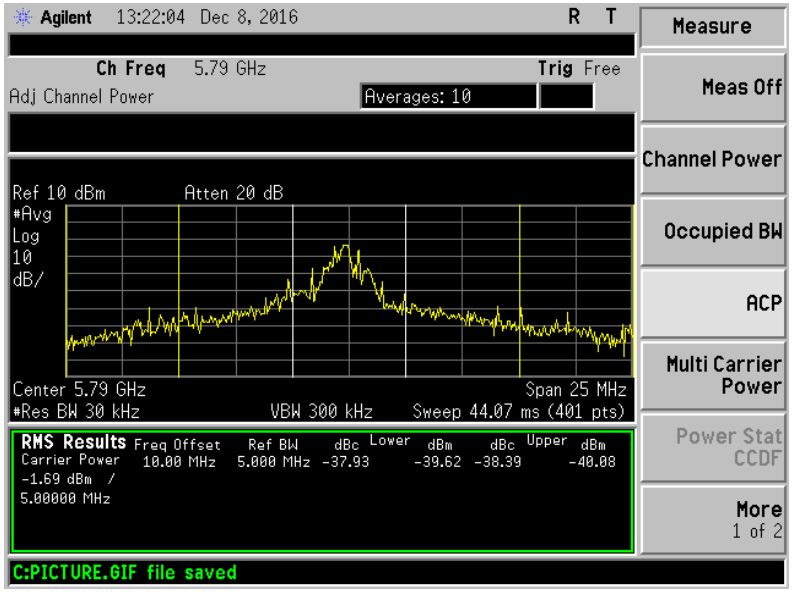
Tx
ASK modulator (32 tuning steps)
PA (4 gain options)

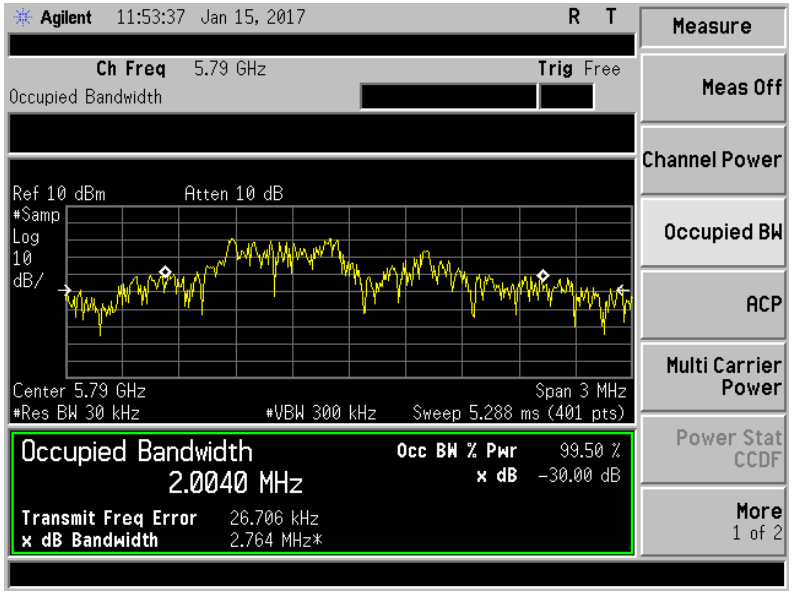
Rx
LNA (4 gain options)
Mixer (4 gain options)
PGA_1 (2 gain options)
PGA_2 (16 gain options)

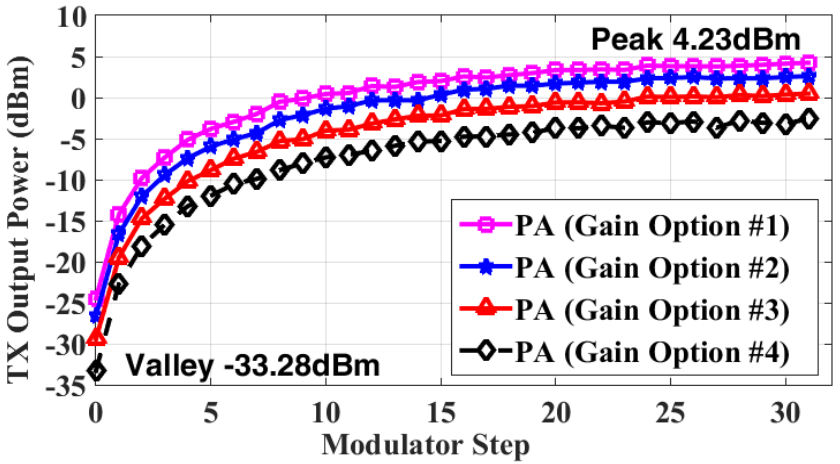


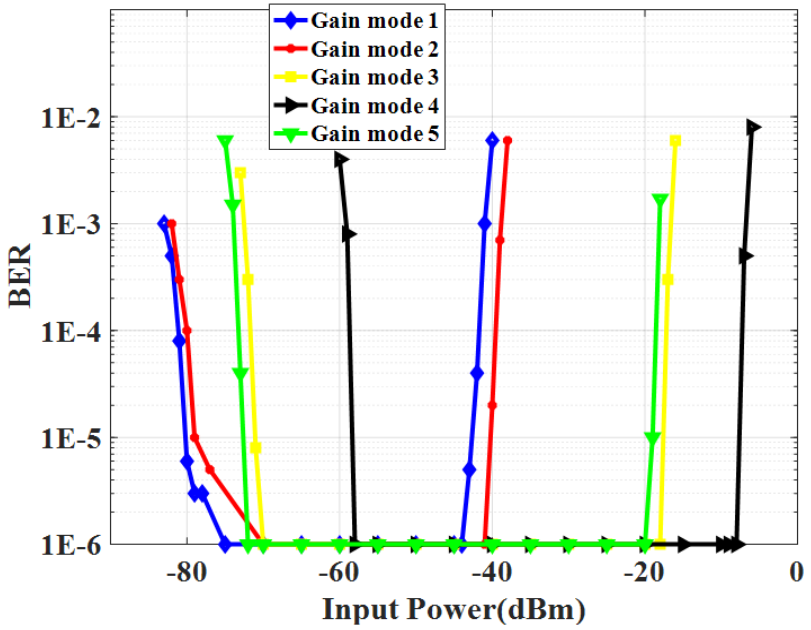


4A-24 Measurement Results









4A-24 Performance Comparison

Reference	[ISCAS, 2008]	[TMTT, 2010]	[ISSCC, 2012]	This work
Technology	CMOS180nm	CMOS130nm	CMOS130nm	CMOS130nm
Control	analog	analog	analog	digital
Tx output peak power (dBm)	+10.5 (differential)	+10 (differential)	+5 (single end)	+7.23 (single end)
OBW (MHz)	2~6	N/A	3	2
ACPR (dBc)	-49 (+6MHz)	-43 (+5MHz)	-53 (+5MHz)	-38 (+5MHz)
Tx dynamic range (dB)	19	N/A	34	37
Rx dynamic range (dBm)	-76 ~ -40	-84 ~ N/A	-60 ~ 0	-76 ~ -8
BER	N/A	10^{-5}	N/A	10^{-6}
AGC	Limited	limited	No	On-chip
Area of RF blocks (mm^2)	N/A	3.31	2	1.32
Current consumption of RF blocks (mA)	51	N/A	59	58

Advantages in design flexibility, Tx output peak power, Tx & Rx dynamic range, Rx sensitivity, BER, area