



UNIVERSITY OF MINNESOTA

Driven to Discover[®]

Low Latency Parallel Implementation of Traditionally-Called Stochastic Circuits using Deterministic Shuffling Networks

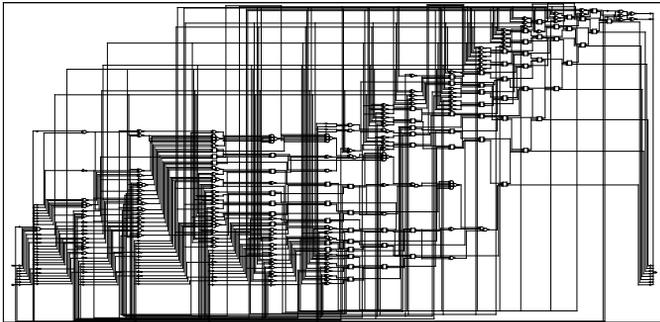
Zhiheng Wang, Soheil Mohajer and Kia Bazargan

Agenda

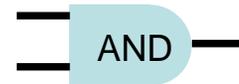
- **Motivation and Background**
- Architecture
- Result
- Summary

Stochastic Computation

- Small area of CKT for complex function



Traditional Multiplication of 10bit
Synthesized using Synopsys tool



Stochastic
Computation of 10 bit
multiplication

Introduction of SC

- Example of Multiplication of two numbers

x=3/6 X: 010110
y=2/6 Y: 100010



Serial Configuration:

- Long clock cycle latency
- Small area

x=3/6 X: 111000
y=2/6 Y: 110000

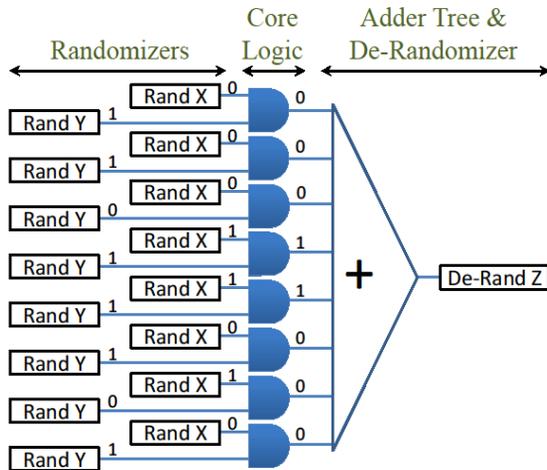


Correlation Problem



Introduction of SC

- Example of Multiplication of two numbers

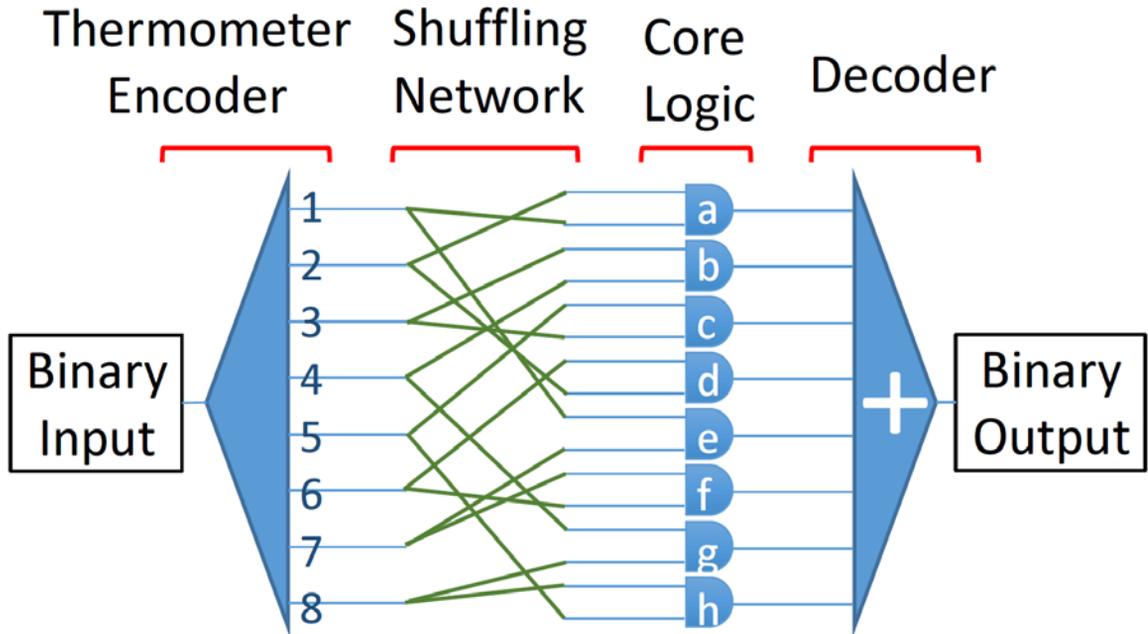


- Parallel Configuration:
- Small clock cycle delay
 - Large area

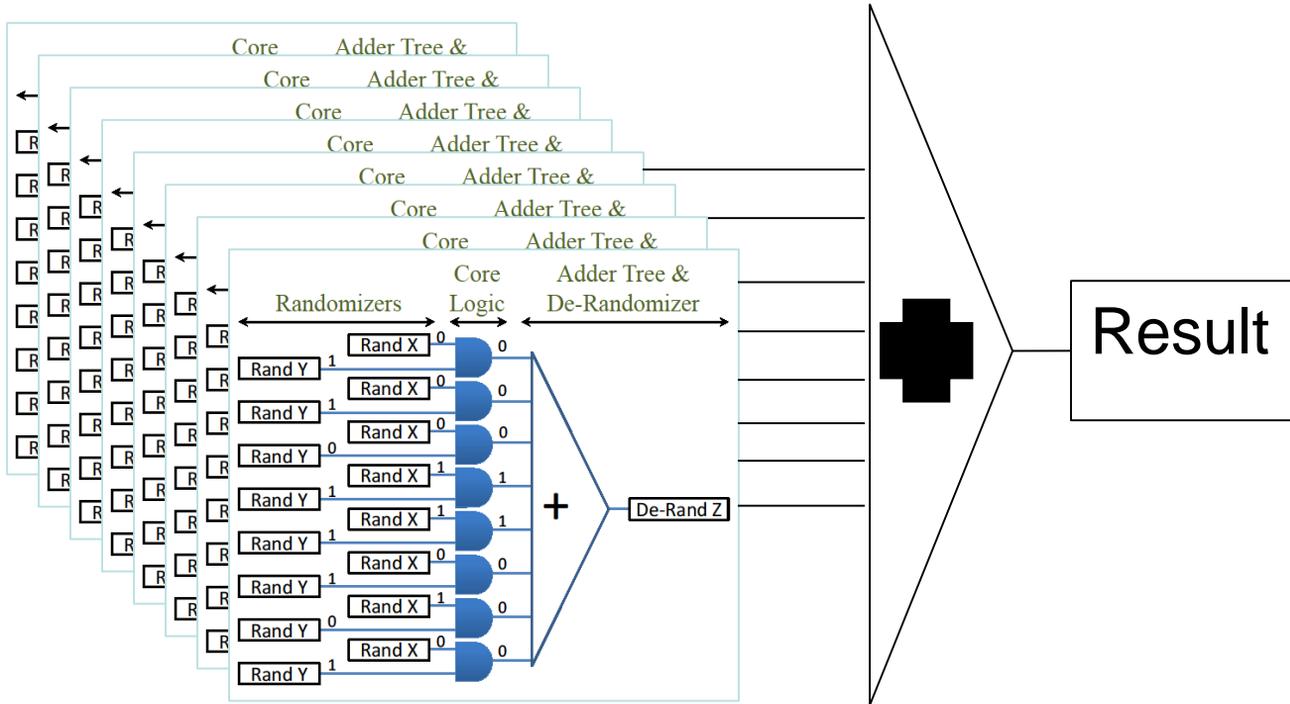
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Deterministic Approach

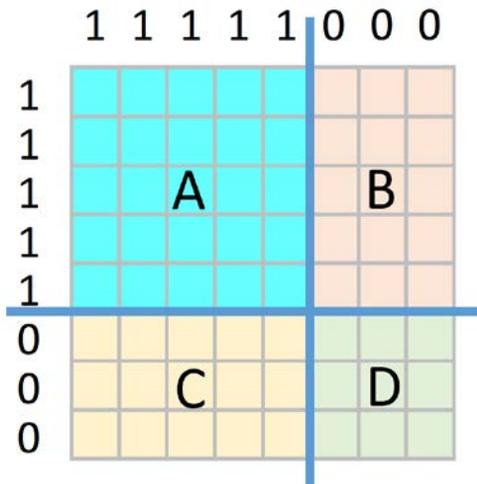


Naïve method: N^2 outputs

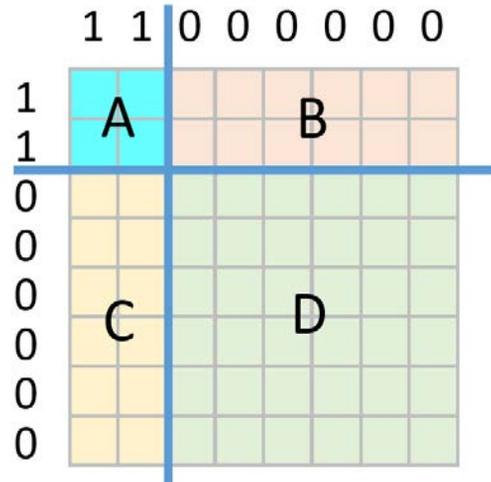


Connection Sampling

- Region Division 5/8:



- Region Division 2/8:



Connection Sampling

- AND gate for 5/8:

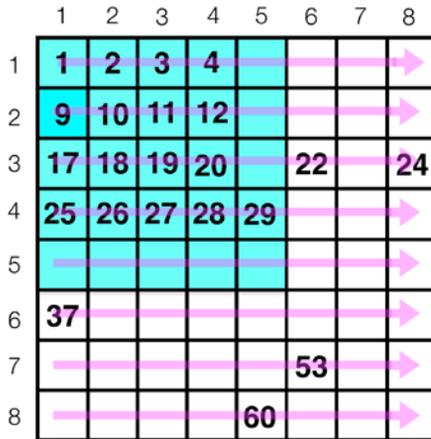
	1	1	1	1	1	0	0	0
1	1	1	1	1	1	0	0	0
1	1	1	1	1	1	0	0	0
1	1	1	1	1	1	0	0	0
1	1	1	1	1	1	0	0	0
1	1	1	1	1	1	0	0	0
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0

- XOR gate for 5/8:

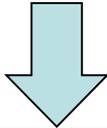
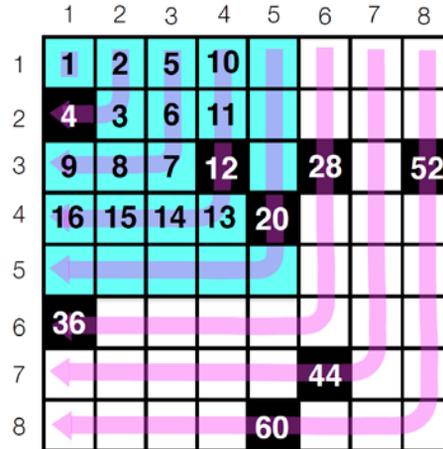
	1	1	1	1	1	0	0	0
1	0	0	0	0	0	1	1	1
1	0	0	0	0	0	1	1	1
1	0	0	0	0	0	1	1	1
1	0	0	0	0	0	1	1	1
1	0	0	0	0	0	1	1	1
0	1	1	1	1	1	0	0	0
0	1	1	1	1	1	0	0	0
0	1	1	1	1	1	0	0	0

Connection Sampling

- Region Division:

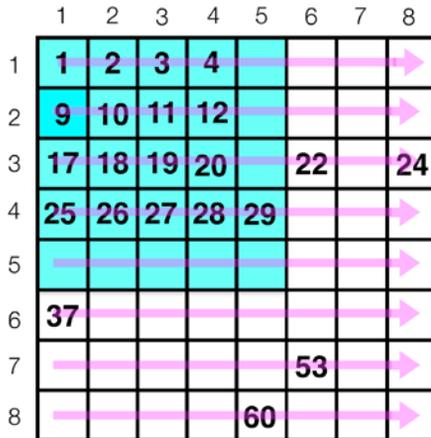


- Sweep Sampling

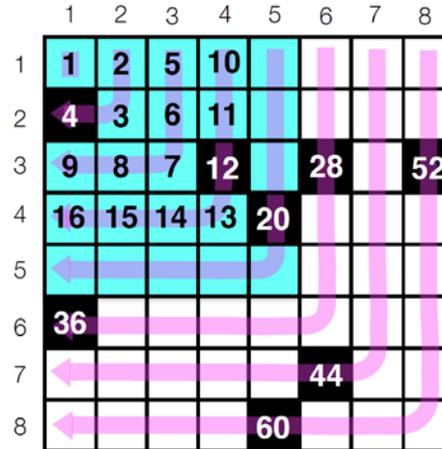


Connection Sampling

- Region Division:



- Sweep Sampling



Example of Multiplication

- 2 bit Multiplication

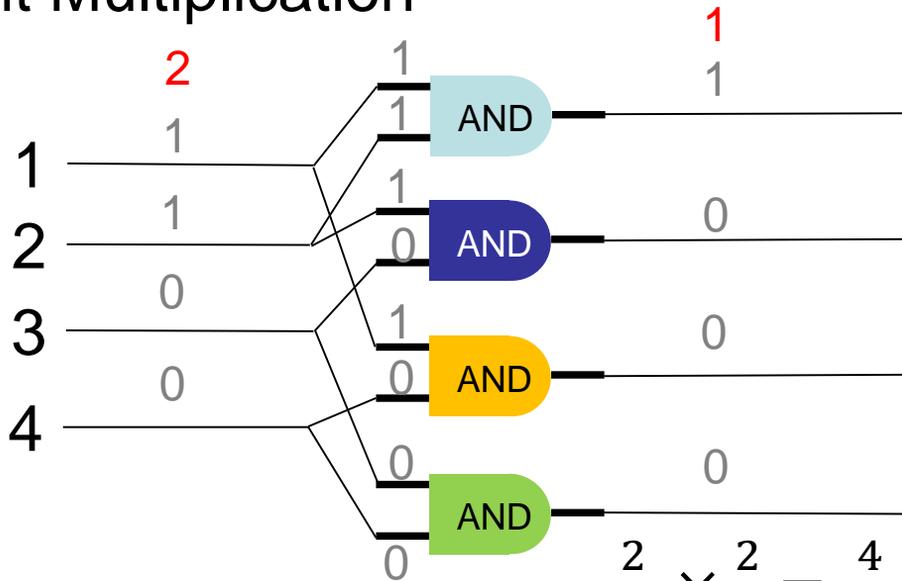
	1	2	3	4
1	1	2	5	10
2	4	3	6	11
3	9	8	7	12
4	16	15	14	13



	1	2	3	4
1	1	2	5	10
2	4	3	6	11
3	9	8	7	12
4	16	15	14	13

Example of Multiplication

- 2 bit Multiplication

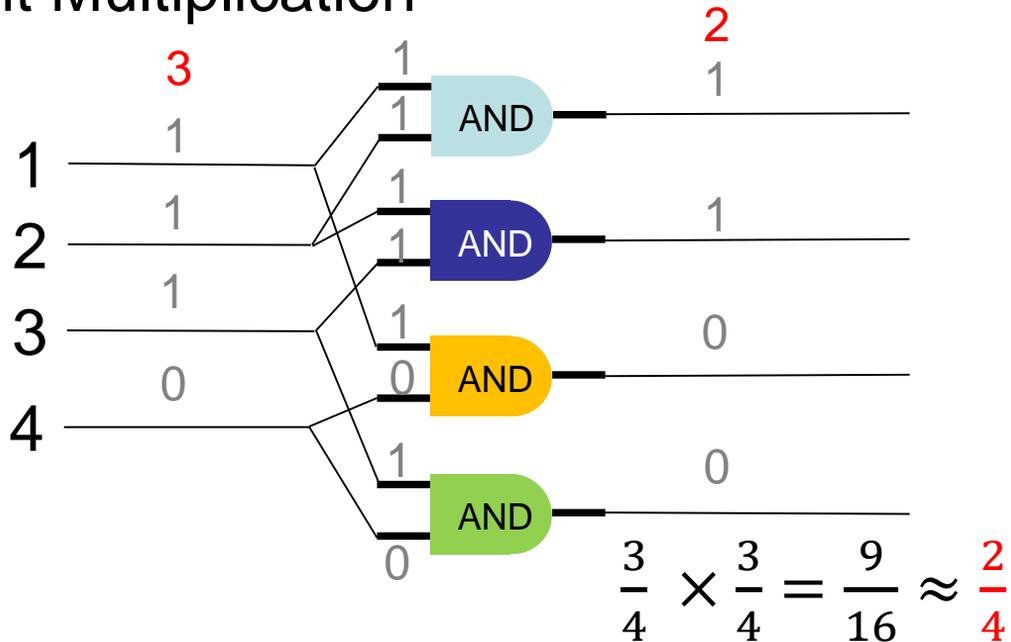


	1	2	3	4
1	1	2	5	10
2	4	3	6	11
3	9	8	7	12
4	16	15	14	13

$$\frac{2}{4} \times \frac{2}{4} = \frac{4}{16} = \frac{1}{4}$$

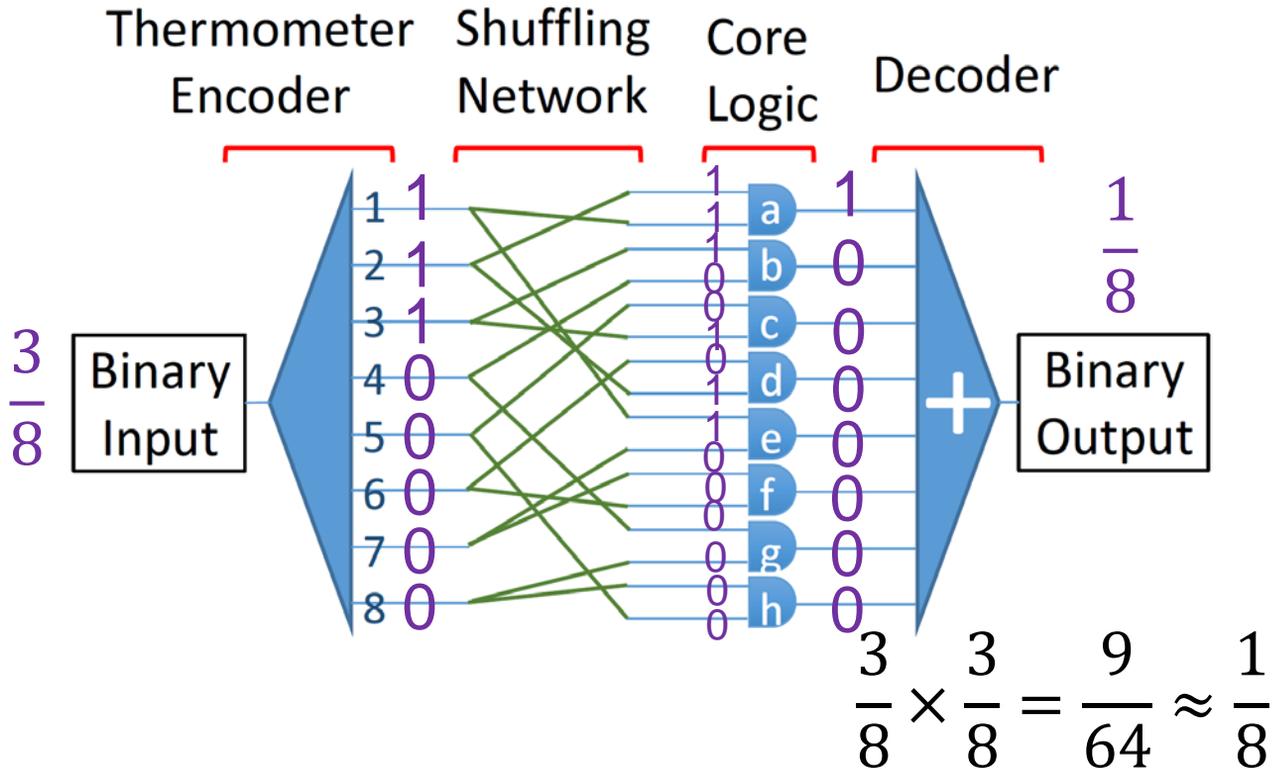
Example of Multiplication

- 2 bit Multiplication

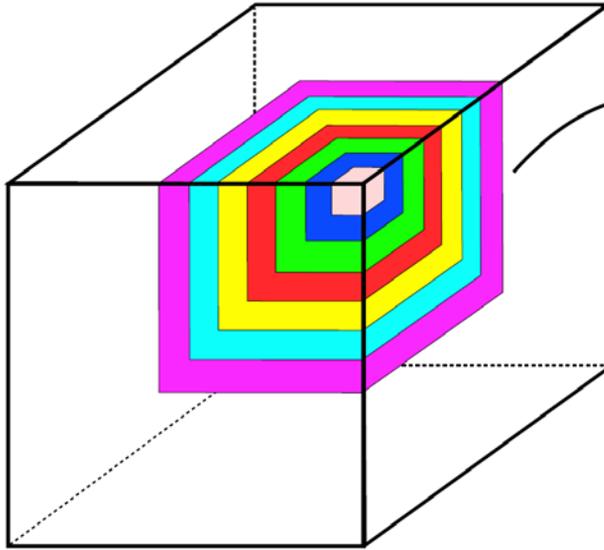


	1	2	3	4
1	1	2	5	10
2	4	3	6	11
3	9	8	7	12
4	16	15	14	13

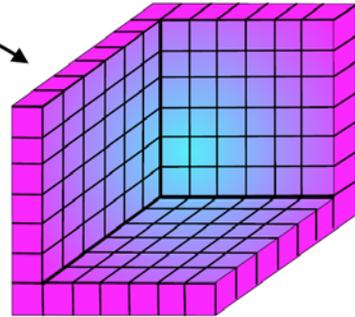
Deterministic Approach



Multi-dimension



d-dimensional cube



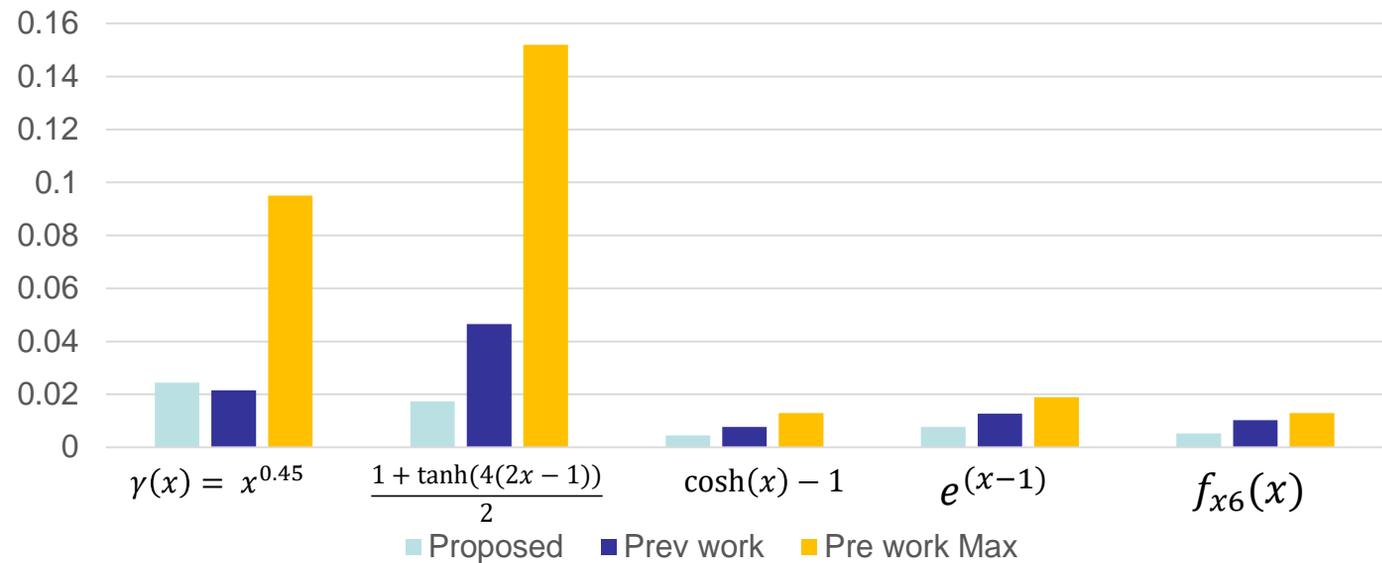
m-th layer

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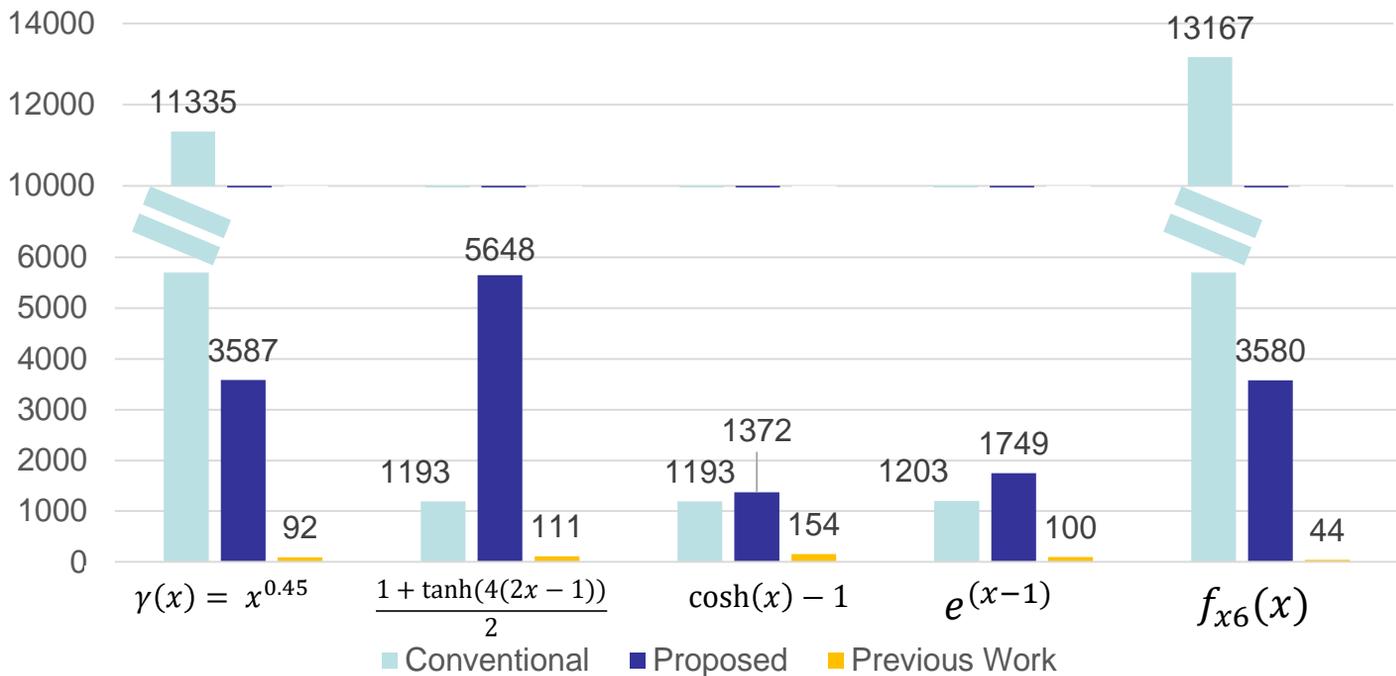
Accuracy

Mean Square Error Comparison



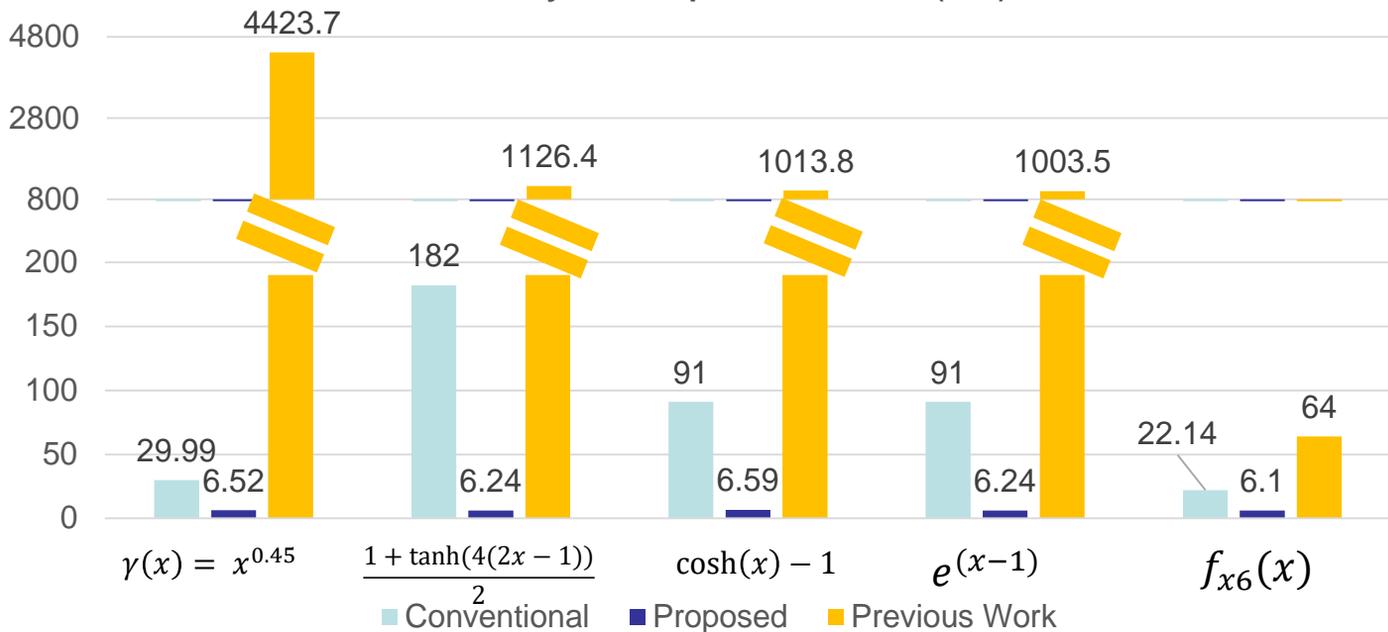
Hardware Comparison

Area Comparison: LUT number

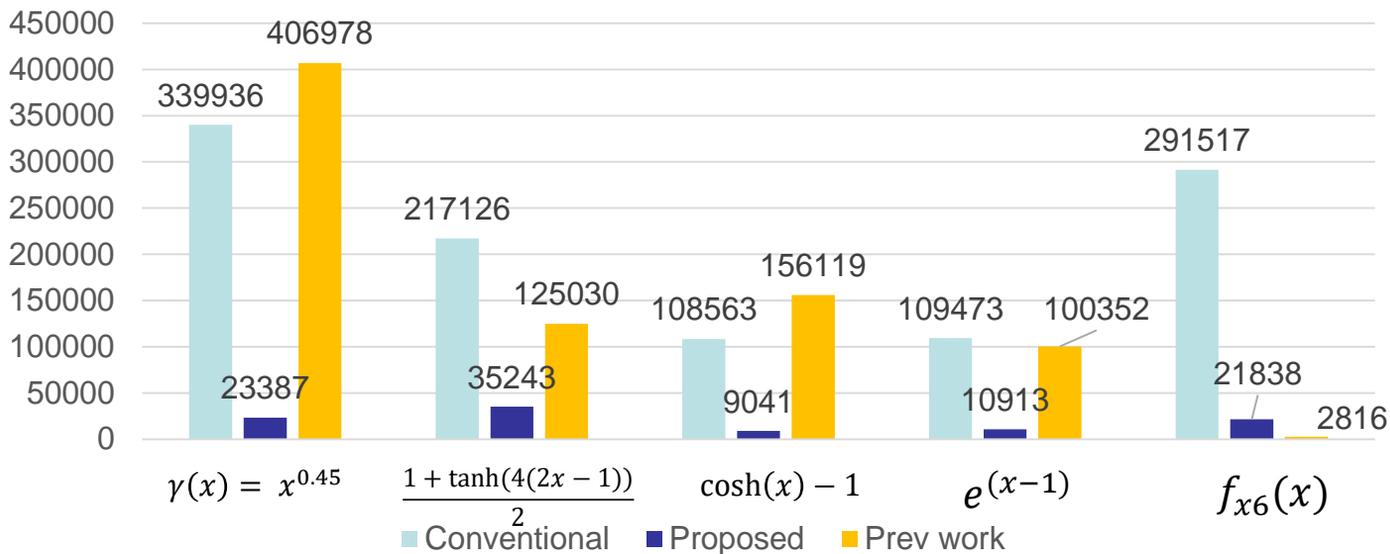


Hardware Comparison

Latency Comparison: in (ns)



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Summary

- On average this only require 10% of area and latency product compare to conventional binary
- High performance computation

THANK YOU!