

SCBench: A Benchmark Design Suite for SystemC Verification and Validation

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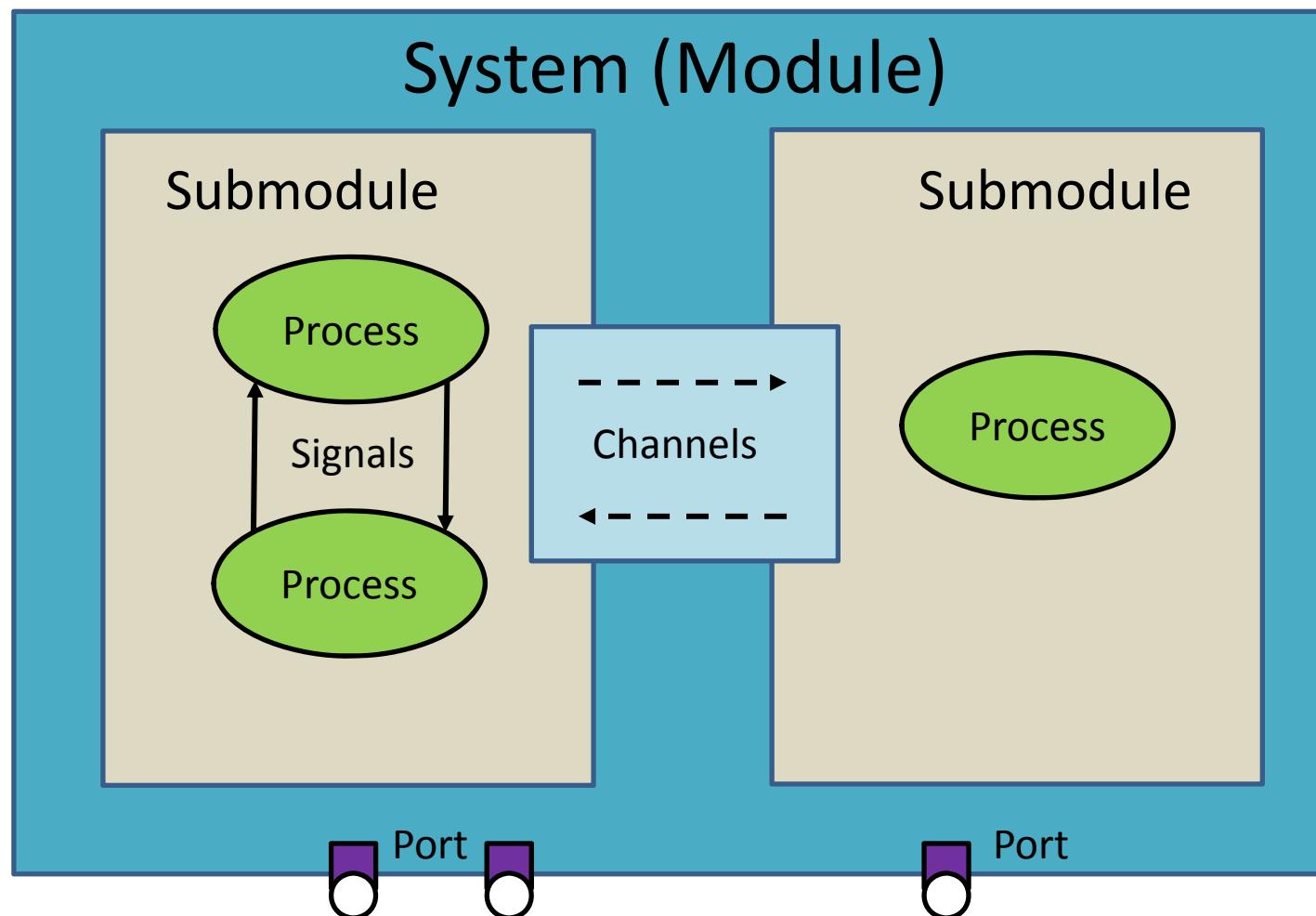
Agenda

- Background and Motivation
- Overview of Benchmark Designs
- Key Features of SCBench
- Characteristics of SCBench
- Benchmark Validation
- Summary and Future Work

What is SystemC?

- A hardware description language (HDL) extending C++
- A set of C++ classes and macros for hardware design
- IEEE Standard 1666™-2011

Major SystemC Structures



Motivation

- The quality of SystemC designs is critical
- It is challenging to assure the quality of SystemC designs
- It is important to evaluate the performance of SystemC verification approaches
- There lack common and up-to-date benchmarks

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Overview of Benchmark Designs

Categories	# Designs	SystemC Specifics
CPU architecture	8	Modules, Hierarchical modules, SC_METHOD, SC_THREAD, SC_CTHREAD, Ports, Interfaces, Signals, FIFOs,
Security	6	
Digital signal processing	4	Events, Timers,
Automotive and industrial	4	Bit vectors, Fixed-point numbers, Fixed-precision types,
Image processing	3	Arbitrary-precision types,
Network	3	LT/AT coding styles,
Artificial intelligence	1	Blocking transport interface, Non-blocking transport interface,
Classical concurrent scenarios	4	Direct memory interface, Debug transport interface,
TLM-2.0	5	Generic payload

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Key Features of SCBench

- Consists of 38 well-written SystemC designs
- Ranges from small single-process to large multi-process designs
- Provides a testbench and a set of stimuli for each design
- Freely available online at
[\(http://svl.cs.pdx.edu/scbench/scbench.html\)](http://svl.cs.pdx.edu/scbench/scbench.html)

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Characteristics of SCBench

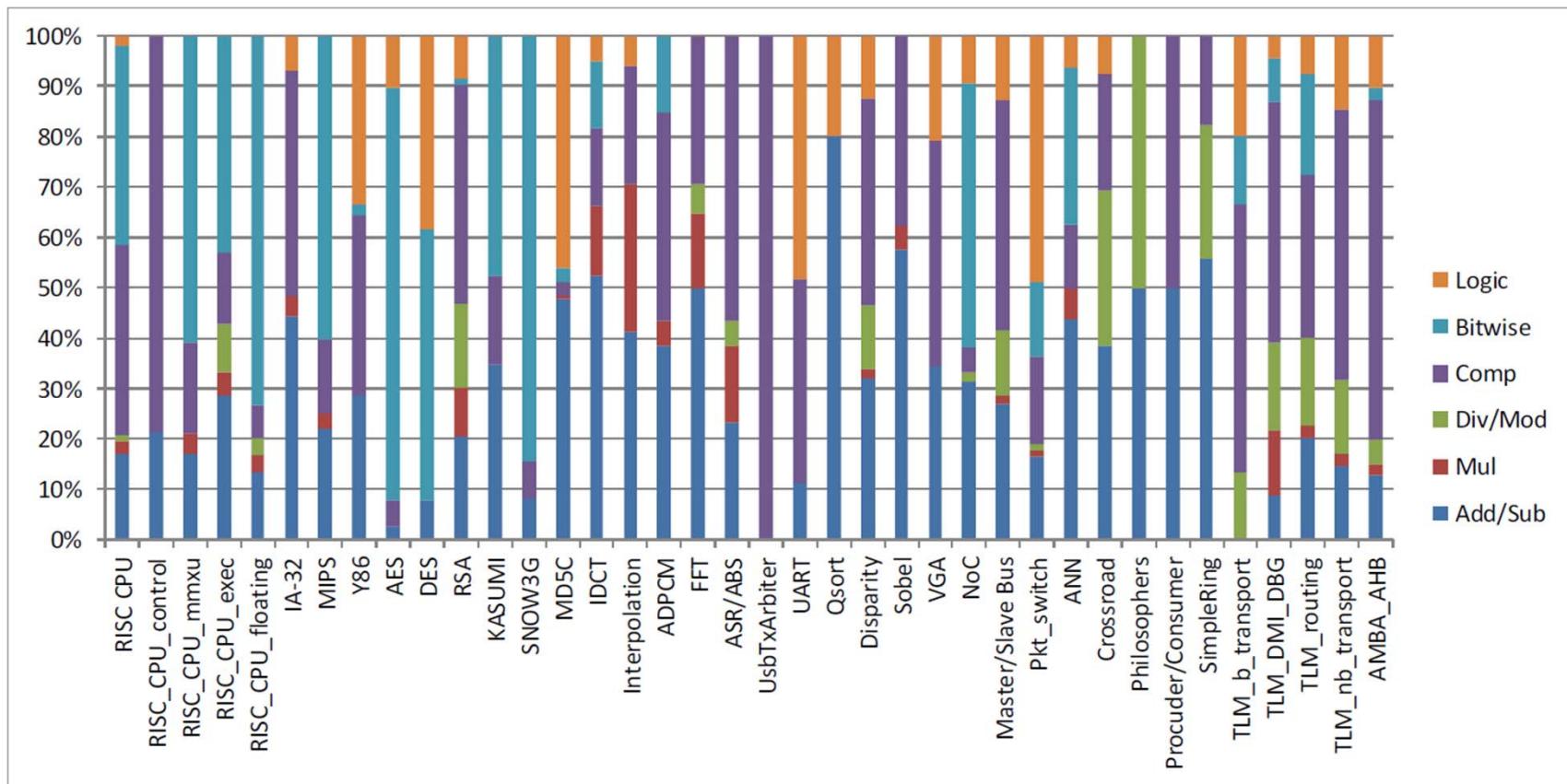


Fig. 1. Occurrence Rate of Operations per Design

Characteristics of SCBench (cont.)

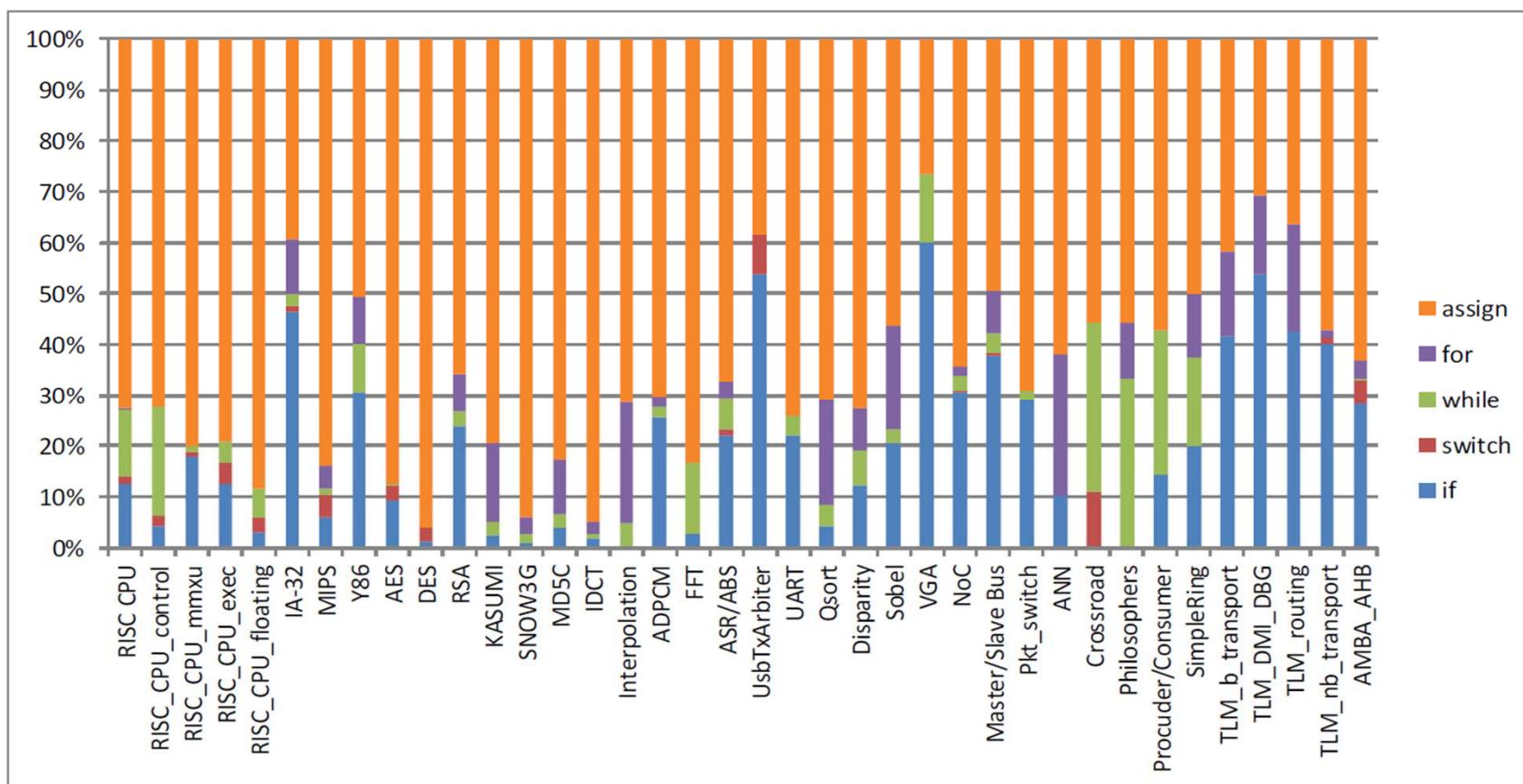


Fig. 2. Occurrence Rate of Statements per Design

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Benchmark Validation

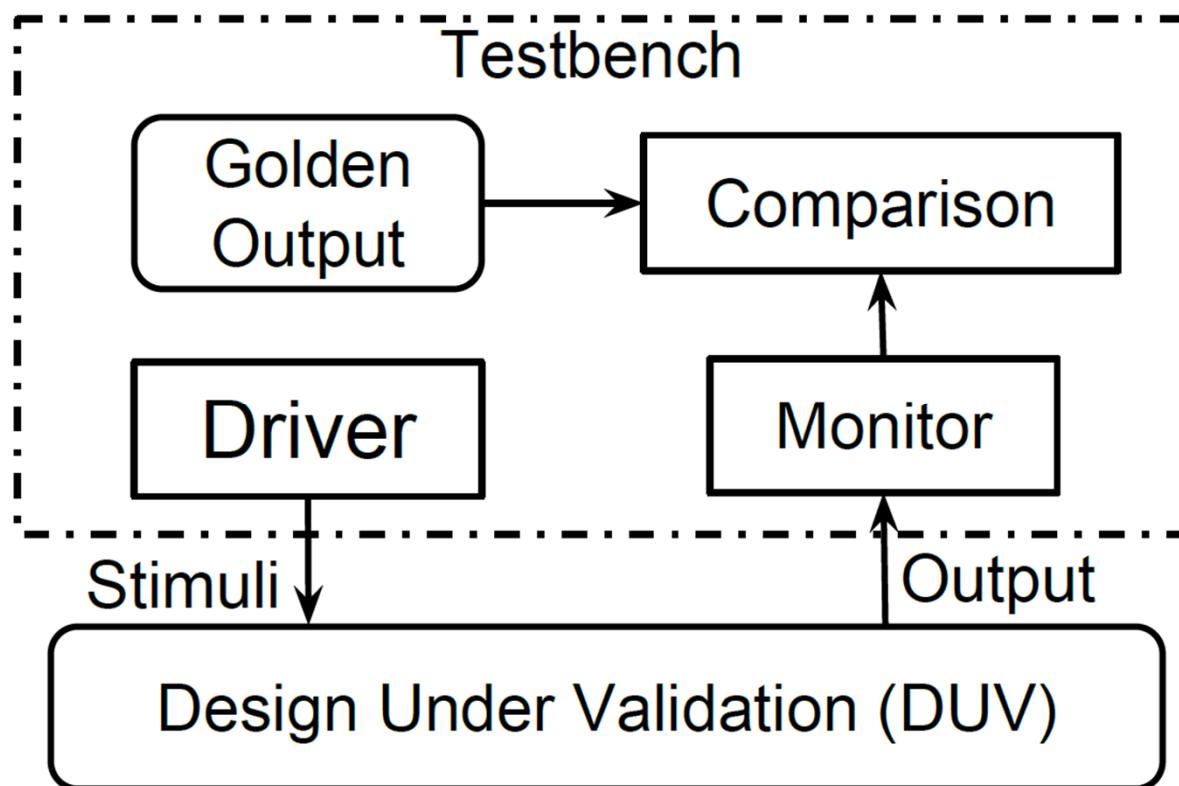


Fig. 3. Testbench

Benchmark Validation (cont.)

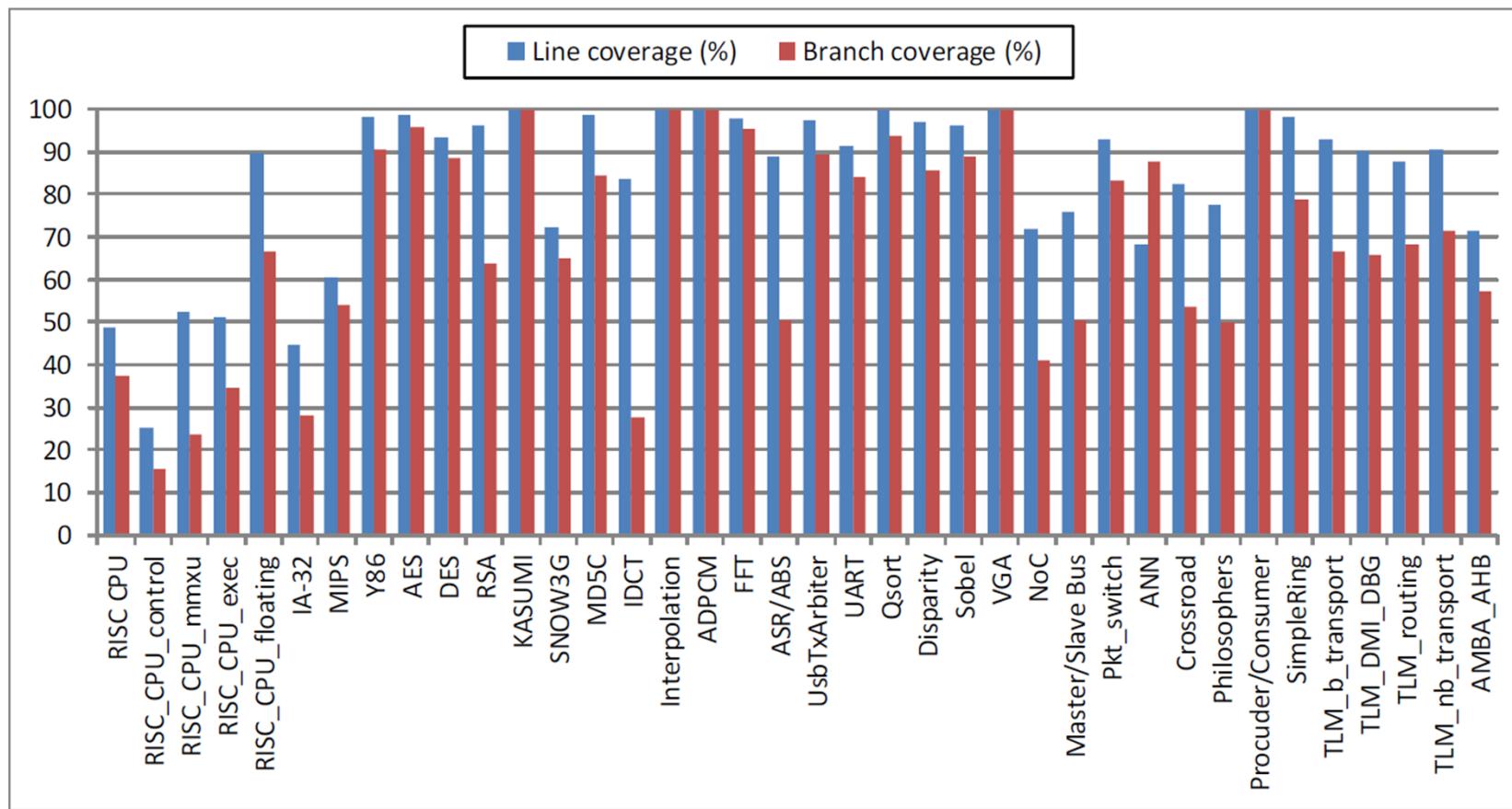


Fig. 4. Code Coverage

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Summary of SCBench

- 38 well-written SystemC designs
- A variety of application domains
- Most core features of SystemC
- A testbench and a set of stimuli for each design
- Freely available online at
[\(http://svl.cs.pdx.edu/scbench/scbench.html\)](http://svl.cs.pdx.edu/scbench/scbench.html)

Future Work

- Extend the benchmark with very large designs, such as system-on-chip designs
- Develop new designs to cover the SystemC features yet to be covered, such as Semaphore and four-valued logic types

Thank you!