An Optimal Gate Design for the Synthesis of Ternary Logic Circuits

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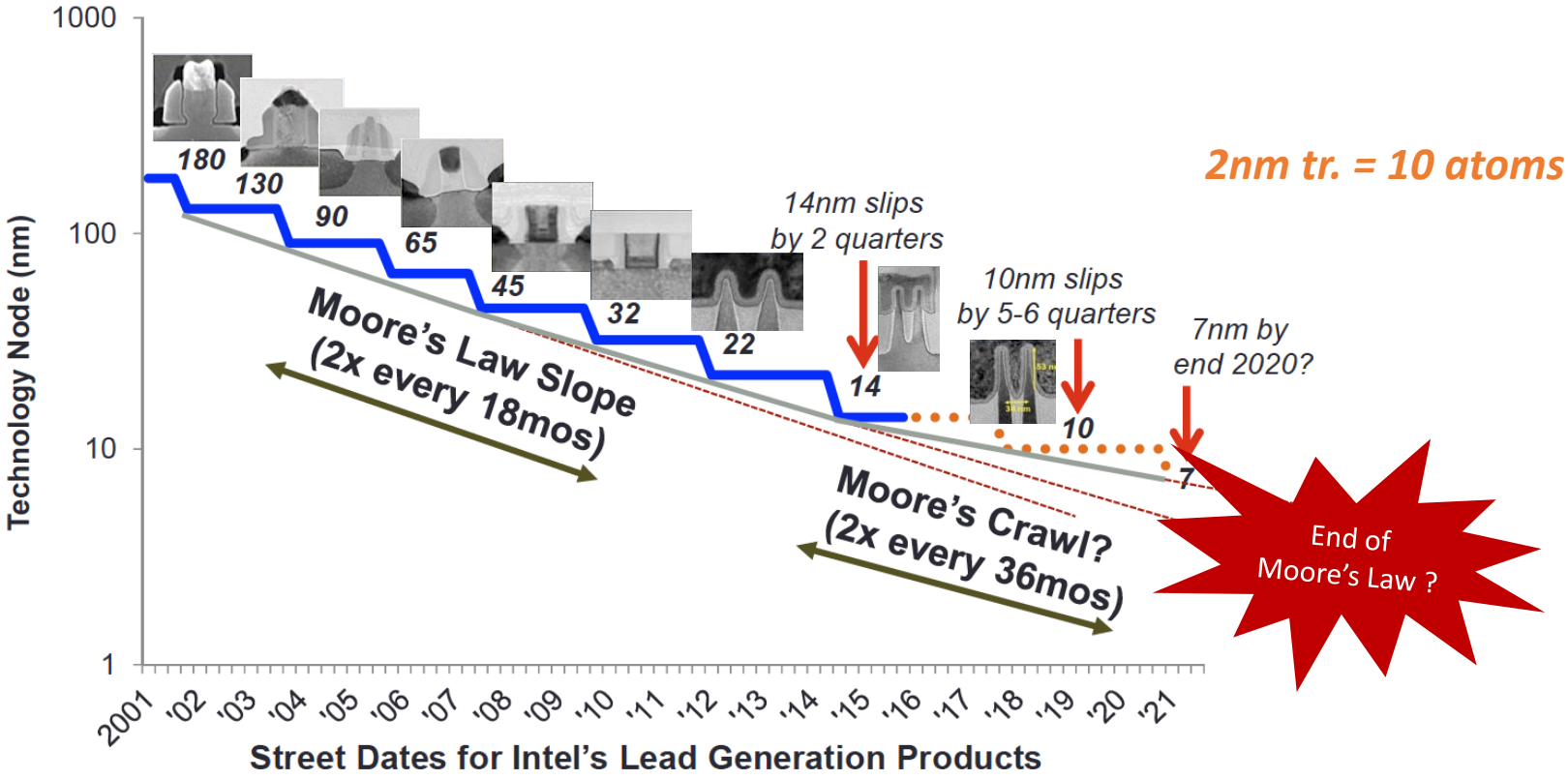
I. Introduction

- Why MVL?

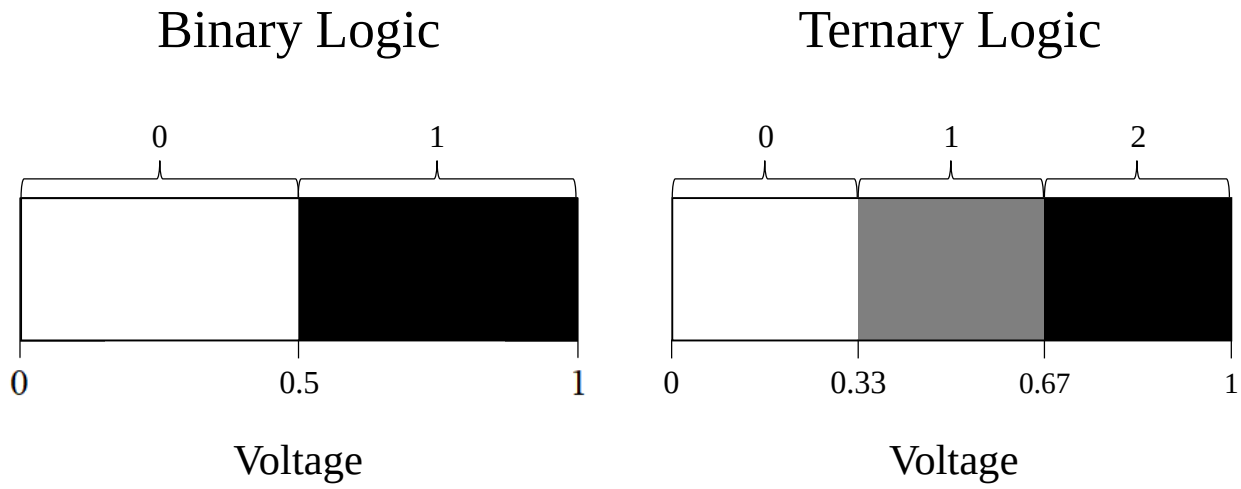
Post Moore's Law



- **Performance gap is increasing and scaling is slow down.**
- **We don't know if the density can be still scaling.**

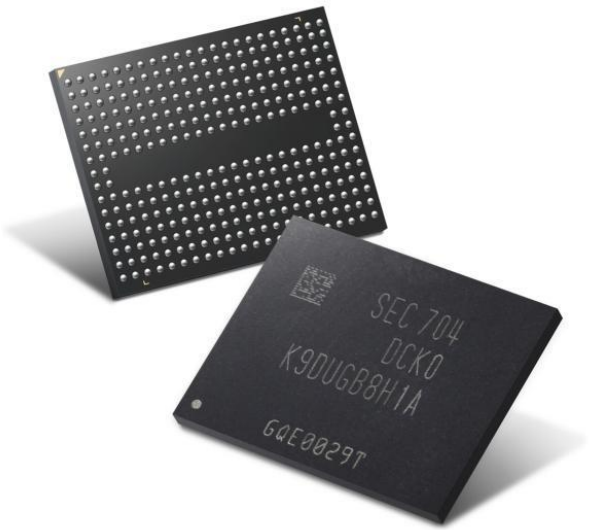
Source: Todd Austin, ICCAD 2018

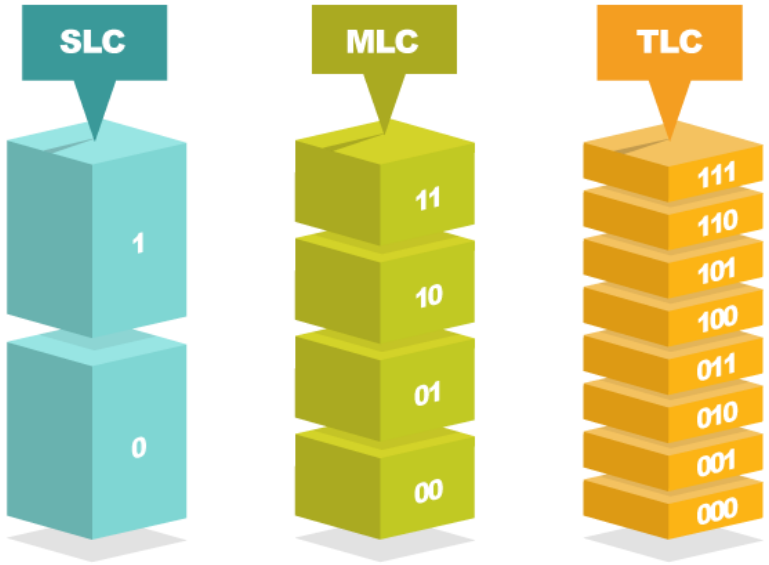
Multi-Valued Logic (MVL)



- **MVL is a logical calculus which have more than two truth values.**
- **MVL circuit designed to use more than two discrete levels.**
- **Digit size and noise margin are a trade off relationship.**

Example of MVL

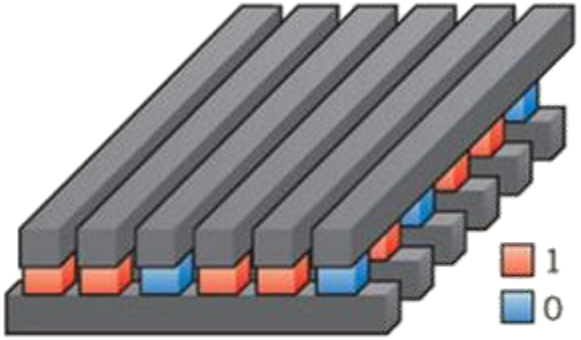




- Solid-state Drive (SSD) and NAND flash memory are example of MVL.
- SLC (Single Level Cell), MLC (Multi Level Cell), and TLC (Triple Level Cell).
- Binary logic (1 bit), Quaternary Logic (2 bit), and Octal Logic (3 bit).

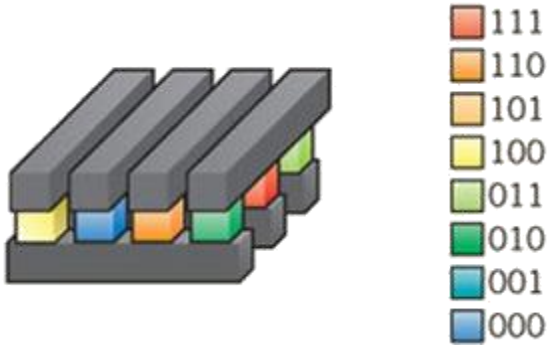
Multi-Valued Circuit

Binary Circuit



Number of Cell : 6 × 6
Digit Size : 1 bit

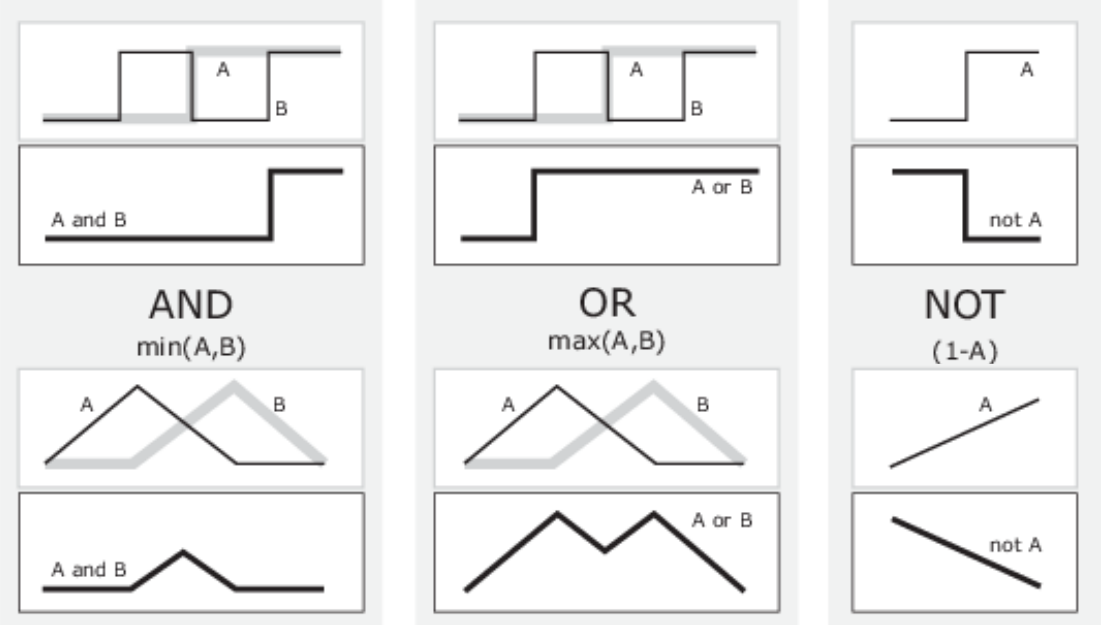
Multi-Valued Circuit



Number of Cell : 3 × 4
Digit Size : 3 bit

- **MV circuit can process the same amount of calculation in a smaller size.**
- **The number of cells, pins, and interconnects are reduced.**
- **It is possible to overcome the limitation of binary circuit.**

MV Logical Operation

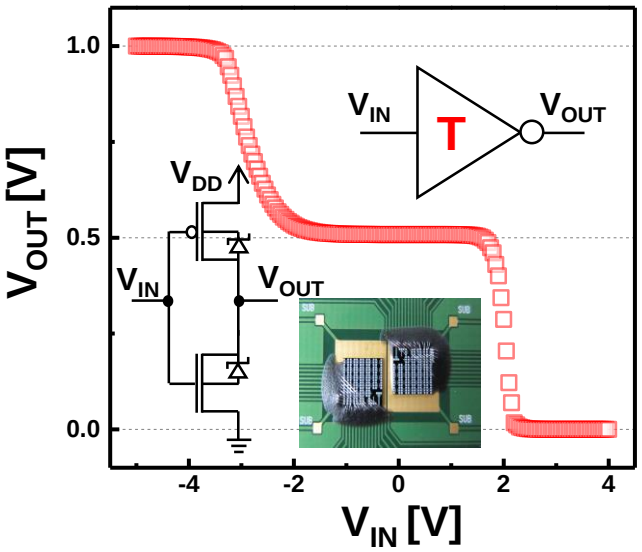


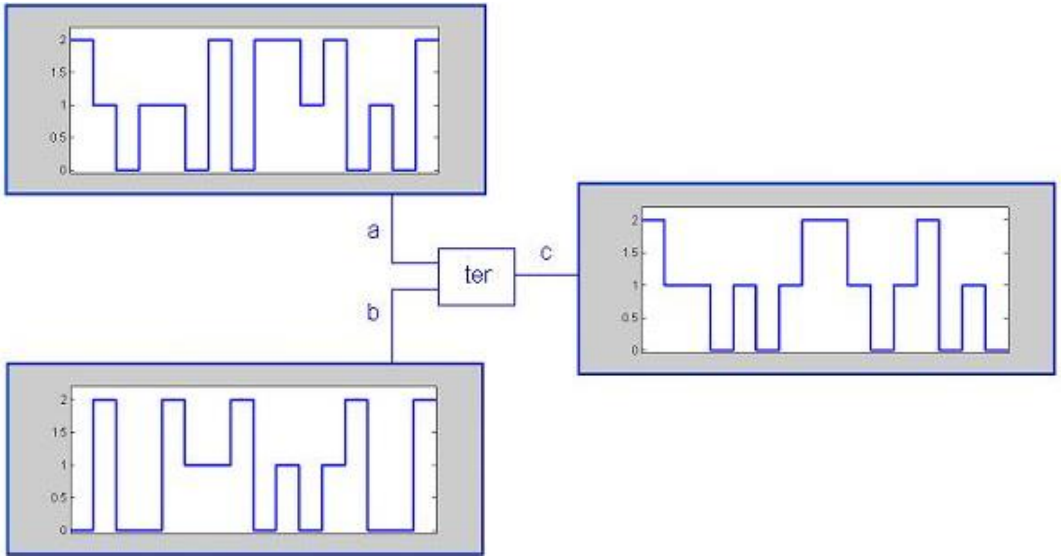
- MVL operations are a superset of standard boolean logic.
- NOT, AND, and OR operation in binary logic.
- NOT, MIN, and MAX operation in Multi-Valued logic.

II. Ternary Logic

- Facing Problem

Ternary Logic & Circuit

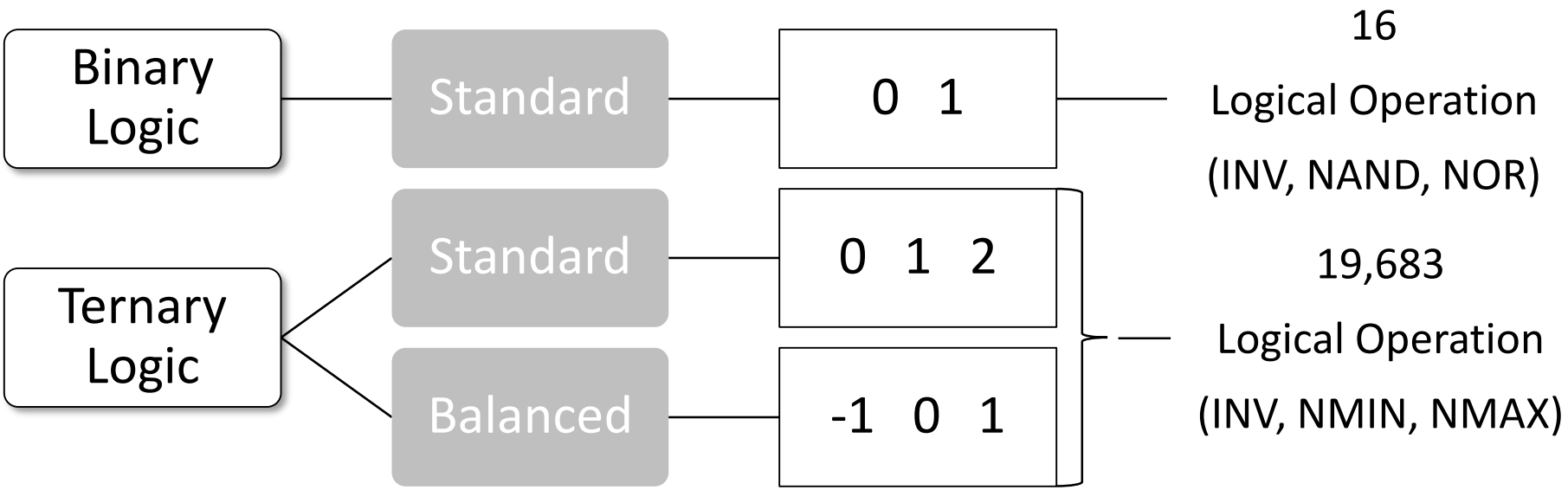




- Ternary logic is a first step of Multi-Valued logic.
- Ternary devices are studied to realize Multi-Valued digital circuits.
- Carbon nanotube FET (CNTFET), Ternary CMOS (T-CMOS), etc.

[5] S. Shin et al., IEEE Trans. of Electron Devices, 2015

2 & 3 Valued Logical Operation

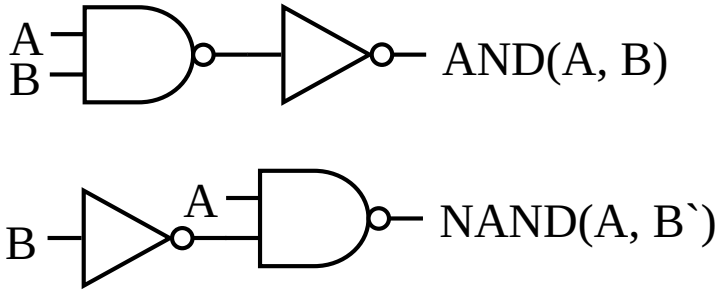


- **Binary logic has 16 (=2^2^2) logical operations.**
- **There are two types of ternary logic depending on the truth value.**
- **Ternary logic has 19,683 (=3^3^3) logical operations.**

Binary Logical Operation

	0	1
0		
1		

2-stage Cascade



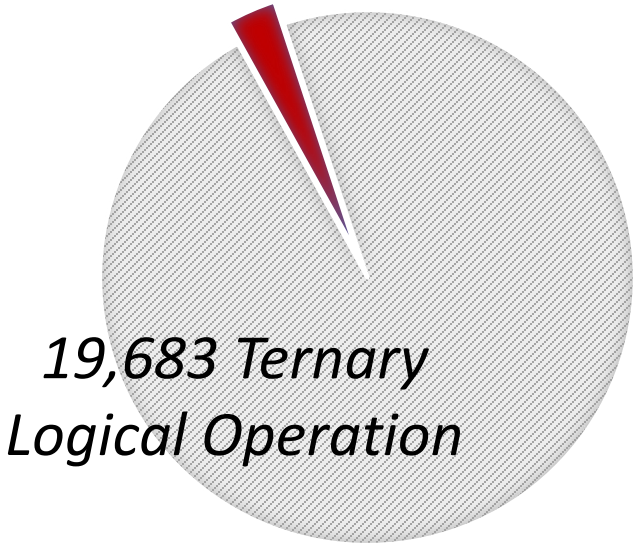
GND	AND(A, B)	NOR(A`, B)	BUF(A)	NOR(A, B`)	BUF(B)	XOR(A, B)	OR(A, B)
0 0	0 0	0 0	0 0	0 1	0 1	0 1	0 1
0 0	0 1	1 0	1 1	0 0	0 1	1 0	1 1

VDD	NAND(A, B)	NAND(A, B`)	INV(A)	NAND(A`, B)	INV(B)	XNOR(A, B)	NOR(A, B)
1 1	1 1	1 1	1 1	1 0	1 0	1 0	1 0
1 1	1 0	0 1	0 0	1 1	1 0	0 1	0 0

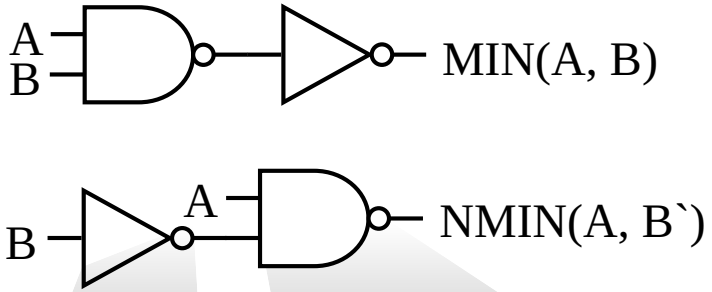
- **INV, NAND, NOR, XOR → 2-stage cascade**
- **16 binary logical operations are implemented with simple circuits.**

Ternary Logical Operation

Less than 1% !



2-stage Cascade



In	Out
0	2
1	1
2	0

STI

\	0	1	2
0	2	2	2
1	2	1	1
2	2	1	0

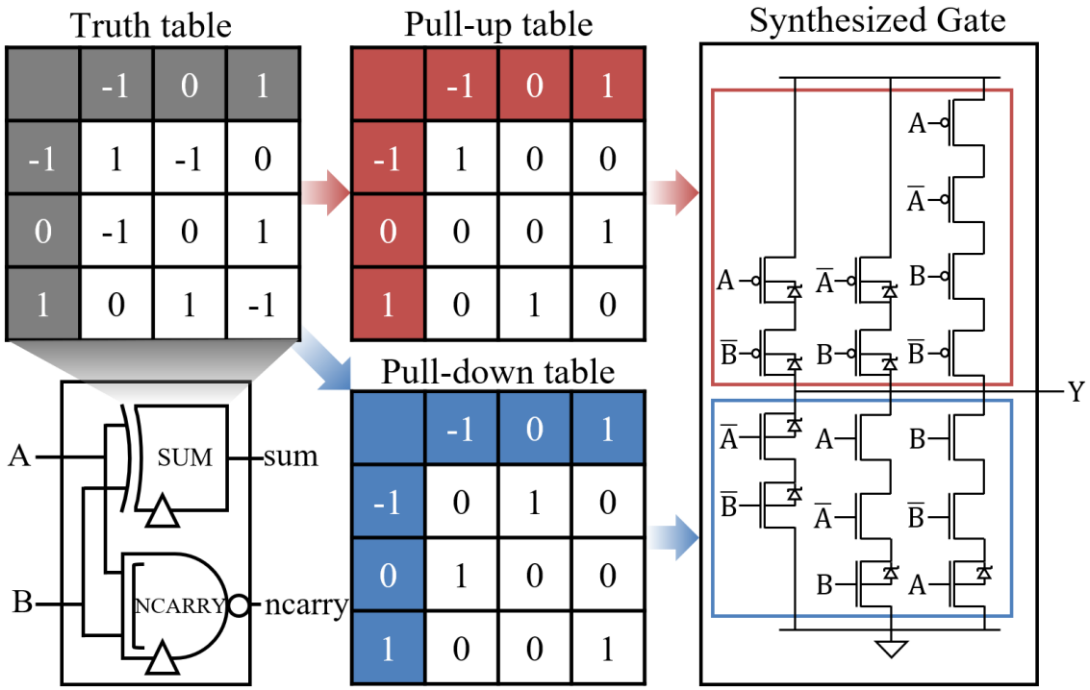
NMIN

- **All ternary logical operations can be designed with STI and NMIN.**
- **Only 1% of ternary logical operations are designed as 2-stage cascade.**
- **For efficient design of ternary circuit, more logic gates are needed.**

III. Methodology

- Optimal Gate Design

Optimal Gate Design Flow

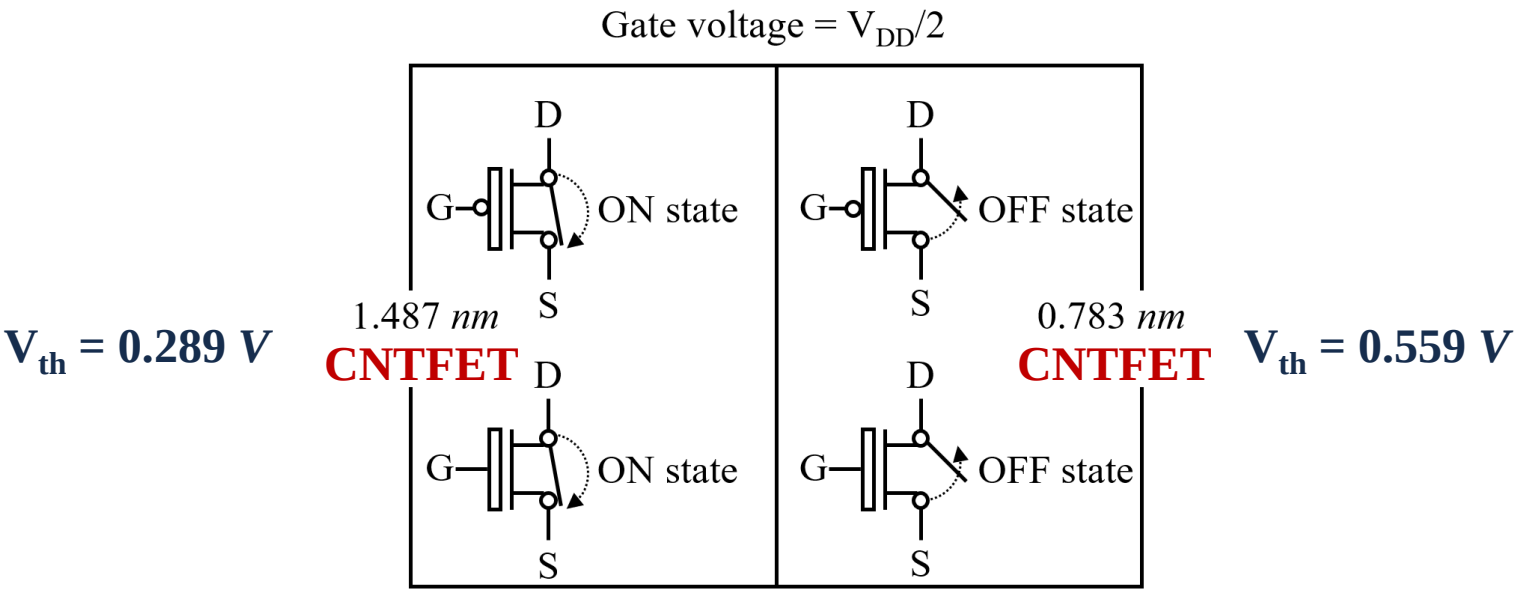


- **Design flow of the SUM gate for balanced ternary half adder**

1. **Building pull-up/down switching tables from the ternary truth table**

2. **Converting to a SOP expression, generating an optimal gate circuits**

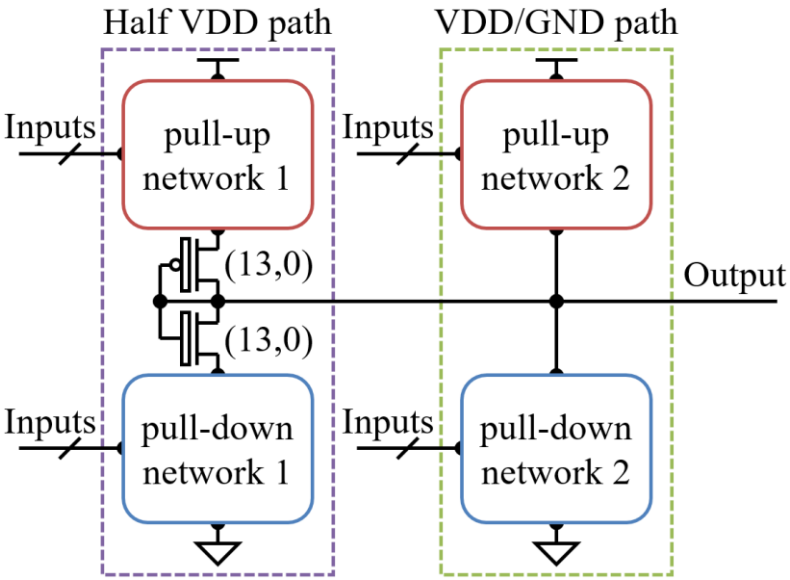
Ternary Devices

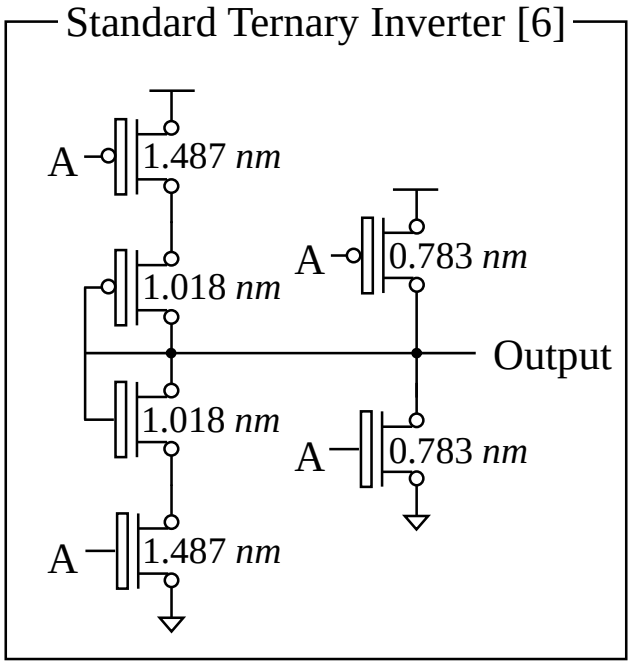


- The operation of ternary devices same @ the gate voltage = V_{DD}, GND.
- The operation of ternary devices differ @ the gate voltage = half V_{DD}.
- CNTFET uses two different diameter for different ON/OFF states.

[6] J. Deng et al., IEEE Trans. of Electron Devices, 2007

Generalized Structure of Static Ternary Gate



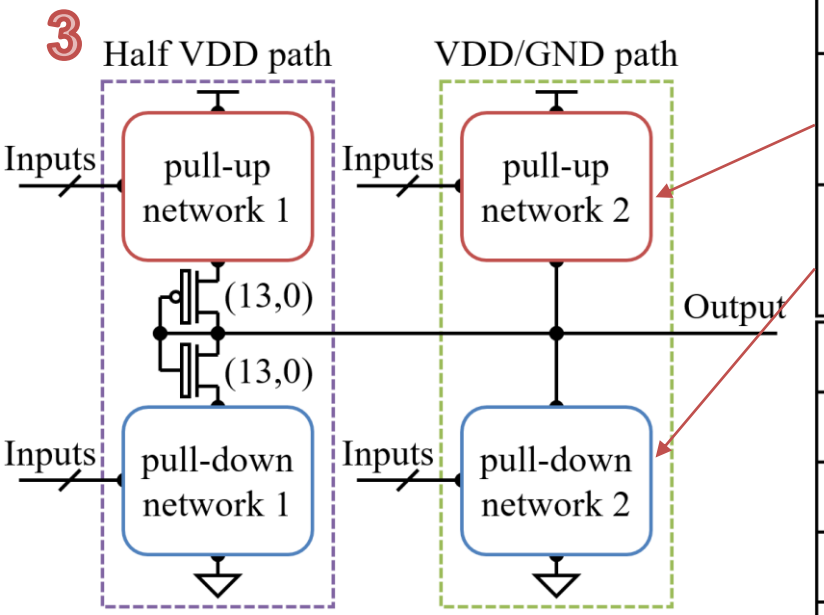


In	Out
0	2
1	1
2	0

- Generalize the structure of static ternary gate based on STI [6].
- V_{DD}/GND path generate logical 0 (GND) and logical 2 (V_{DD}).
- Half V_{DD} path is attached to generating logical 1 (half V_{DD}).

[6] S. Lin et al., IEEE Trans. of Nanotechnology., 2011

Ternary Gate Design Methodology



2 Ternary device switching table

Pull-up network	(19, 0) I 0.289 *V* 1.487 *nm*	(10, 0) I 0.559 *V* 0.783 *nm*	(19, 0) I_N 0.289 *V* 1.487 *nm*	(19, 0) I_P 0.289 *V* 1.487 *nm*
Pull-down network	(19, 0) I_P 0.289 *V* 1.487 *nm*	(19, 0) I_N 0.289 *V* 1.487 *nm*	(19, 0) I 0.289 *V* 1.487 *nm*	(10, 0) I 0.559 *V* 0.783 *nm*

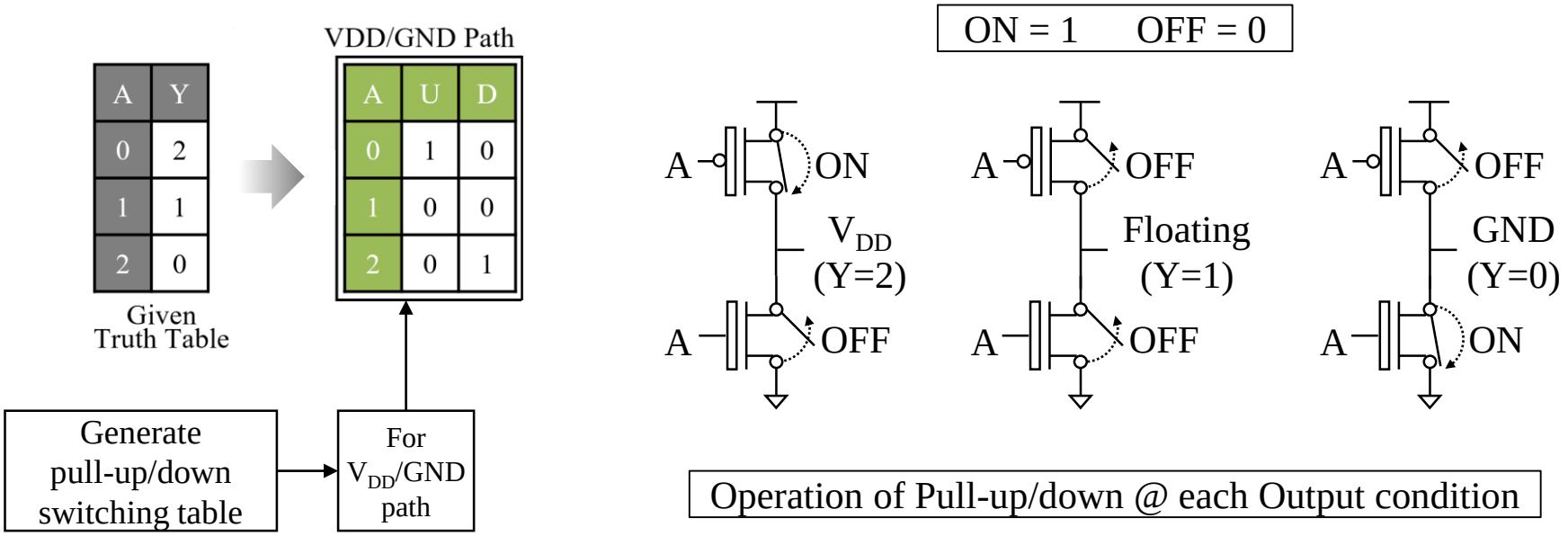
1 Switching operation

Input = 0	ON state	ON state	OFF state	OFF state
Input = 1	ON state	OFF state	ON state	OFF state
Input = 2	OFF state	OFF state	ON state	ON state
Operator	A_0+A_1	A_0	A_1+A_2	A_2

- **By input gate voltage (0, 1, 2), define different switching operations.**
- **Each switching operation have operator and P-type/N-type transistor.**
- **Use P-type/N-type ternary devices for pull-up/pull-down network.**

Example of Ternary Gate Design

- **Switching table of V_{DD}/GND path (STI)**



- **Output = 2 → Pull-up = 1 (ON-state), Pull-down = 0 (OFF-state)**
- **Output = 1 → Pull-up = 0 (OFF-state), Pull-down = 0 (OFF-state)**
- **Output = 0 → Pull-up = 0 (OFF-state), Pull-down = 1 (ON-state)**

Example of Ternary Gate Design

- **Switching table of Half V_{DD} path (STI)**

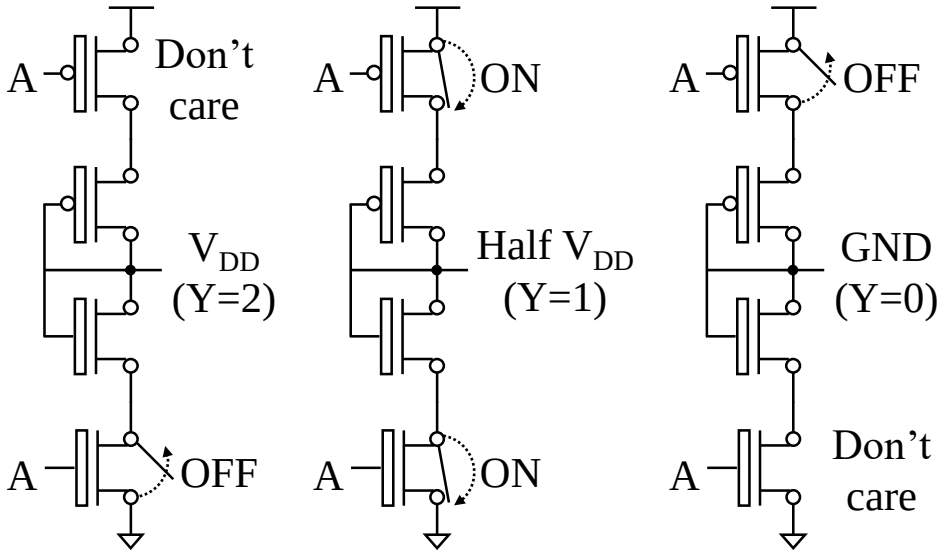
A	Y
0	2
1	1
2	0

Given Truth Table

	VDD/GND Path			Half VDD Path	
A	U	D	A	U	D
0	1	0	0	X	0
1	0	0	1	1	1
2	0	1	2	0	X

Generate pull-up/down switching table → For V_{DD}/GND path → For Half V_{DD} path

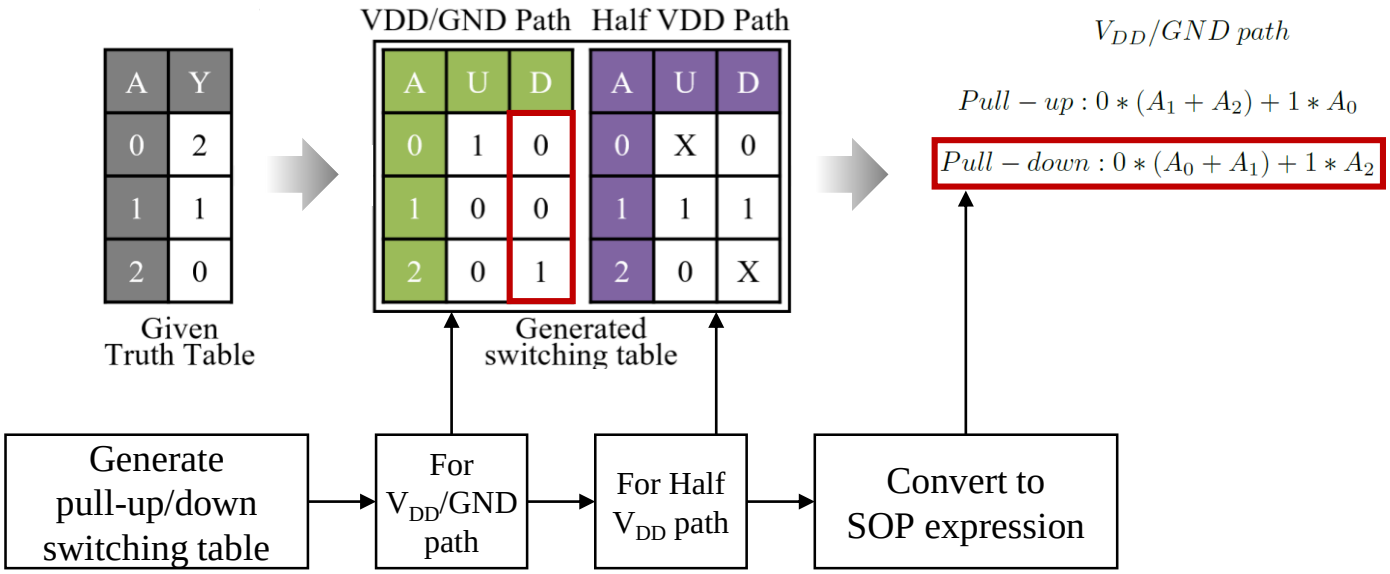
X = don't care



- **Output = 2 → Pull-up = X (don't care), Pull-down = 0 (OFF-state)**
- **Output = 1 → Pull-up = 0 (ON-state), Pull-down = 0 (ON-state)**
- **Output = 0 → Pull-up = 0 (OFF-state), Pull-down = X (don't care)**

Example of Ternary Gate Design

- **Sum of Product expression of switching table (STI)**



- **Convert from switching table to Sum of Product expression.**
- **$1*A_0 + 0*A_1 + 0*A_2$ @ Pull-up network**
- **$0*A_0 + 0*A_1 + 1*A_2$ @ Pull-down network**

Example of Ternary Gate Design

- **Don't care condition in SOP expression (STI)**

A	Y
0	2
1	1
2	0

Given Truth Table

VDD/GND Path | Half VDD Path

A	U	D	A	U	D
0	1	0	0	X	0
1	0	0	1	1	1
2	0	1	2	0	X

Generated switching table

$V_{DD}/GND\ path$

$Pull-up: 0*(A_1+A_2)+1*A_0$

$Pull-down: 0*(A_0+A_1)+1*A_2$

$Half\ V_{DD}\ path$

$Pull-up: 0*A_2+1*(A_0+A_1)$

$Pull-down: 0*A_0+1*(A_1+A_2)$

Generate pull-up/down switching table → For V_{DD}/GND path → For Half V_{DD} path → Convert to SOP expression

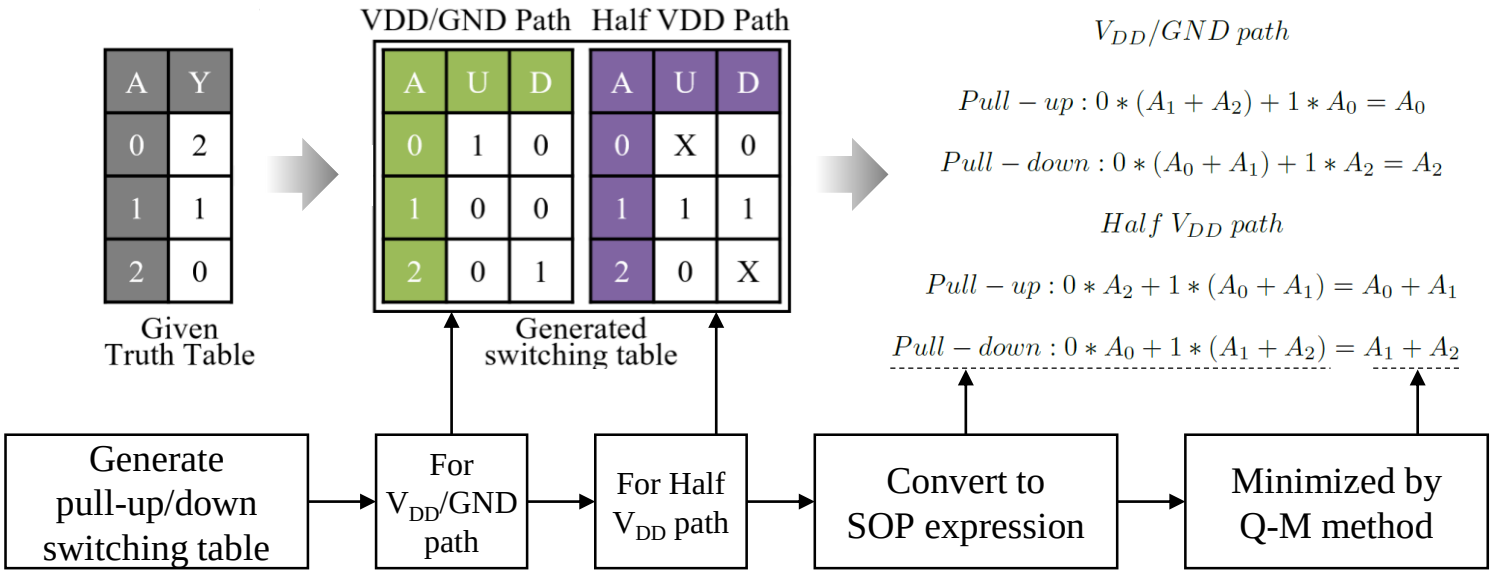
Ternary device switching table		
Pull-up network	(19, 0) I 0.289 V 1.487 nm	(19, 0) I_N 0.289 V 1.487 nm
Pull-down network	(19, 0) I_P 0.289 V 1.487 nm	(19, 0) I 0.289 V 1.487 nm

Switching operation		
Input = 0	ON state	OFF state
Input = 1	ON state	ON state
Input = 2	OFF state	ON state
Operator	A_0+A_1	A_1+A_2

- **Consider don't care condition to design a smaller circuit.**
- **X=1 @ Pull-up circuit → 1*A_0 + 1*A_1 + 0*A_2 → 1 transistor (Better)**
- **X=0 @ Pull-up circuit → 0*A_0 + 1*A_1 + 0*A_2 → 4 transistor (Worse)**

Example of Ternary Gate Design

- **Minimization of SOP expression (STI)**



- **When design a complex ternary gate, it is necessary to minimize the SOP expression of switching table.**
- **Use Q-M method to minimize a SOP expression.**

Example of Ternary Gate Design

- **Single input gate design (STI)**

Ternary device switching table				
Pull-up network	(19, 0) I 0.289 *V* 1.487 *nm*	(10, 0) I 0.559 *V* 0.783 *nm*	(19, 0) I_N 0.289 *V* 1.487 *nm*	(19, 0) I_P 0.289 *V* 1.487 *nm*
Pull-down network	(19, 0) I_P 0.289 *V* 1.487 *nm*	(19, 0) I_N 0.289 *V* 1.487 *nm*	(19, 0) I 0.289 *V* 1.487 *nm*	(10, 0) I 0.559 *V* 0.783 *nm*
Switching operation				
Input = 0	ON state	ON state	OFF state	OFF state
Input = 1	ON state	OFF state	ON state	OFF state
Input = 2	OFF state	OFF state	ON state	ON state
Operator	A_0+A_1	A_0	A_1+A_2	A_2

$V_{DD}/GND\ path$

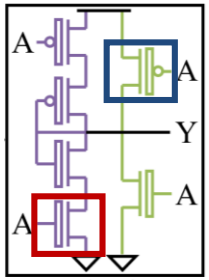
$Pull-up: 0*(A_1+A_2)+1*A_0 = A_0$

$Pull-down: 0*(A_0+A_1)+1*A_2 = A_2$

$Half\ V_{DD}\ path$

$Pull-up: 0*A_2+1*(A_0+A_1) = A_0+A_1$

$Pull-down: 0*A_0+1*(A_1+A_2) = A_1+A_2$



Synthesized Circuit

Convert to SOP expression → Minimized by Q-M method → Transistor Mapping Using Device Table

- **Finally, synthesize the circuit by mapping the transistor corresponding to each operator of the SOP expression in the device switching table.**

Example of Ternary Gate Design

- **Multi-Input gate design (SUM gate)**

	0	1	2
0	0	1	2
1	1	2	0
2	2	0	1

Given Truth table of SUM gate

VDD/GND path — Half VDD path

Pull-up table

U	0	1	2
0	0	0	1
1	0	1	0
2	1	0	0

U	0	1	2
0	0	1	X
1	1	X	0
2	X	0	1

Pull-down table

D	0	1	2
0	1	0	0
1	0	0	1
2	0	1	0

D	0	1	2
0	X	1	0
1	1	0	X
2	0	X	1

Generated switching table

$$V_{DD}/GND\ path$$

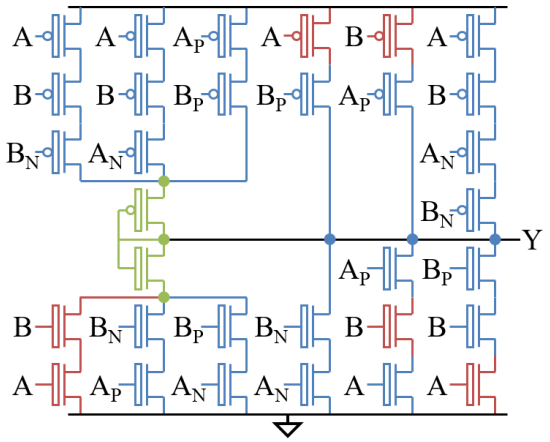
$$Pull-up : A_0 * B_2 + A_1 * B_1 + A_2 * B_0$$

$$Pull-down : A_0 * B_0 + A_1 * B_2 + A_2 * B_1$$

$$Half\ V_{DD}\ path$$

$$Pull-up : A_0 * (B_1 + B_2) + (A_1 + A_2) * B_0 + A_2 * B_2$$

$$Pull-down : A_0 * (B_0 + B_1) + (A_0 + A_1) * B_0 + A_2 * B_2$$



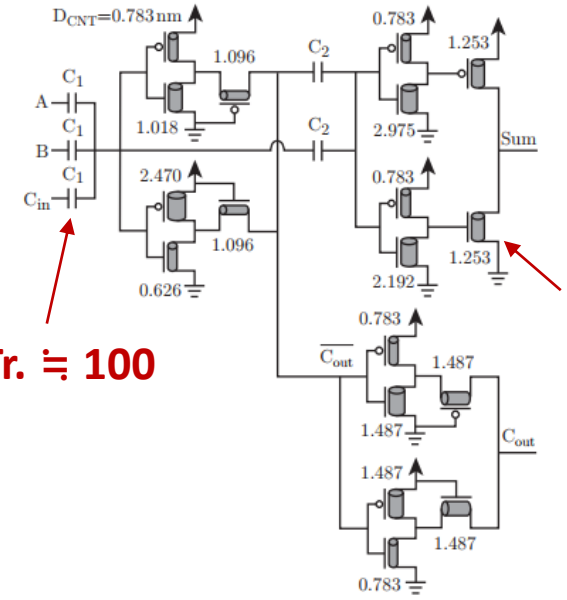
- **The methodology of a single input gate design can be applied to gate designs with more than two inputs.**

IV. Circuit Design

- Proposed Ternary Gate

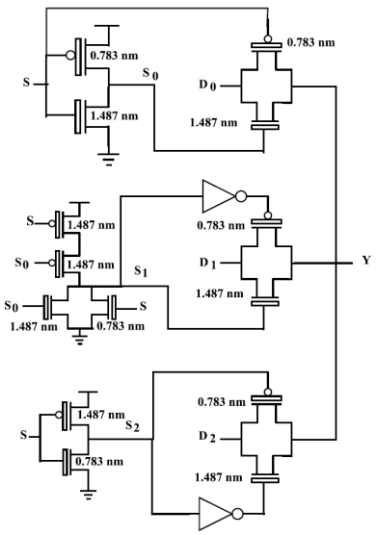
Previous Ternary Full Adder Design

- **Capacitor based Design [10]**
- **MUX based Design [7]**



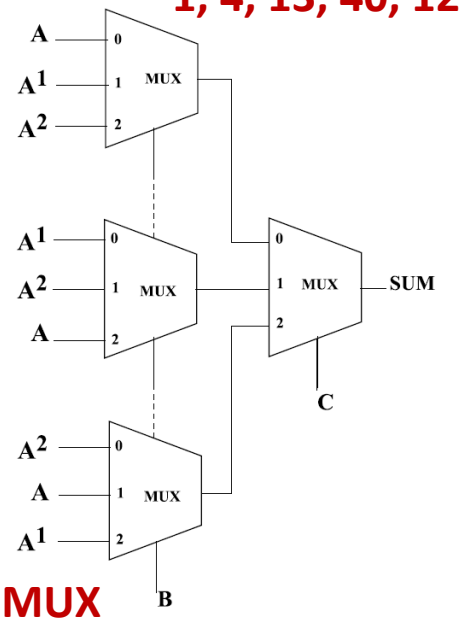
 # Tr. ≒ 100

Not a Static STI



Area increasing exponentially

1, 4, 13, 40, 121 …

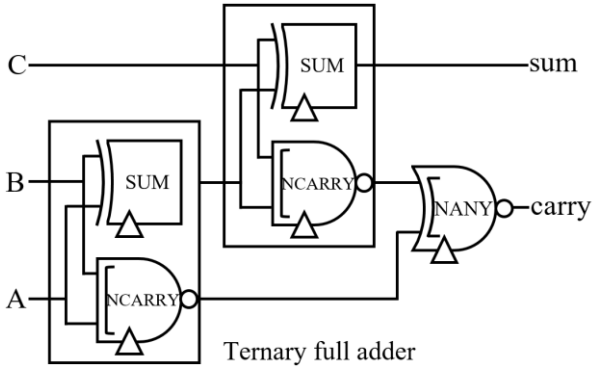


Couldn't build 3-stage only using MUX

- **Capacitor based design have worse power, speed, and area.**
- **MUX based design have worse power, speed and noise margin.**

[7] B. Srinivasu et al., IEEE TCAS-I 2017 [10] M. H. Moaiyeri et al., Nano-Micro Lett. 2011

Standard Ternary Full Adder



Half adder
# of tr. = 50

Full adder
# of tr. = 110

SUM gate

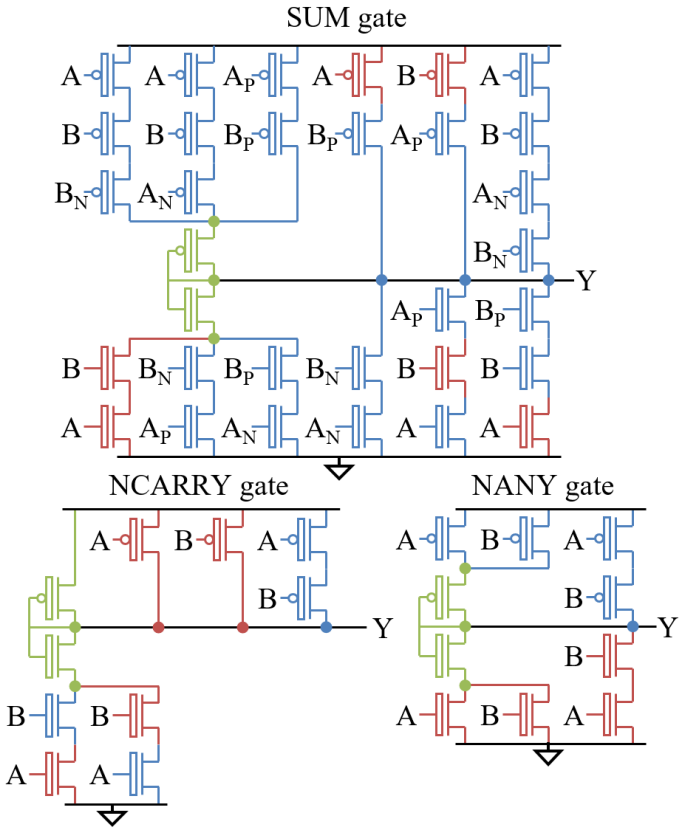
	0	1	2
0	0	1	2
1	1	2	0
2	2	0	1

NCARRY gate

	0	1	2
0	2	2	2
1	2	2	1
2	2	1	1

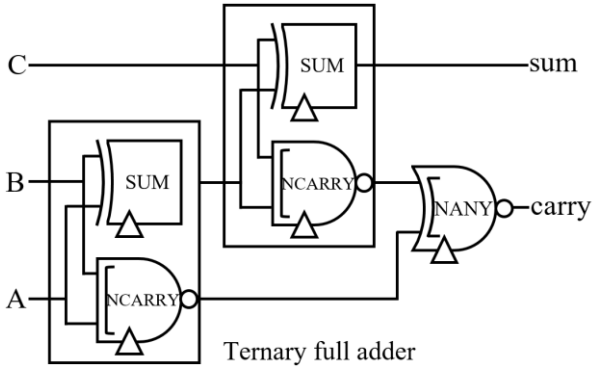
NANY gate

	0	1	2
0	2	2	1
1	2	2	1
2	1	1	0



- **Ternary half adder consists of one SUM gate and one NCARRY gate.**
- **Ternary full adder consists of two half adders and NANY gate.**

Balanced Ternary Full Adder



Half adder
# of tr. = 50

Full adder
# of tr. = 118

SUM gate

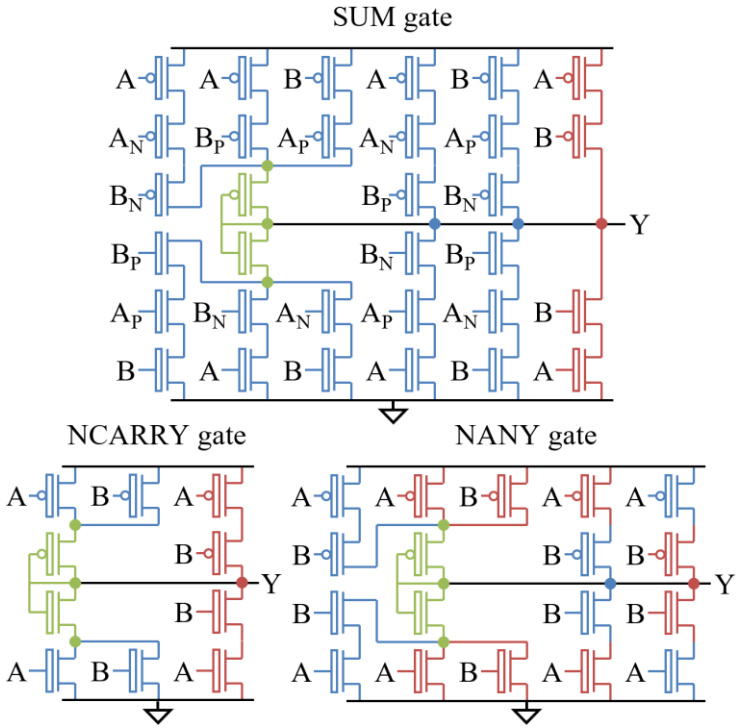
	-1	0	1
-1	1	-1	0
0	-1	0	1
1	0	1	-1

NCARRY gate

	-1	0	1
-1	1	0	0
0	0	0	0
1	0	0	-1

NANY gate

	-1	0	1
-1	1	1	0
0	1	0	-1
1	0	-1	-1



- **Signed ternary full adder is implemented without a sign trit.**
- **It is necessary for efficient design of signed ternary arithmetic logic.**

V. Simulation

- Efficiency of Method

Simulation Condition

- SYNOPSYS HSPICE circuit simulator are used.
- CNTFET compact model and it's default parameter are used.
- Transistor sizing is not applied.
- Operation voltage (V_{DD}) is 0.9 V.
- Transition time is 10 ps.
- Calculated characteristic using input patterns of [11].
  - Worst delay
  - Average power
  - Power delay product (PDP) = worst delay * average power
- Previous designs were simulated in the same simulation environment.
- Simulation results were normalized based on the proposed design.

[11] P. Keshavarzian et al., CSSP 2014

Flow Chart & Function Table

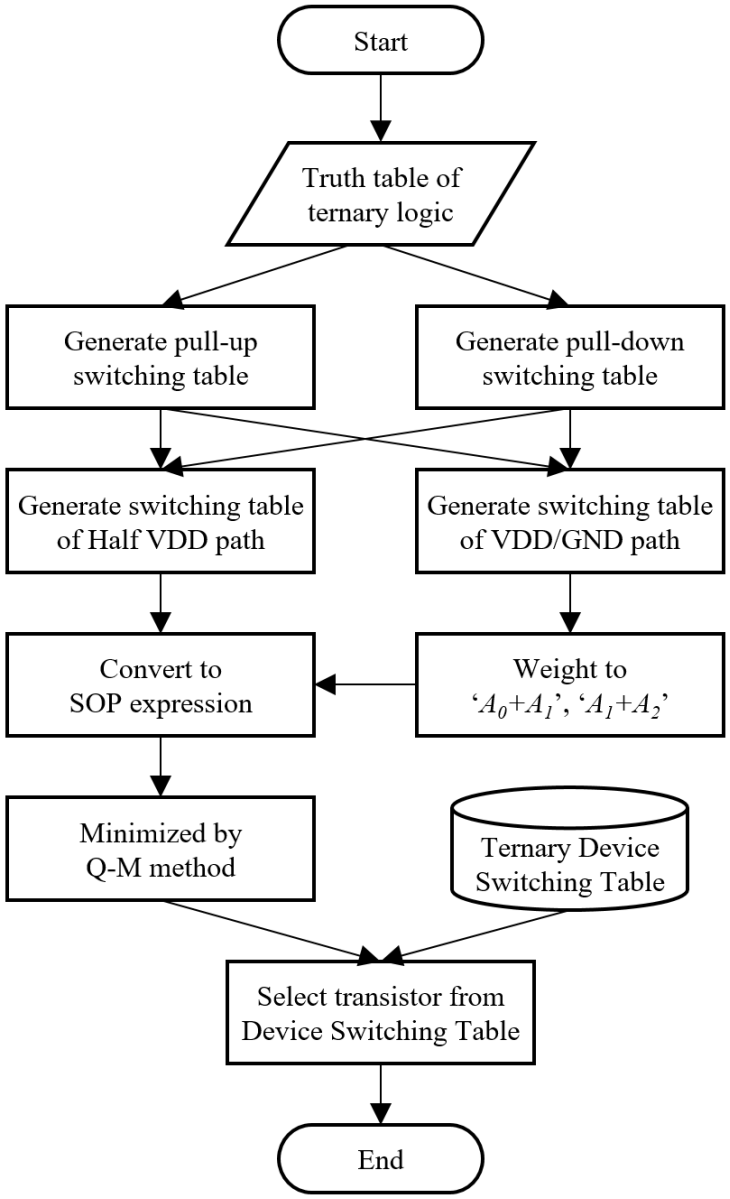


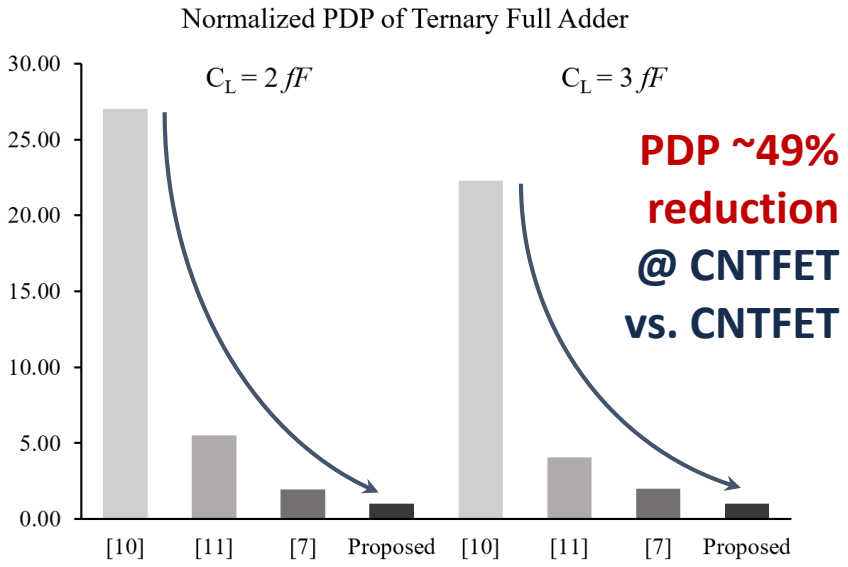
TABLE I
FUNCTION OF TERNARY LOGIC GATE

Logic	Design	Gate	Function
Unsigned ternary logic	Full adder	SUM	$Sum(A,B) = (A+B)\ mod\ 3$
		NCARRY	$NCarry(A,B) = \begin{cases} 1, & A+B \geq 3 \\ 2, & otherwise \end{cases}$
		NANY	$NAny(A,B) = \begin{cases} 0, & A = B = 2 \\ 2, & A \neq 2\ and\ B \neq 2 \\ 1, & otherwise \end{cases}$
	Multiplier	PRODUCT	$Prod(A,B) = (A \cdot B)\ mod\ 3$
		CARRY	$Prod\ Carry(A,B) = \begin{cases} 1, & A = B = 2 \\ 0, & otherwise \end{cases}$
Signed ternary logic	Full adder	SUM	$Sum(A,B) = \begin{cases} -1, & A+B > 1 \\ 1, & A+B < -1 \\ A+B, & otherwise \end{cases}$
		NCARRY	$NCarry(A,B) = \begin{cases} -1, & A = B = 1 \\ 1, & A = B = -1 \\ 0, & otherwise \end{cases}$
		NANY	$NAny(A,B) = \begin{cases} -1, & A+B > 0 \\ 1, & A+B < 0 \\ 0, & otherwise \end{cases}$
	Multiplier	PRODUCT	$Prod(A,B) = A \cdot B$

Ternary Full Adder

TABLE II
COMPARISON OF TERNARY FULL ADDER DESIGN

Design	Load Cap. (*fF*)	Normalized Delay	Normalized Power	Normalized PDP
[10]	2	1.58	16.98	27.02
[10]	3	1.30	17.05	22.31
[11]	2	0.93	5.90	5.49
[11]	3	0.66	6.15	4.06
[7]	2	0.71	2.76	1.96
[7]	3	0.73	2.70	1.98
Proposed	2	1.00	1.00	1.00
Proposed	3	1.00	1.00	1.00



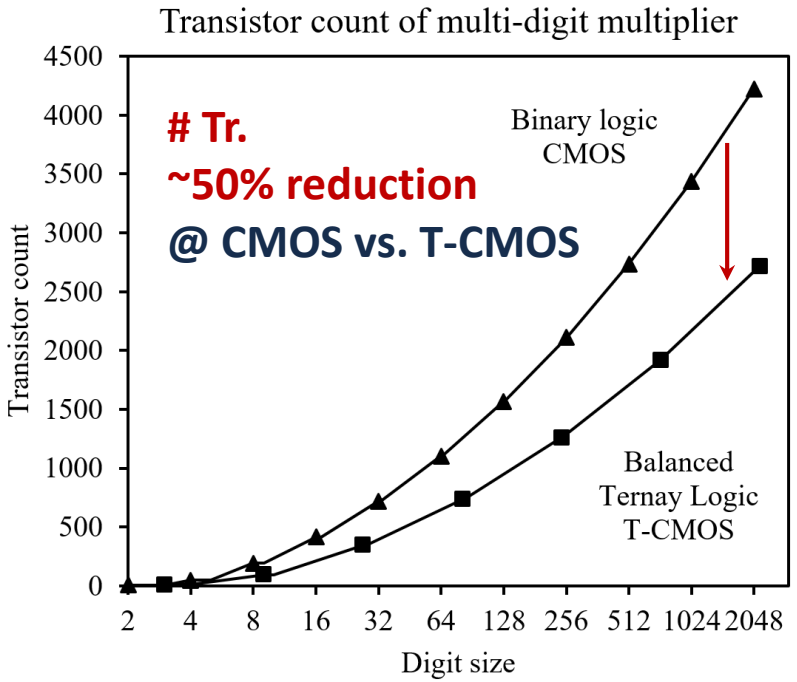
- Power-delay-product (PDP) of ternary full adder is reduced by 49.24 %.
- Because it is an optimal static gate, power consumption is very low.
- During voltage dividing (half V_{DD}), the delay of static gate increases.

Ternary Multiplier

TABLE III
COMPARISON OF TERNARY MULTIPLIER DESIGN

Design	Load Cap. (fF)	Normalized Delay	Normalized Power	Normalized PDP
[7]	2	1.03	2.63	2.71
[7]	3	1.02	2.47	2.53
Proposed	2	1.00	1.00	1.00
Proposed	3	1.00	1.00	1.00

PDP ~61% reduction
@ CNTFET vs. CNTFET



- **We design a ternary multiplier using our methodology.**
- **Power-delay-product (PDP) of ternary multiplier is reduced by 61.78 %.**
- **When using T-CMOS, # of tr. is reduced by 50% compared to CMOS.**

VI. Conclusion

Conclusion

- We propose an optimal gate design methodology for the synthesis of ternary circuits.
- We have modeled the characteristics of emerging ternary devices.
- Our proposed methodology can be applied to emerging devices that support ternary logic (e.g., CNTFET, T-CMOS).
- Our proposed methodology can be applied to not only standard ternary logic but also balanced ternary logic.

THANK YOU