Department of Electrical Engineering, National Central University
Electronic Design Automation Laboratory (EDA LAB)

Performance-Preserved Analog Routing Methodology via Wire Load Reduction

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Outline

- Introduction
- Problem Formulation
- Algorithm
- Experimental Results
- Conclusion

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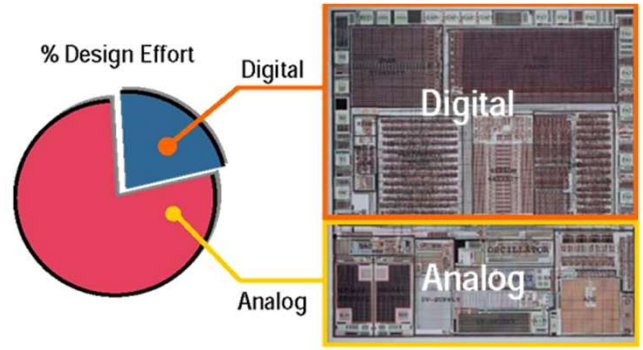
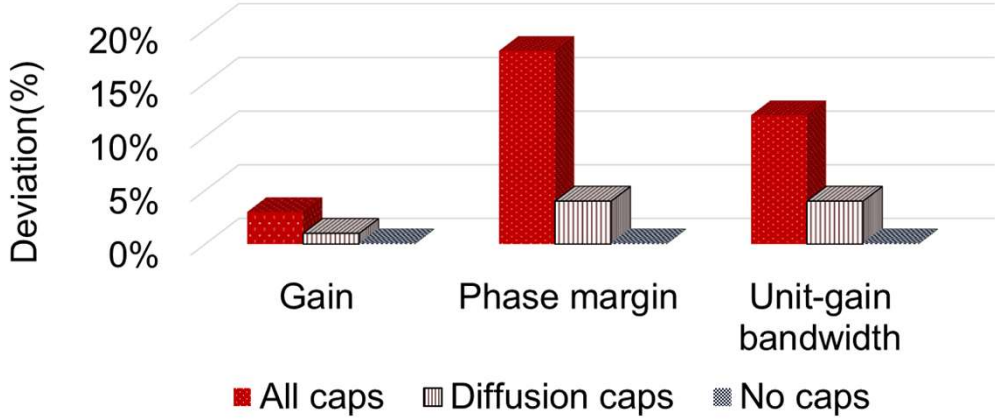
Analog Design Flow

- Advance process makes analog components more sensitive
  - Layout effects impact circuit performance [2]



Commercial Mixed Signal ASIC [1]



- Analog EDA tools need to be enhanced to deal with non-ideal effects

[1] R.A Rutenbar, "Design Automation for Analog: The Next Generation of Tool Challenges" 1st IBM Academy Conference on Analog Design, Technology, Modeling and Tools, IBM T.J. Waston Research Labs 2006
[2] A. Agatwal, et al., "Fast and accurate parasitic capacitance models for layout aware synthesis of analog circuits", in Proceedings DATE, 2000.

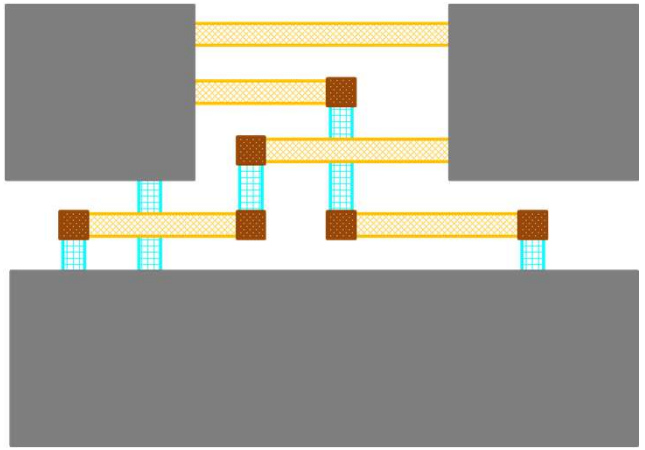
Analog Layout Design

- Impact circuit performance significantly
  - Topology constraints
  - Parasitic effects
- How to keep the performance during layout
  - Placement
    - Topology constraint (ex. symmetry, proximity)
  - Routing
    - Parasitic effects(ex. wire length, via numbers)
    - Topology constraint (ex. symmetry)

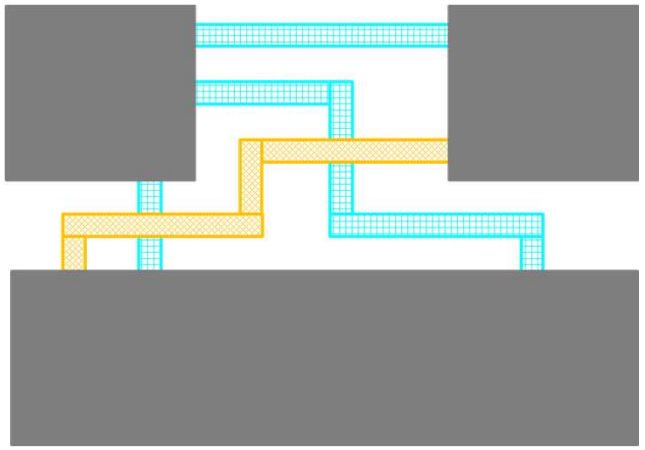
Traditional Routing Methodology

- Suitable for analog circuits?
  - ➢ Have lots of via in a single net
  - ➢ More via, more resistance
- Routing Method Comparison
  - ➢ Post-layout result fails to meet the spec
    - ☐ Two-stage OPA in 0.18μm

	Spec	Pre-sim	HV	This work
Gain(dB)	>80	81.8	77.7	80.5
GB(MHz)	>20	22.2	19.8	21



HV



This work

Contribution

- Present an analog routing method with wire resistance consideration
  - Propose a crossing-aware initial routing
  - Propose an analog routing algorithm considering wire load as well as wire length
  - Propose a resistance minimization method in layer assignment stage
- Post-layout performance is improved to HV result

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Problem Formulation

INPUT

- Placement result
- Netlist
- Pin locations
- Design rule
- Wires and vias Resistance

OBJECTIVE

- Minimize wire load
- Minimize wire length
- Minimize the via usage

Analog Routing Flow

Net decomposition

Crossing-aware initial routing

Routing path legalization

Layer assignment

Layout fine-tune

OUTPUT

- Route all the nets complete
- Routing result without DRC error

POST LAYOUT

- Keep the circuit performance
- Smaller wire load than HV routing

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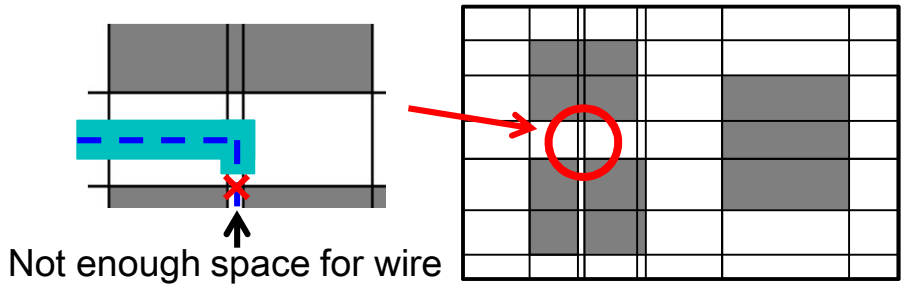
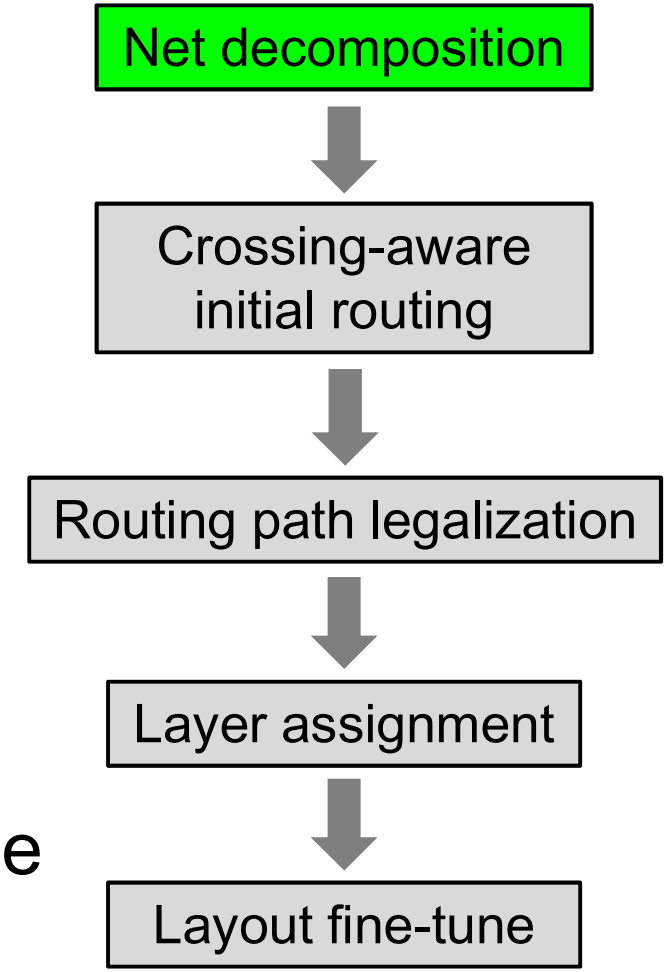
Net Decomposition

- Routing Graph Construction
  - Build G by obstacle boundaries
  - Analyze $g_{i,j}$ width and length
    - Width (length) ≥ $d + w$



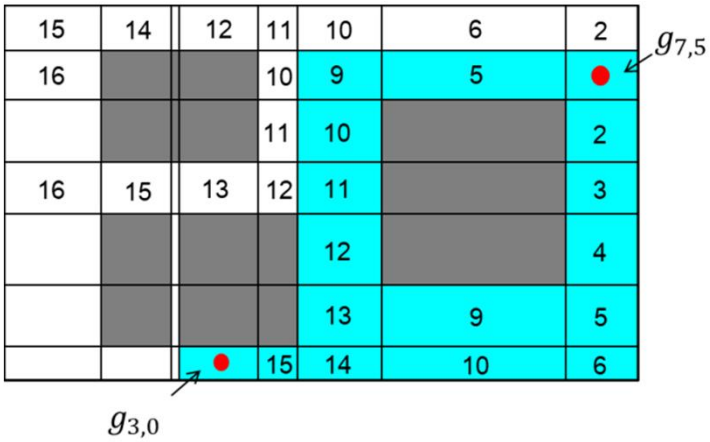
- Break multi-terminal into 2 pins
  - Use FLUTE[4] generate Steiner tree
  - Move Steiner points out of obs.

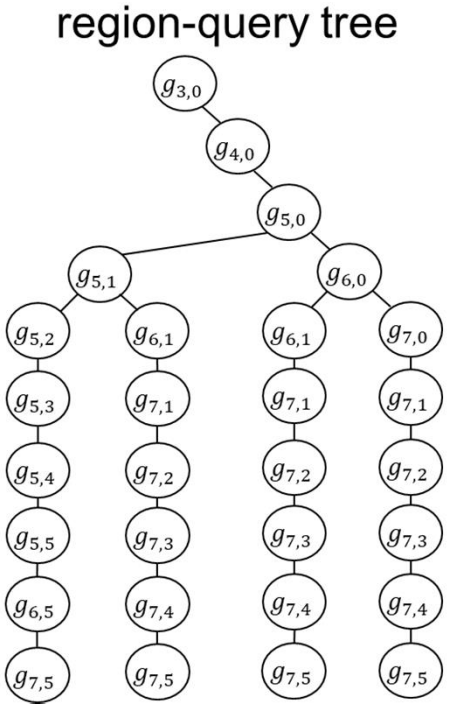


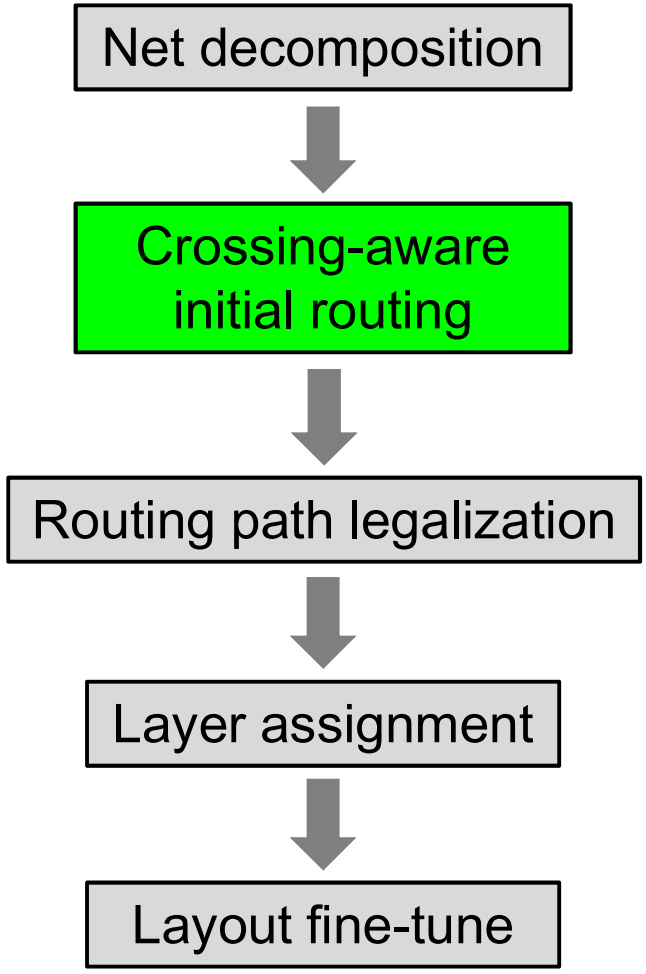
[4] C. Chu and Y. C.Wong, "FLUTE: Fast Lookup Table-based Rectilinear Steiner Minimal Tree Algorithm for VLSI Design," IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, 2008.

Crossing-Aware Initial Routing (1/2)

- Weighted Lee Algorithm
  - Search all possible routing solution
- Build up routing region
  - Region-query tree

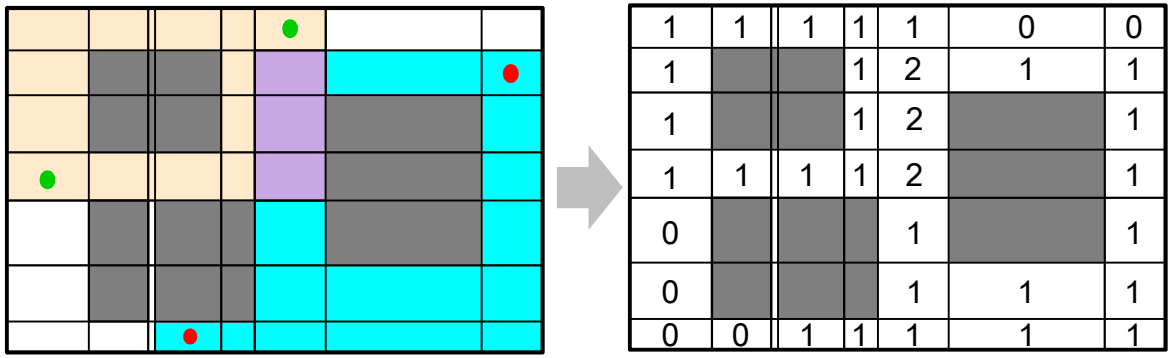




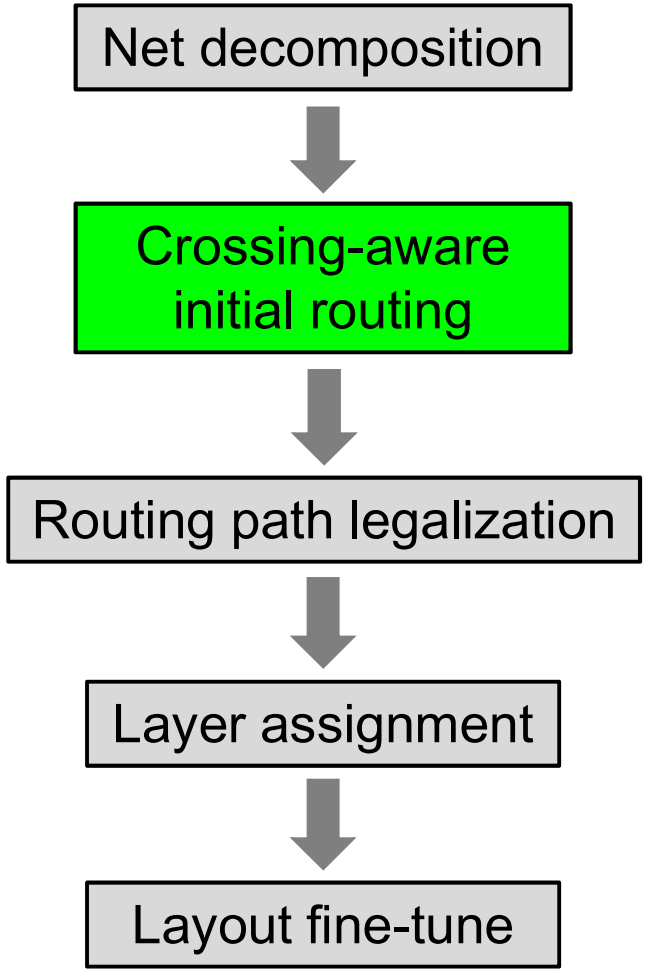


Crossing-Aware Initial Routing (2/2)

- Calculate Routing Occupancy
  - How many nets will pass this $g_{i,j}$



- Crossing consideration
  - Smaller occupancy, less crossing
  - Route the net with $\sum g_{i,j}$(occup.)
  - Update occupancy in routing region



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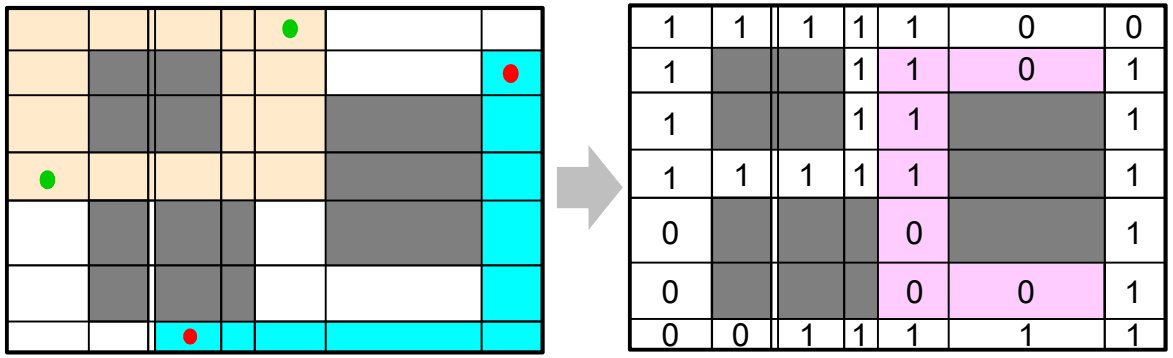

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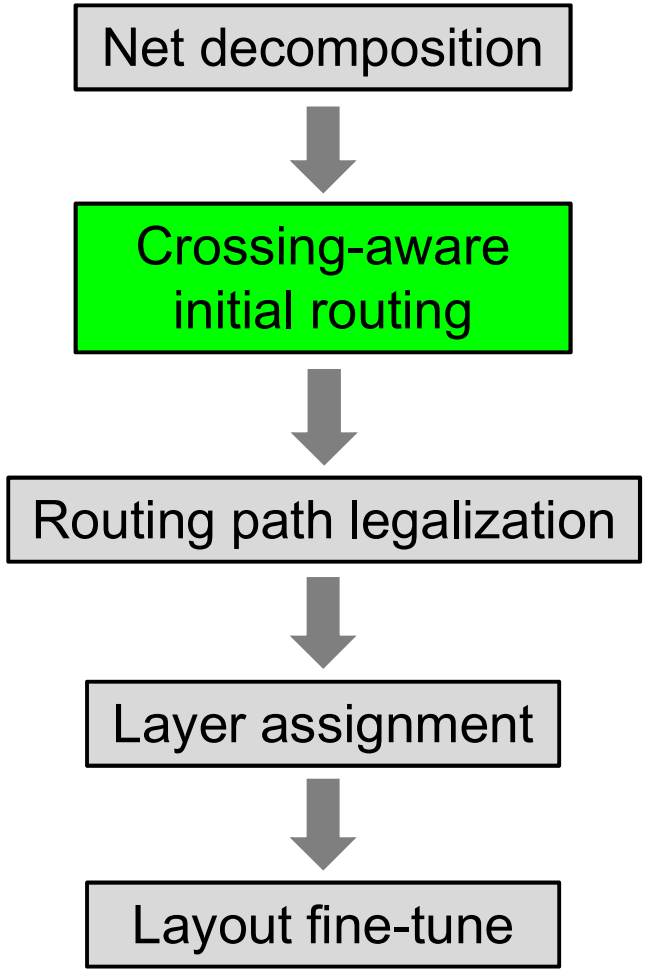
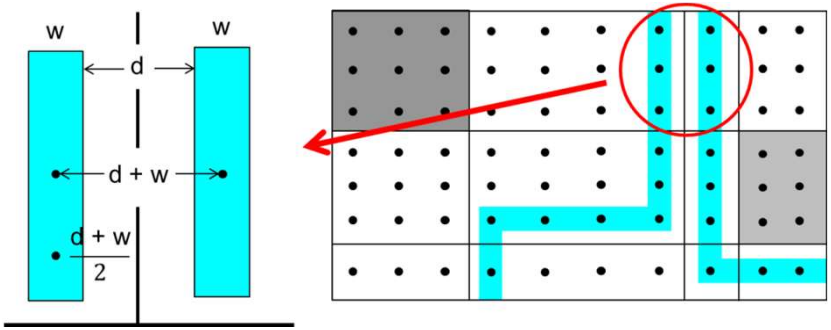


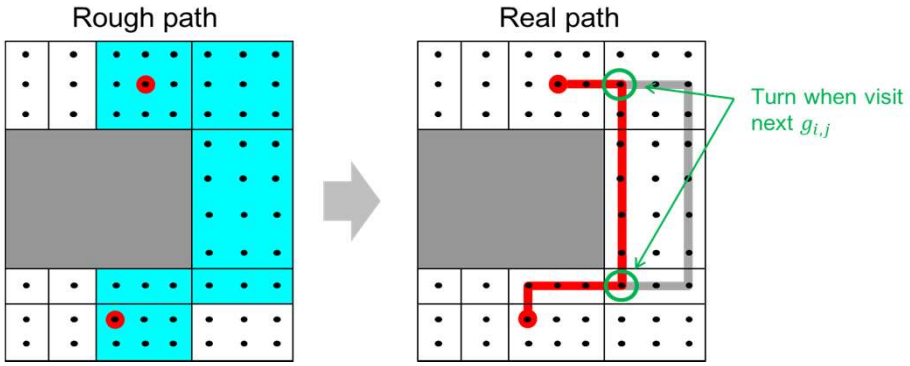
Routing Path Legalization

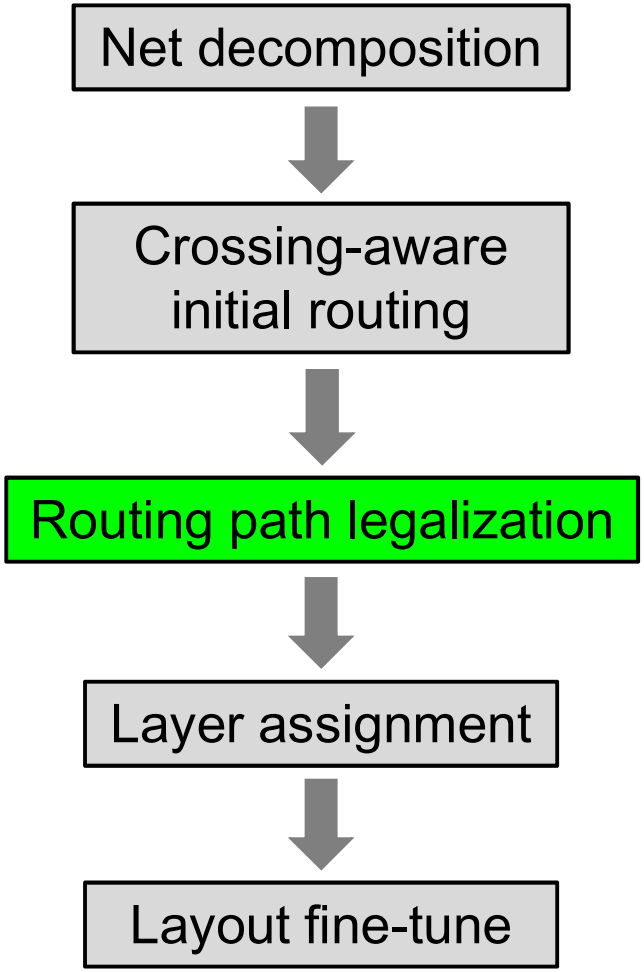
- Construct the routing graph
  - More finer grid D in $g_{i,j}$

* D to $D \geq d + w$



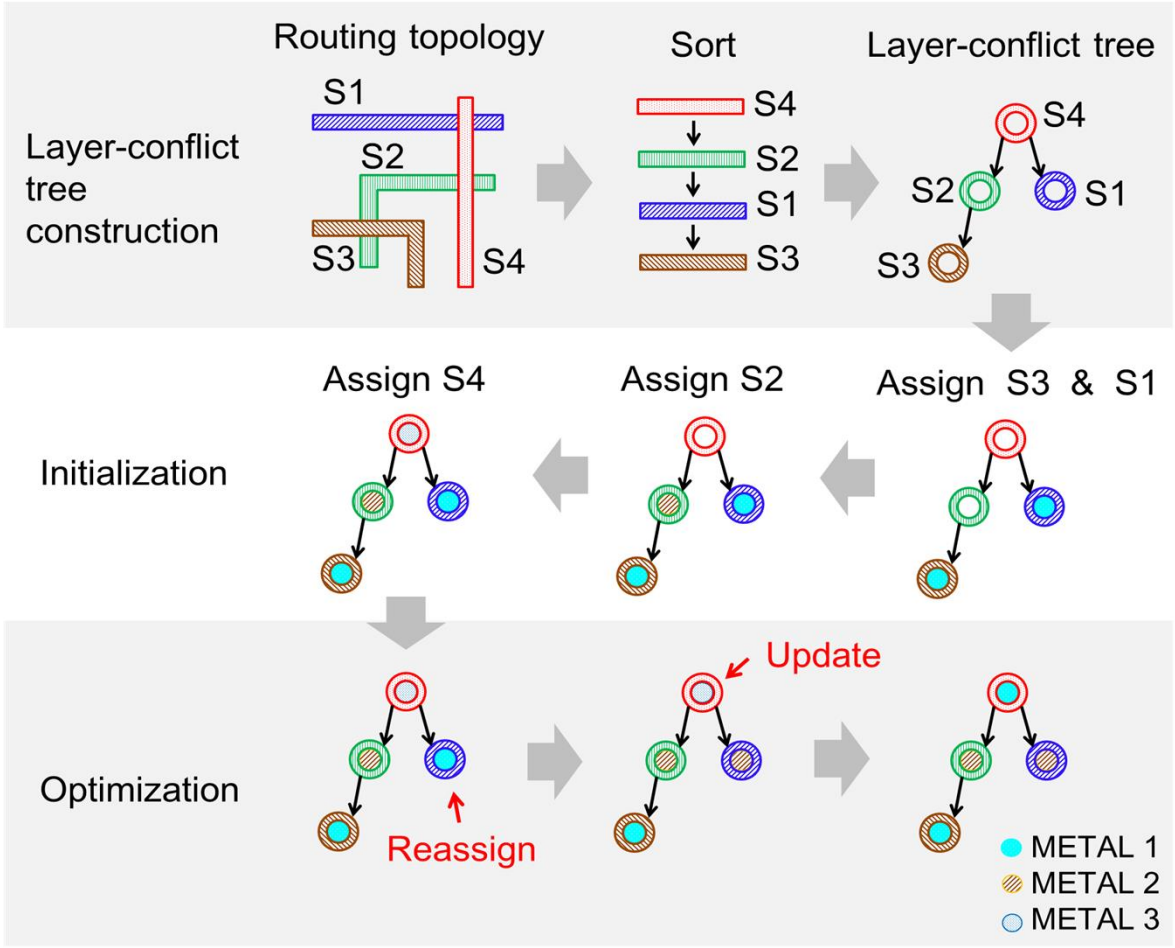
- Route the real path for each net

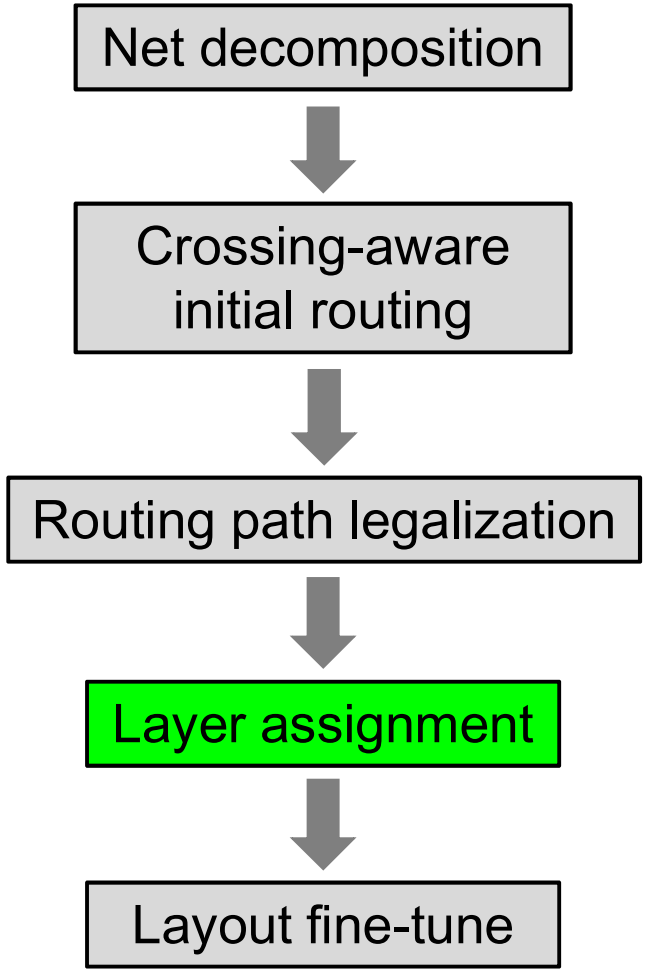




Layer Assignment

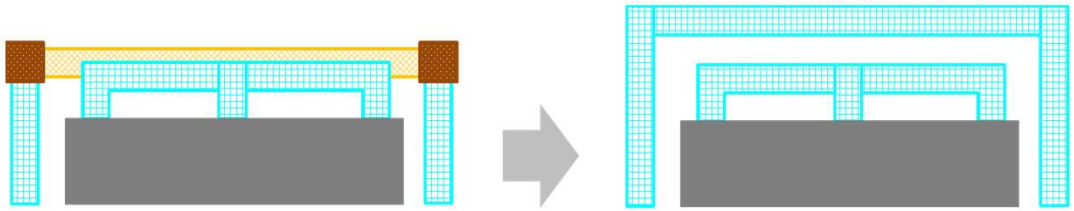
- Assign layer with minimal layers



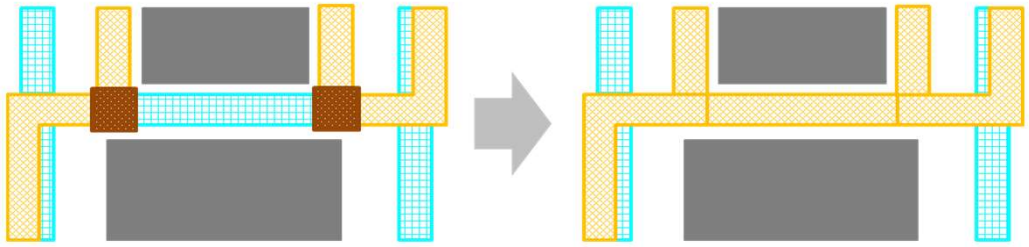


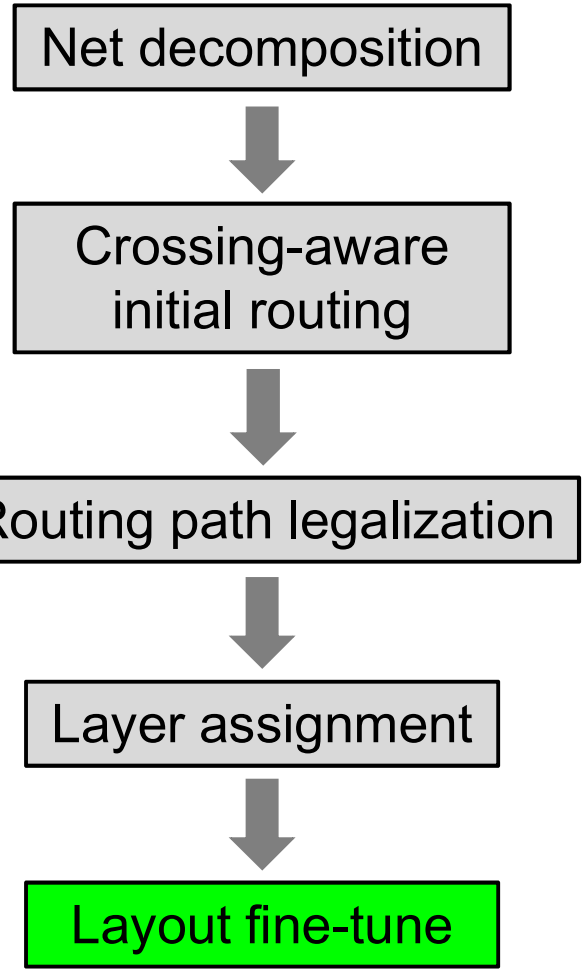
Layout Fine-Tune

- Wire load consideration
  - Reroute multilayer nets
    - $L_{ext} = n_{via} * R_{via}/R_{wire}$
    - $L_{new} = L_{ext} + L_{old}$



  - Reassign layer to reduce via
    - $C_{via} = \sum net_i(n_{via})$





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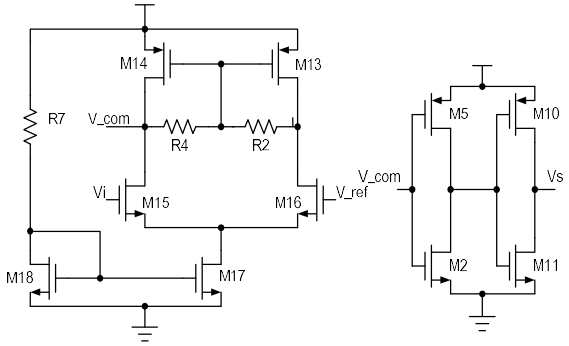
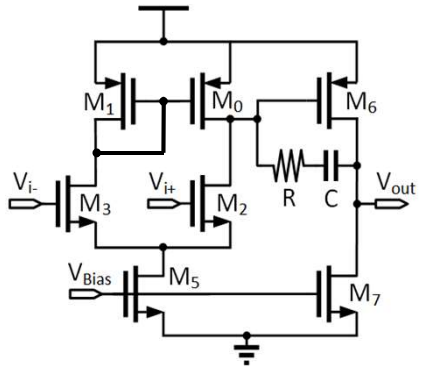
Environment and Test Circuits

- Programming language, Processor & Memory
  - C++, Intel Xeon 3.5GHz and 64GB memory
- Test case with 0.18μm process
  - Two-stage OPA, comparator

Circuit name	# of blocks	# of nets	# of pins	Total area (μm^2)
Two-stage OPA	17	5	26	521.13
Comparator	13	9	65	1318.94



Comparator



Two-stage OPA

Two-stage OPA

Spec.	Pre-sim	Post-sim			Comparison		
		Manual	HV	This	Manual	HV	This
Gain≥ 80(dB)	82	81.5	79.2	81.3	-0.6%	-3.4%	-0.8%
GB ≥ 40(MHz)	45	43	39.3	43	-4.4%	-12.6%	-4.4%
PM ≥ 60 (°)	60	65	62	65	+8.3%	+3.3%	+8.3%
SR ≥ 40(V/μs)	40.2	42	41.5	42	+4.4%	+4.1%	+4.4%
Total wire length(μm)	-	67.6	81.8	78.9	1	1.21	1.17
*Via Usage	-	36	55	31	1	1.52	0.86
Total wire resistance	-	44.2	136.4	48.9	1	2.08	1.11

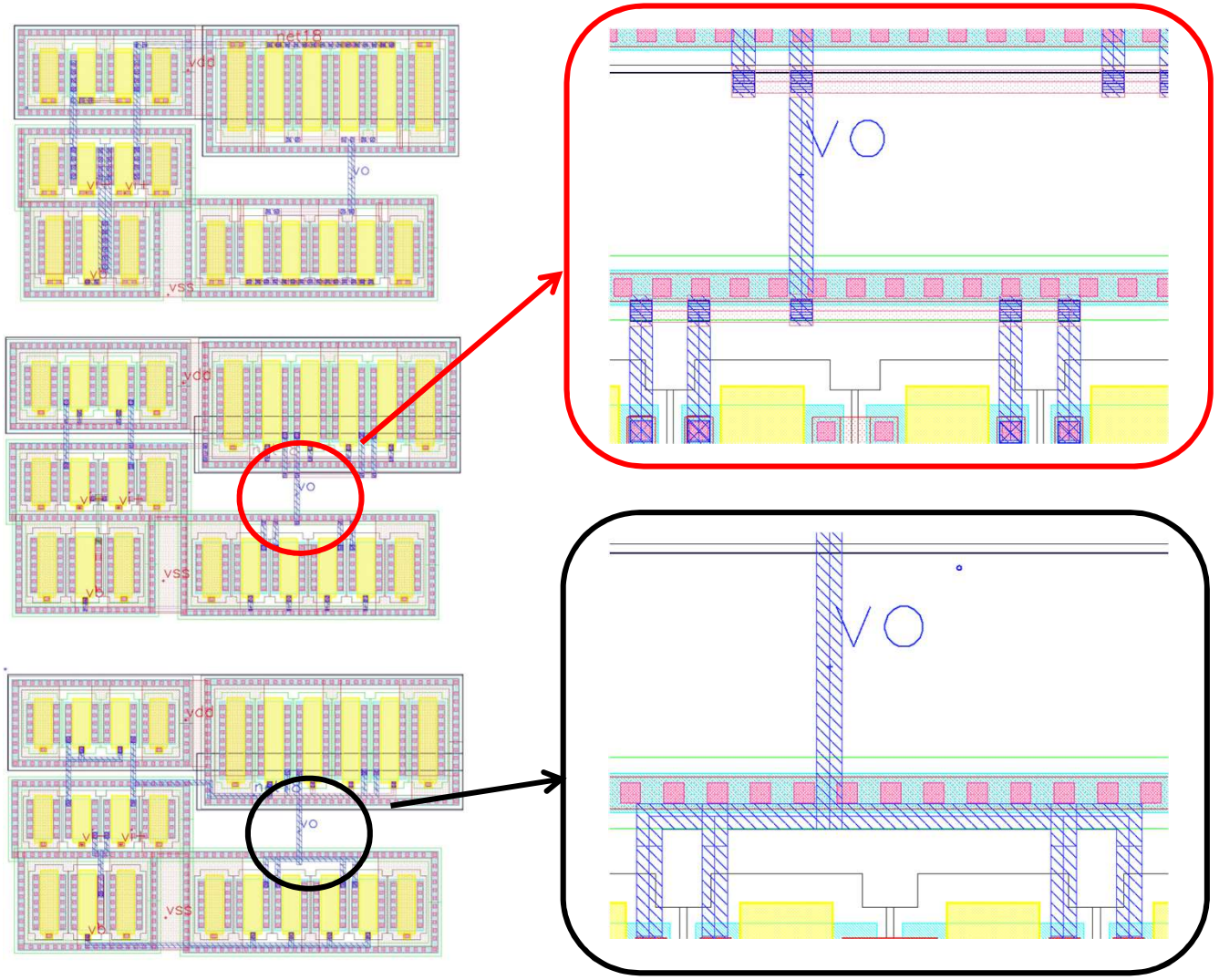
* The double vias at the same location are counted only once

Layout Comparison (OPA)

Manual

HV

This work

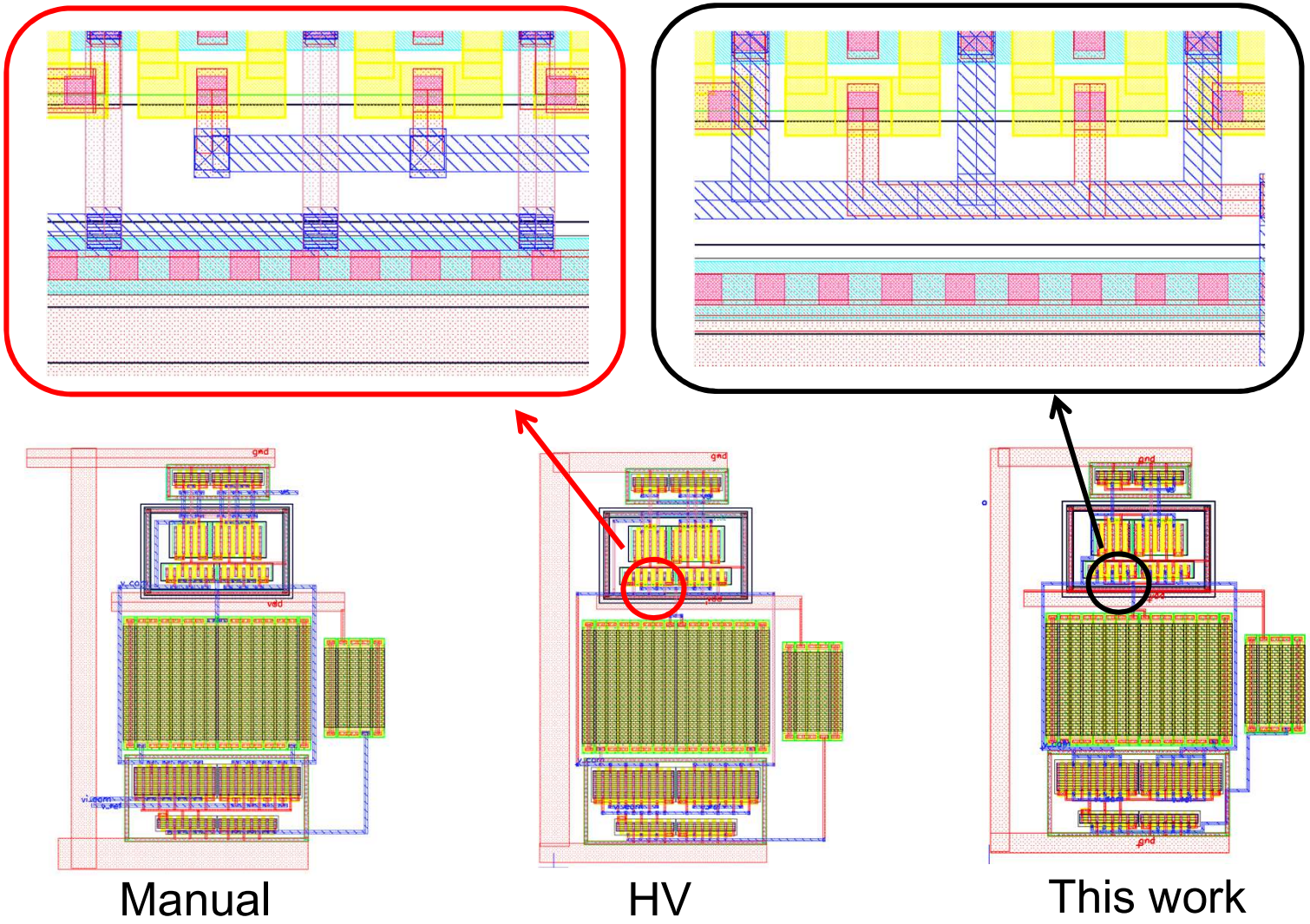


Comparator

Spec	Pre-sim	Post-sim			Comparison		
		Manual	HV	This	Manual	HV	This
Gain≥ 30(dB)	30.8	30.9	30.8	30.9	+0.3%	0%	+0.3%
GB ≥ 70(MHz)	70.8	72.4	71.1	73.2	2.2%	1.4%	3.3%
PM ≥ 60 (°)	60	60	60	60	0%	0%	0%
Power ≤ 0.25(mW)	0.23	0.21	0.21	0.21	-8.7%	-8.7%	-8.7%
Total wire length(μm)	-	272.94	273.85	268.55	1	1.003	0.984
*Via Usage	-	57	117	44	1	2.05	0.77
Total wire resistance	-	89.7	172.4	70.6	1	1.92	0.78

* The double vias at the same location are counted only once

Layout Comparison (Comparator)



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Conclusion

- Propose a routing algorithm that tries to minimize wire load instead of wire length
- Reduce crossing in initial routing stage
- Reduce the via usage and wire load in the layer assignment stage
- The performance loss after layout is significantly reduced with the proposed routing approach

Thanks for your listening