

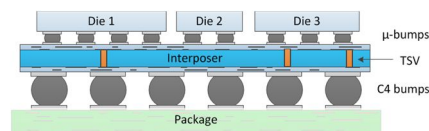
Optimal Die Placement for Interposer-Based 3D ICs

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Igor L. Markov and Jens Lienig

Jeju, Korea, Jan 24 2018

Outline

1. Motivation
2. Optimal placement framework (branch and bound)
3. Advanced pruning techniques
4. Results and Summary



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Part 1

Why 3D Integration? Why Interposer-based Chips and their Placement?

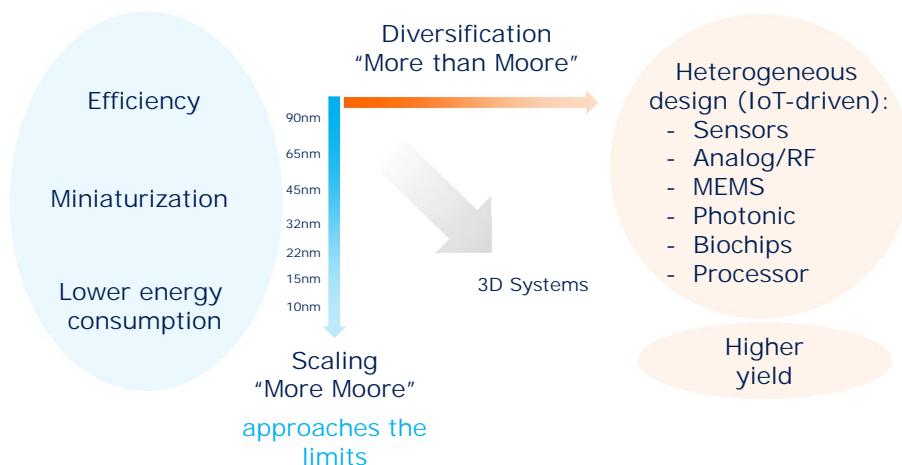
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Modern Requirements for Chip Design



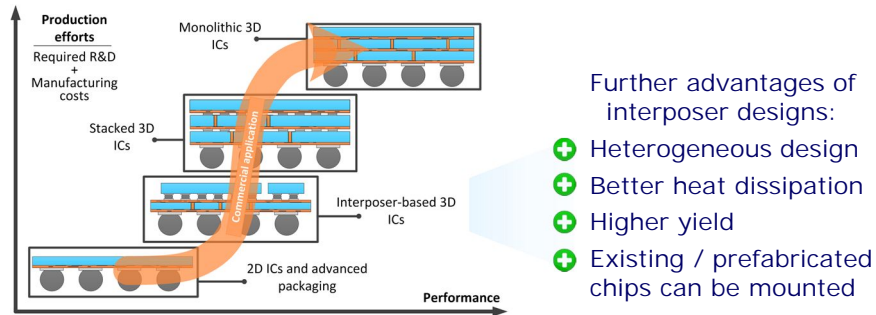
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Advantages of Interposer-Based 2.5/3D ICs



- Interposer-based 3D ICs are currently the most promising option for large-scale 3D integration

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Problem of Interposer Placement

Given:

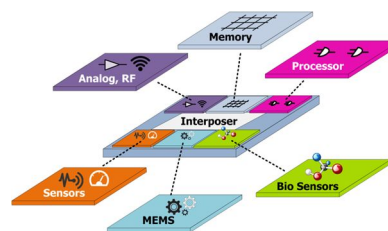
- Prefabricated chips/dies with fixed pins
- Geometry of interposer with defined placement region
- Netlist

Goal:

- Placement with minimal wirelength

Only a few dies need to be placed

- optimal arrangement is accessible but challenging (combinatorial explosion)



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Part 2

Optimal Placement Framework

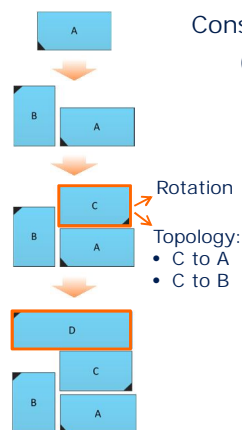
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Placement Framework: Representation



Construct placement by adding dies one at a time
(based on constraint satisfaction problem,
constraint graphs, and search trees)

For every new die we consider:

- Rotation: north (0°), west (90°), south (180°) and east (270°)
- Topological relation to already placed dies: left of / right of / above / below
- Optimal movement within deadspace

➤ All possible placement variations can be covered

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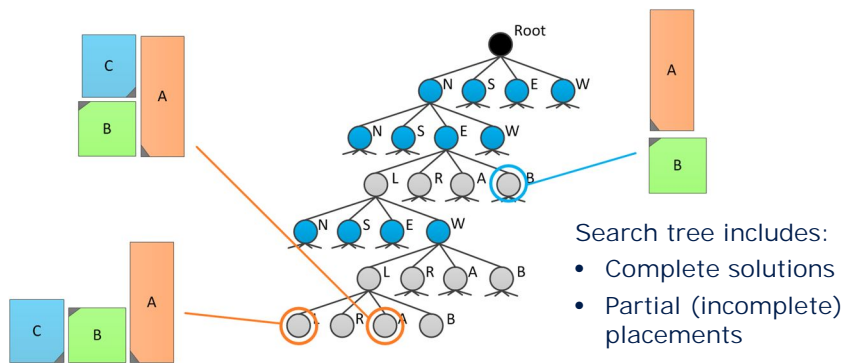
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Placement Framework: Search Tree

Incremental placement procedure is based on search tree



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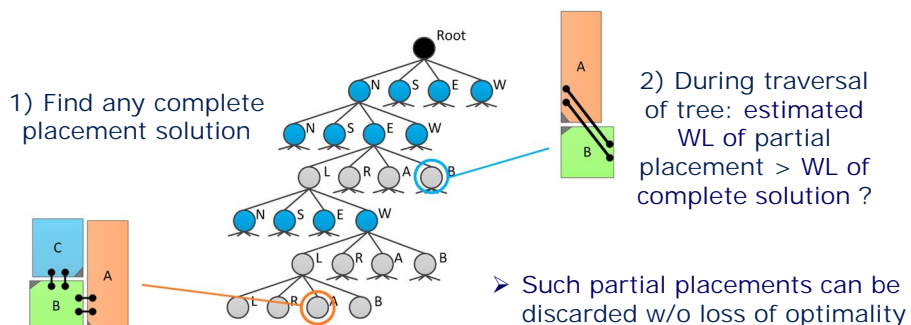
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Placement Framework: Branch and Bound Approach

Discard partial placements if they cannot lead to optimal solutions



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Placement Framework: Branch and Bound Approach



Brute Force
~4,4 · 10¹² nodes: ~43 days

Native Branch-and-Bound
263 million nodes: ~10 min

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Part 3

Advanced Pruning Techniques

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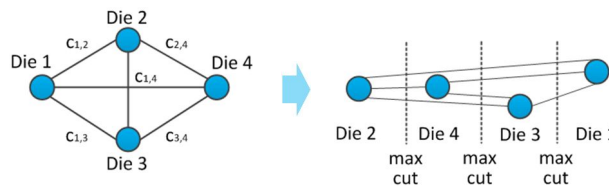
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Advanced Pruning Techniques: Placement Schedule

Dies with large impact on total WL shall be considered early
(Previous works: schedule based only on die size)

Proposed:

- Combined metric: size & number of interconnects
- Greedy graph-based algorithm



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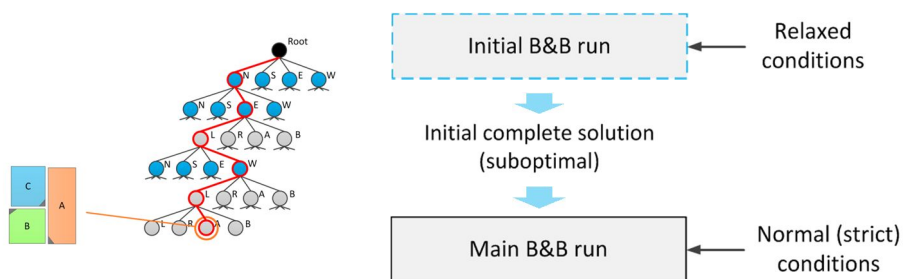
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Advanced Pruning Techniques: Initial Complete Solution

An initial solution (of good quality) helps with search efficiency



➤ Speed-ups of up to x50

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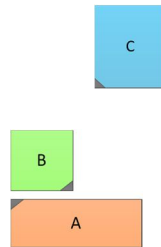
Advanced Pruning Techniques: Forward Wirelength Checking

Before data allocation in tree, look ahead whether new node can become unpromising

Consider new die C

Estimated augmentations for rotations:

East? ≥ 40
 West? ≥ 120
 North? ≥ 140
 South? ≥ 80



Estimated augmentations for topologies:

Die C is left of Die A? ≥ 70
 Die C is above Die B? ≥ 200
 ...

- Predict the minimal WL augmentation incurred by new node in any case; ignore unpromising branches

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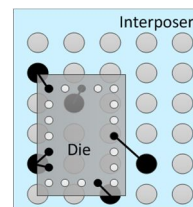
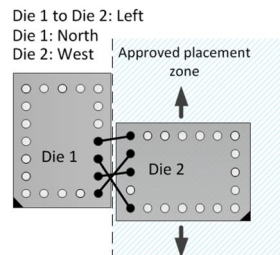
Advanced Pruning Techniques: Forward Wirelength Checking

Topological nodes:

- Place two dies optimally "back-to-back" in all possible variations (rotations included)
- Calculate minimal WL of nets between the two dies

Rotational nodes:

- Align die (sitting alone) optimally to the interposer terminals
- Calculate minimal WL towards the terminals



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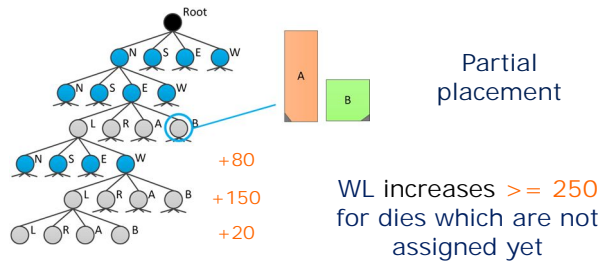
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Advanced Pruning Techniques: Remaining Distances

Estimate how dies yet unassigned will impact wirelength

- We use data from previous techniques (Forward Checking)
- Consider minimal WL augmentations across all remaining levels in the search tree



➤ Better estimation of WL lower bound for partial placements

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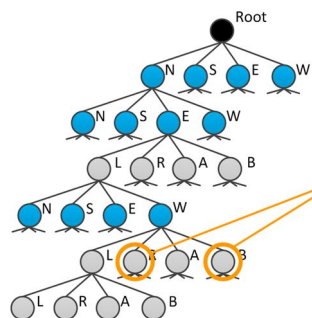
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Advanced Pruning Techniques: Dominated Configurations

Discard placements which appear much worse than others at the same level in the search tree



Is partial placement much worse than other ones?

Criteria: difference between WL estimations in same level >

$$\frac{1}{\text{dies number} + 1} \times \text{best TWL}$$

Example: for 2 dies, difference has to be larger than 33% of the currently best total WL

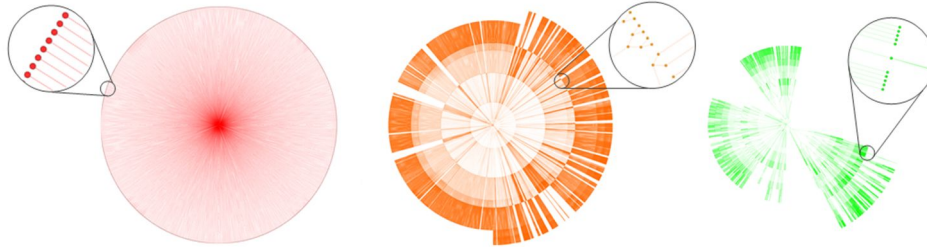
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Advanced Pruning Techniques: Key Result



Brute Force
~4,4 · 10¹² nodes
~43 days

Native Branch & Bound
263 million nodes
~10 min

Advanced B & B
350 thousand nodes
~0.25 sec

- Speedup and scalability
- Up to 11 dies can be placed optimally with reasonable efforts

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Part 4

Results

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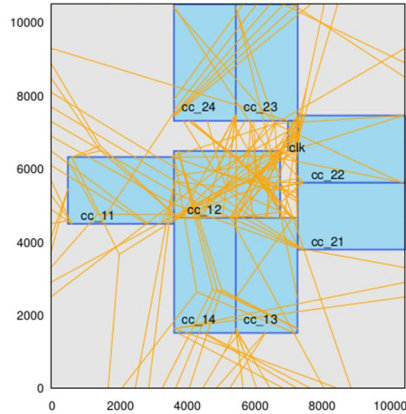
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Results

Layout example for MCNC benchmark apte



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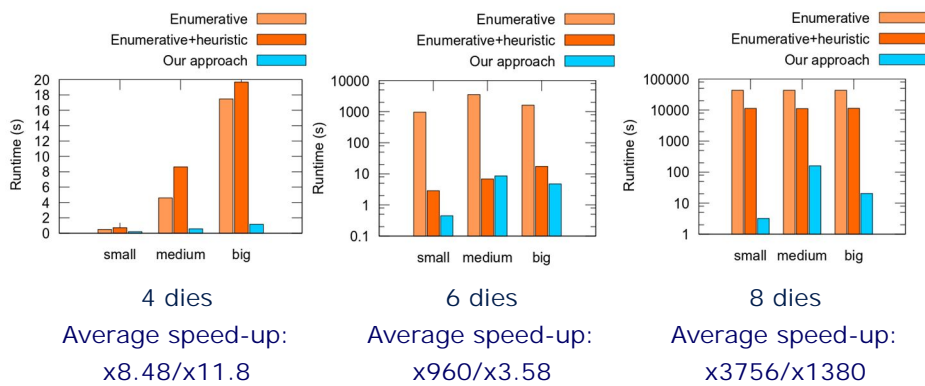
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Results

Comparison for runtime with optimal interposer placement [Liu14] on modified ISPD08 benchmarks



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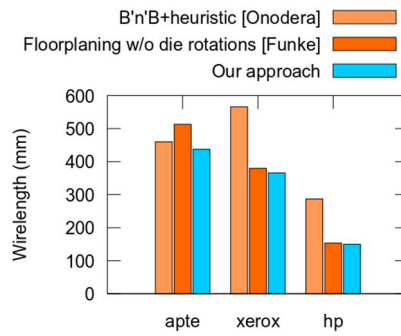
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Results

Comparison for wirelength with (sub-)optimal floorplaning [Onodera93, Funke16]



➤ We report the best WL values for MCNC benchmarks

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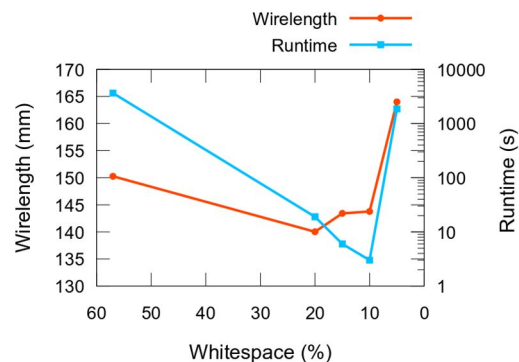
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Results

Trends for practical benchmarks with less whitespace

hp benchmark
as an example



➤ Better wirelength and runtime until some point;
then placement becomes very constrained and challenging

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Summary

- Branch-and-bound flow with advanced pruning techniques for optimal die placement on interposer
- We can optimally place up to 11 dies; prior art only 6 dies
- We consider die rotations and optimize dies within whitespace
- Ours is faster than other optimal methods and reports best WL result for classical MCNC benchmarks
- Binary of tool is publicly available, supports parallel execution:
<http://www.ifte.de/english/research/interposer-design>

Thank you!

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