Flip-Chip Routing with IO Planning Considering Practical Pad Assignment Constraints

Tao-Chun Yu and Shao-Yun Fang

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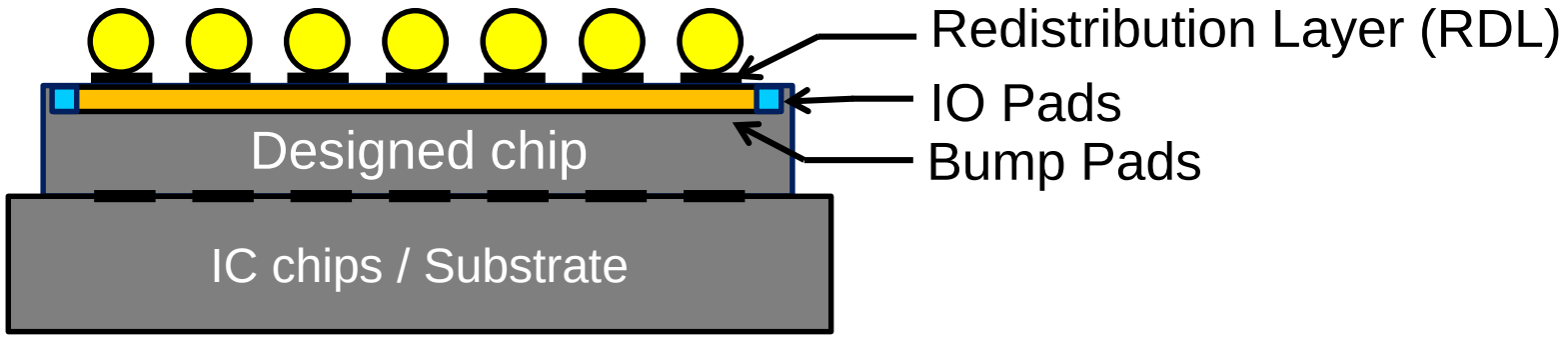
The Electronic Design Automation Laboratory
Department of Electrical Engineering
National Taiwan University of Science and Technology
Taipei 106, Taiwan

臺灣科大

Introduction

Introduction (1/2)

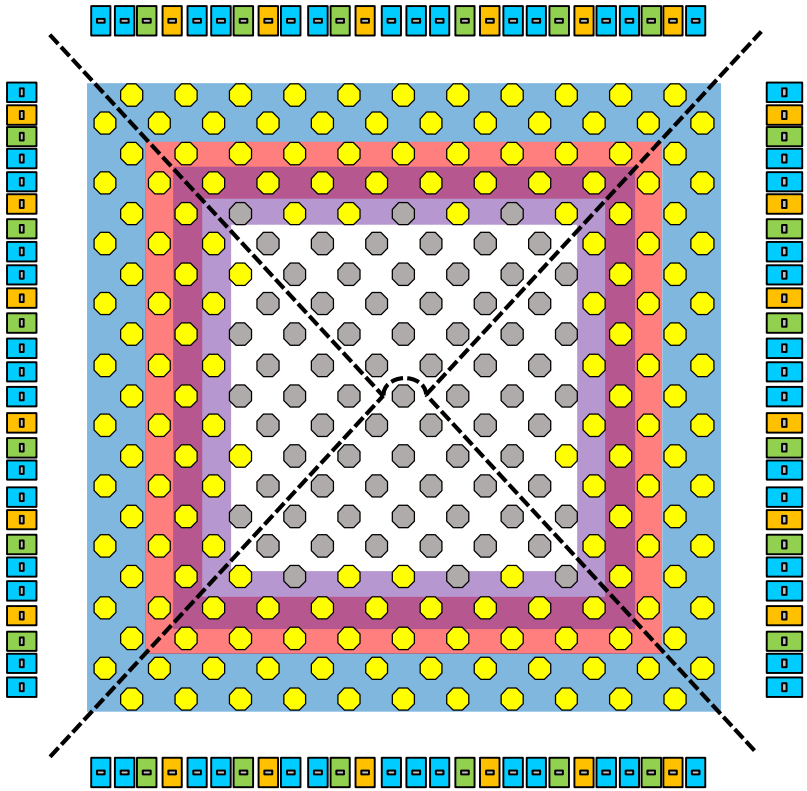
- Flip-Chip packaging technologies



  - Re-distribution layer (RDL)
    - Accomplish the interconnection between bump pads and IO pads (single layer routing problem)
  - Free-assignment
    - The net assignments are free
  - Pre-assignment
    - The net assignments are predefined by designers

Introduction(2/2)

- Power pads and ground pads have been mixed in the modern flip-chip packaging.



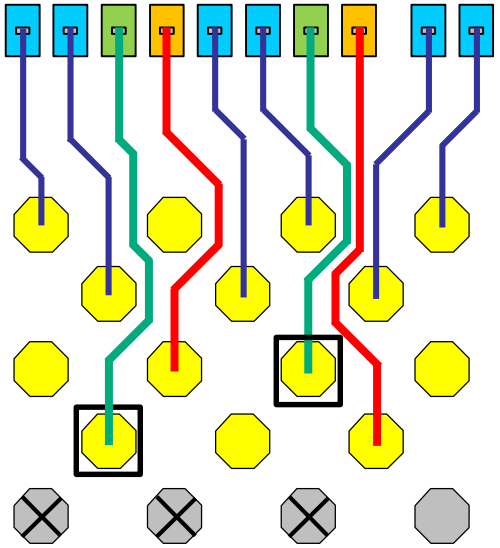
Signal IO
Power IO
Ground IO
Assignable bump
Unassignable bump
For signal
For power
For power and ground
For ground
Partition line

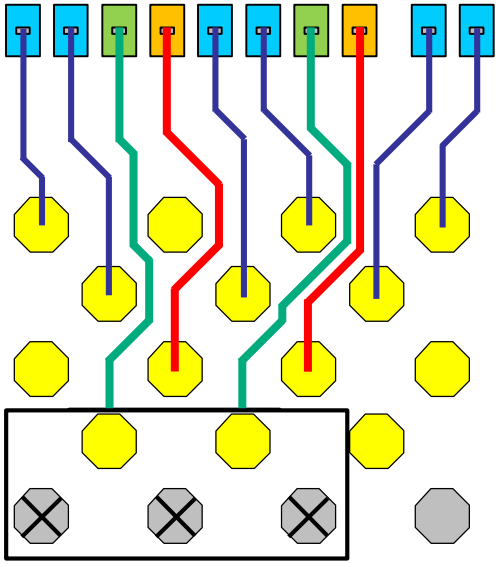
Challenges

Challenges (1/3)

- Facilitation of substrate layout routing design
  - P/G bumps for power pads should not be isolated from the P/G bumps for the P/G mesh
    - P/G pads are routed to the bumps of inner rings

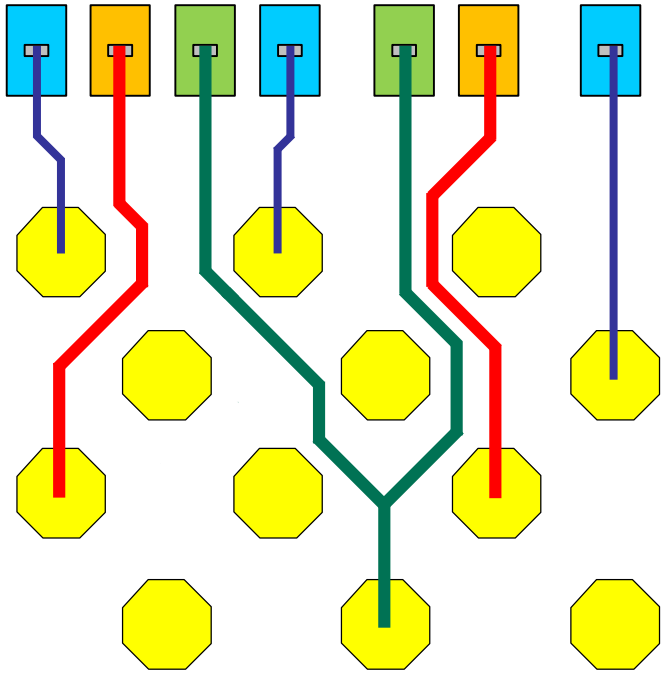
Signal Power Ground Substrate Ground mesh bump





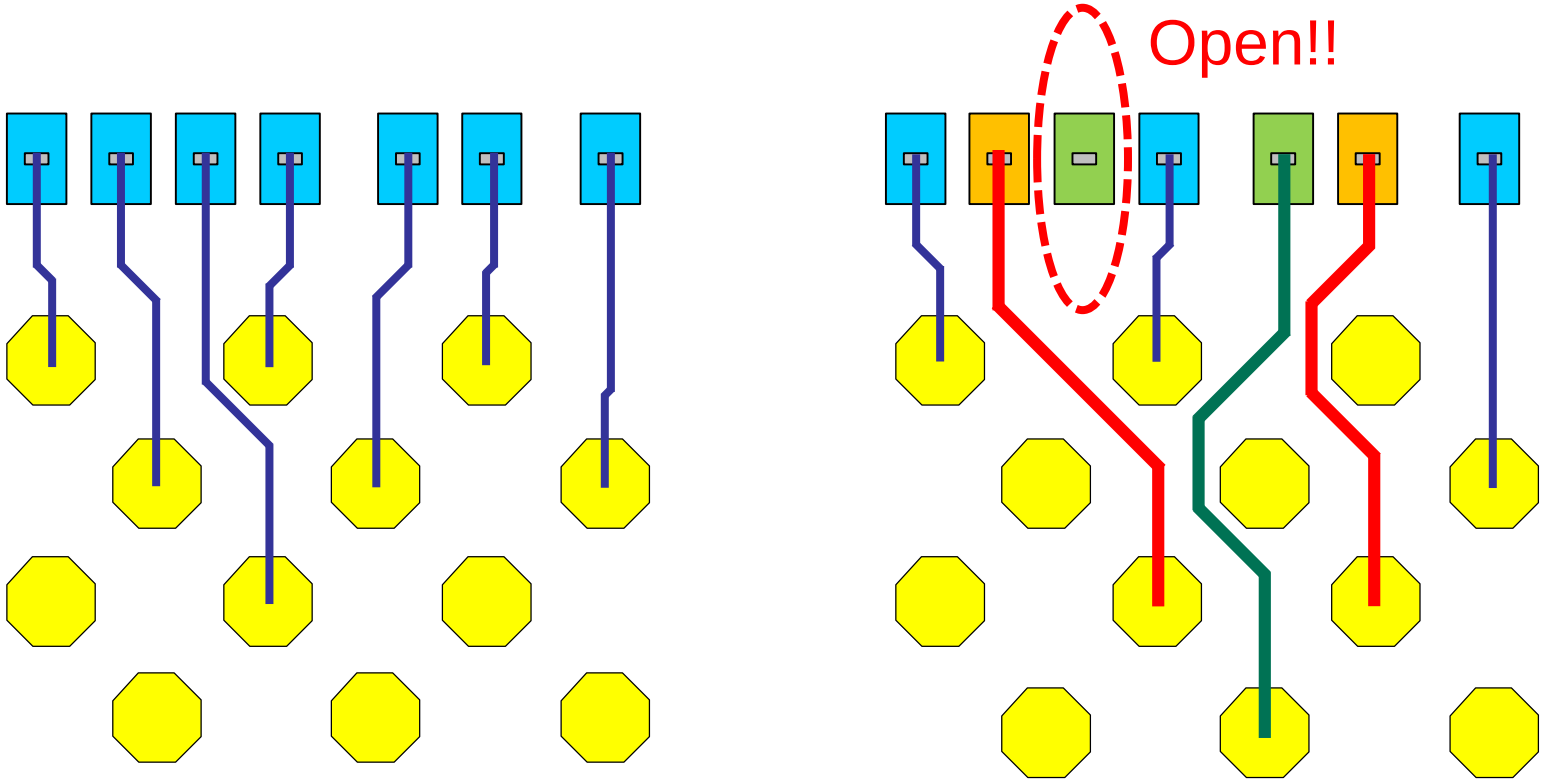
Challenges (2/3)

- Ground nets are connected together in the substrate
  - More than one ground nets may share a single bump to reduce bump utilization and wirelength wire



Challenges (3/3)

- Minimum-cost maximum-flow cannot be applied
  - Cross edges appearance



Contributions

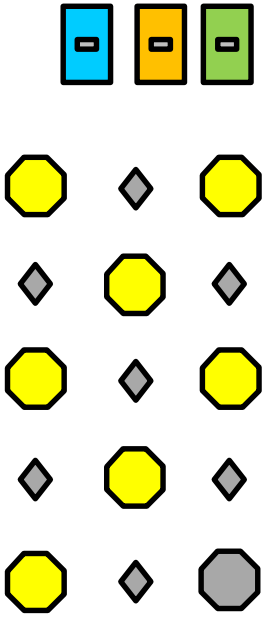
Contributions

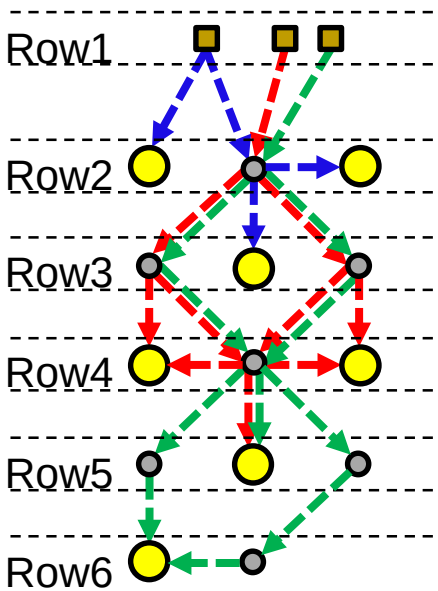
- We propose the first work of free-assignment flip-chip routing considering
  - Mixed IO pads assignment problem
  - Practical IO-bump pad constraints
- We propose a comprehensive algorithm flow
  - Global-routing based IO-bump assignment
  - Linear programming (LP)-based relay point insertion
  - Dynamic programming (DP)-based IO planning algorithm

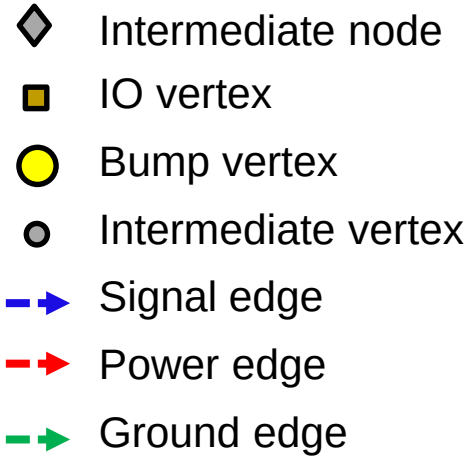
Global Routing-based IO-Bump Assignment

Global Routing-based IO-Bump Assignment (1/3)

- Multi-commodity flow network (MCFN) model is proposed
  - Intermediate nodes are inserted to the middle of any two bumps
  - Distinguish all IO nets as an independent net
  - **Objective:** IO-bump assignment solution with minimum wire length, minimum # used bumps and minimum # used bump rings

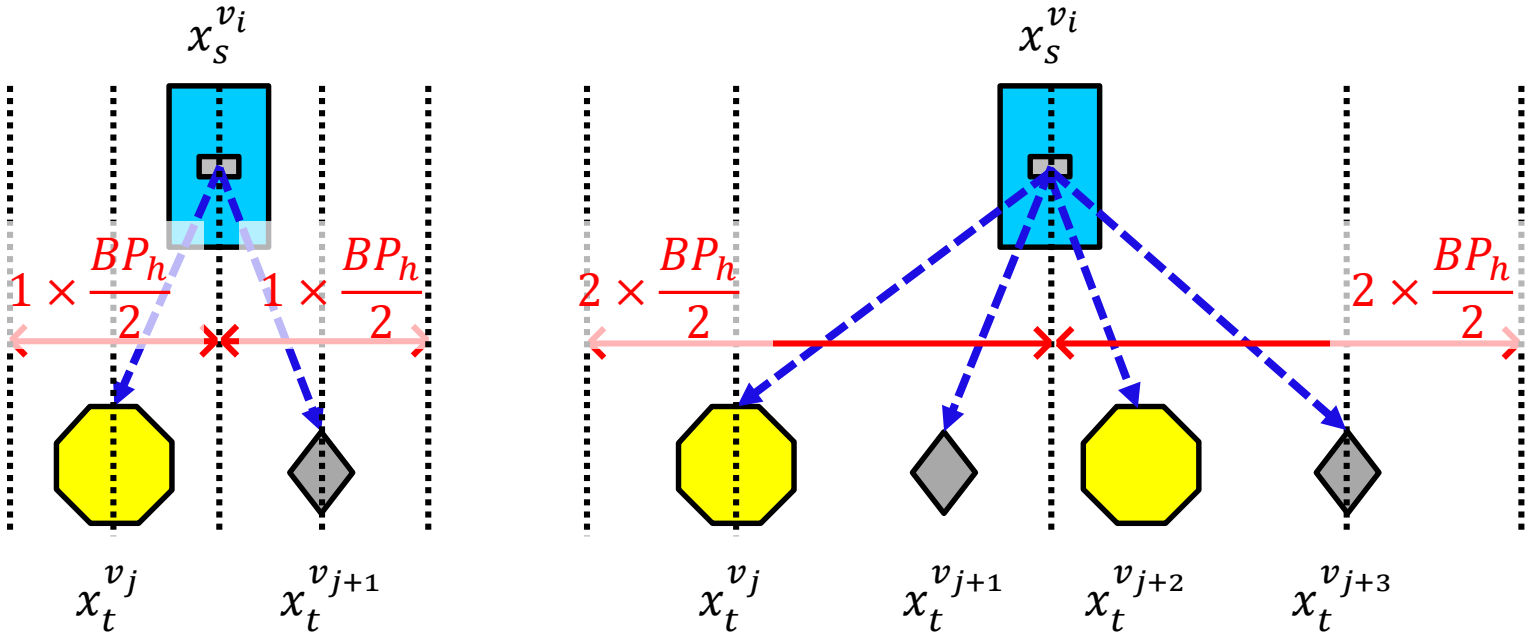






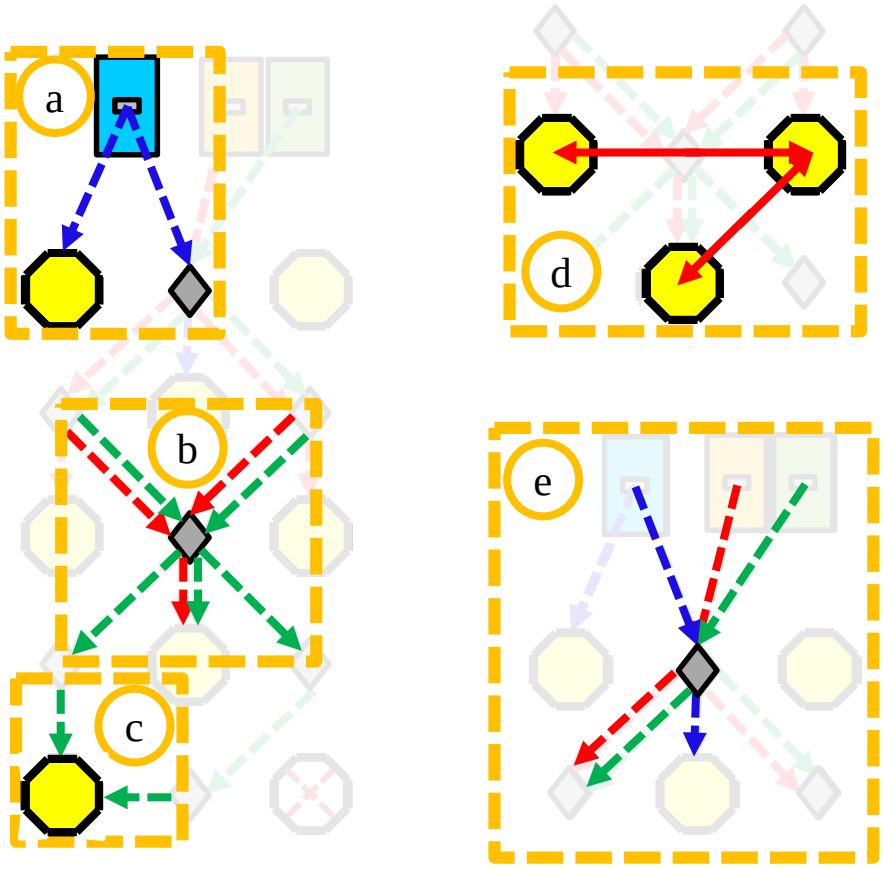
Global Routing-based IO-Bump Assignment (2/3)

- The creation of fanout edges
  - $|x_s - x_t| \leq \alpha \times \frac{BP}{2}$
    - Where BP is the distance between two bumps
    - Where α is a user-defined parameter



Global Routing-based IO-Bump Assignment (3/3)

- 0/1 ILP-based algorithm for MCFN



$$minimize \sum_{p \in P} \sum_{e_{i,j}^p \in E} d_{i,j} \times f_{i,j}^p$$

$subject\ to$

a. Unique flow constraint

$$\sum_{e_{i,j}^p \in E} f_{i,j}^p = 1$$

b. Flow conservation constraint

$$\sum_{e_{i,j}^p \in E} f_{i,j}^p = \sum_{e_{j,k}^p \in E} f_{j,k}^p$$

c. Bump sharing constraint

$$\sum_{p \in P} \sum_{e_{i,j}^p \in E} f_{i,j}^p \leq \beta$$

d. Design rule constraint

$$\sum_{p \in P} f_{i,j}^p \times wp_p + s + w_b \leq BP$$

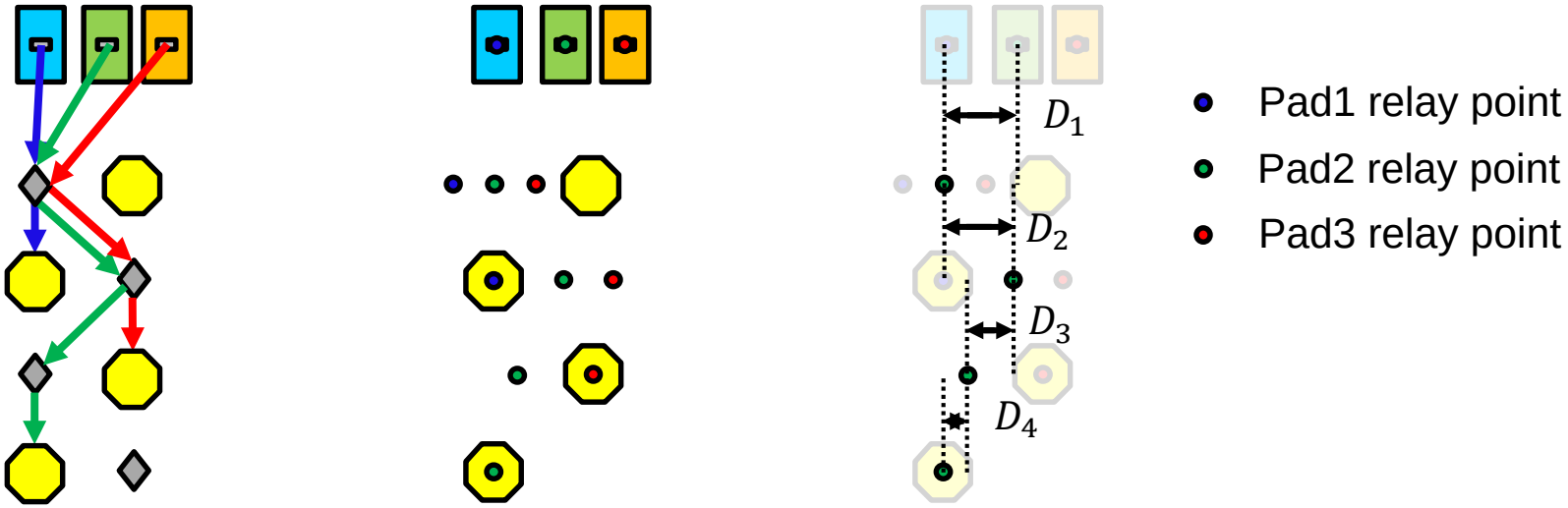
e. Crossing avoidance constraint

$$f_{i,j}^p + f_{i,j'}^p \leq 1$$

Detailed Routing

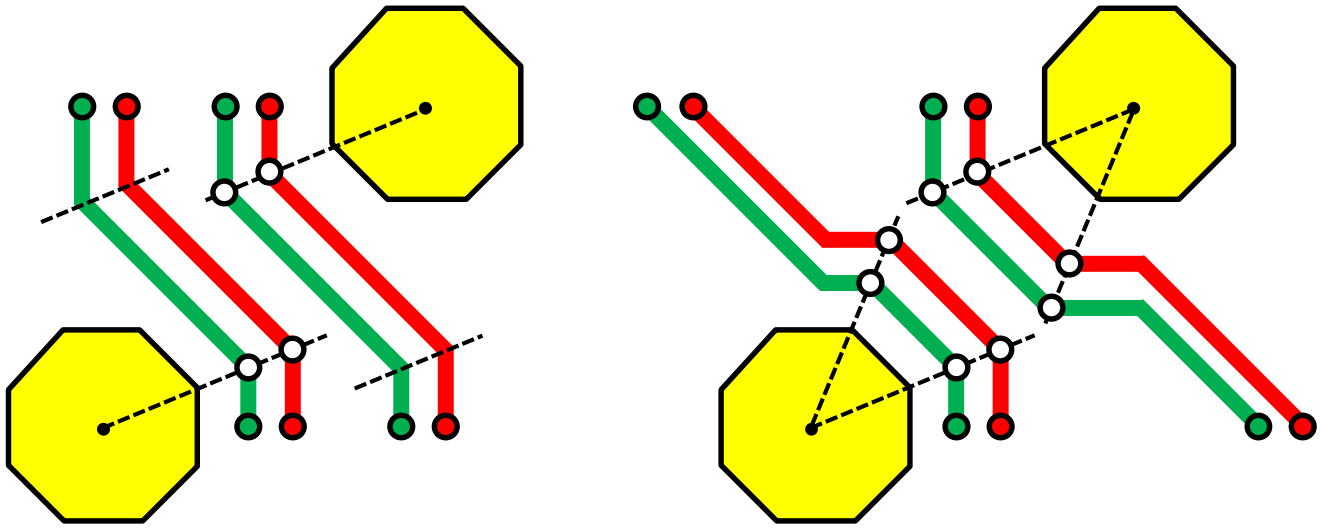
Detailed Routing

- LP-based algorithm is proposed
  - **Objective:** Split all intermediate nodes into successive relay points with minimum x-direction distances
  - **Constraint:**
    - The relay points order must be the same as the IO pins order
    - Minimum spacing rule must be hold



Detailed Routing

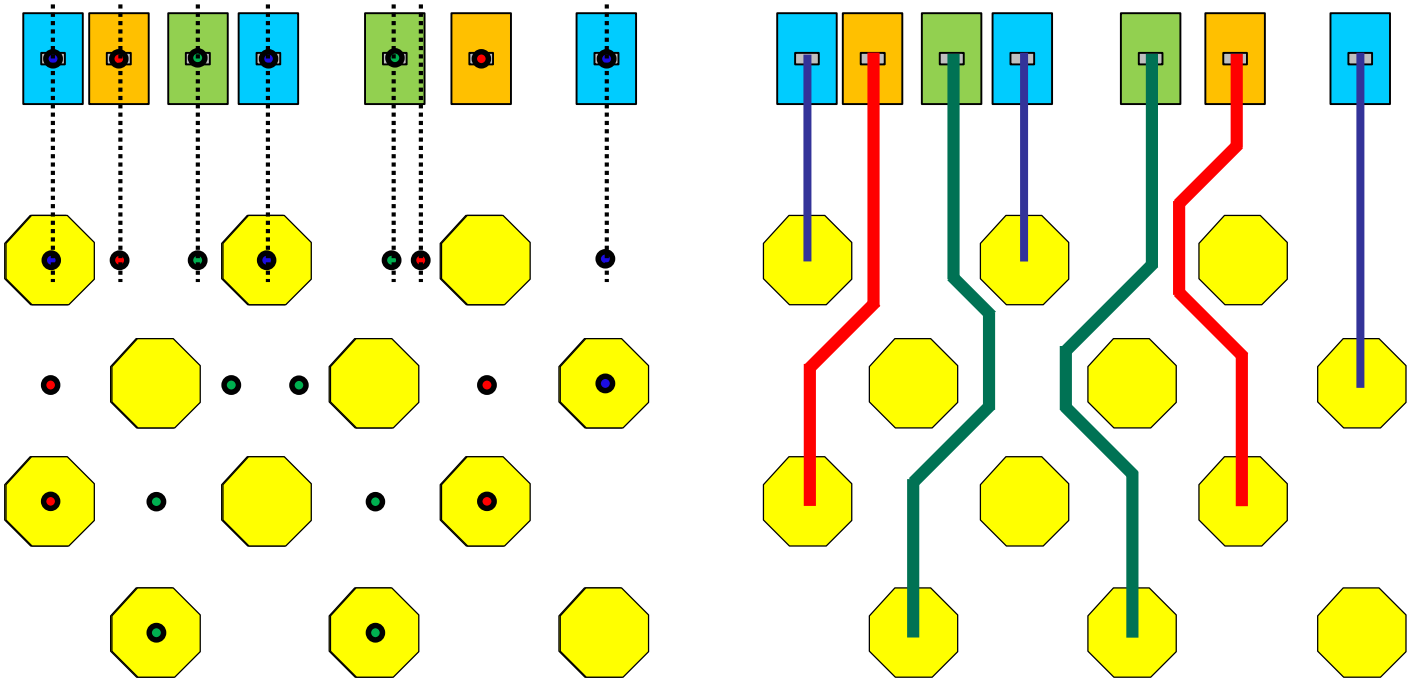
- Critical point insertion technique is proposed to complete all detailed routing path
  - The line with slope $tan22.5°$ and $tan67.5°$ are needed
    - Avoidance of violating minimum spacing rule



Dynamic Programing-based IO planning algorithm

DP-based IO Planning Algorithm (1/4)

- DP-based IO planning algorithm is proposed
  - Minimize the number of wire bends by slightly adjusting the position of IO pads
  - **Objective:** find the maximum number of IO pads that can be aligned with the x-coordinates of their first relay points

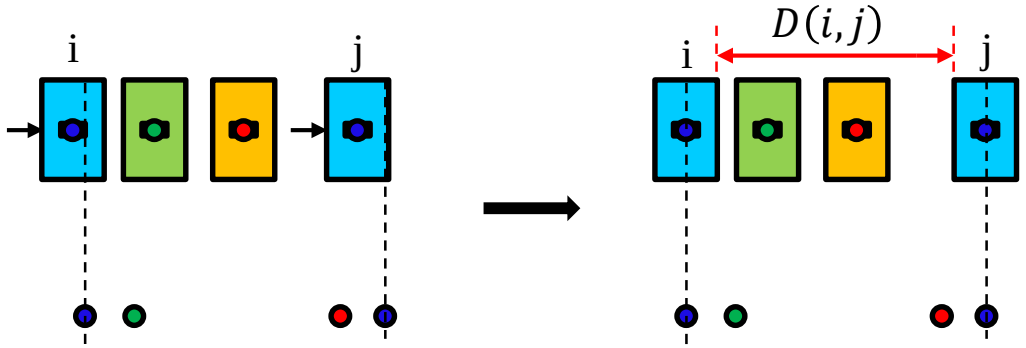


DP-based IO Planning Algorithm (2/4)

- Notations
  - $G(i,j)$: the maximum gain of wire bend reduction between the $i-th$ IO pad and $j-th$ IO pad
    - Under the constraint that the $i-th$ IO pad and $j-th$ IO pad are aligned with their first relay point
  - $f(i,j)$: a 0/1 variable
    - $f(i,j)=1$: a feasible IO planning solution exists
    - $f(i,j)=0$: otherwise

DP-based IO Planning Algorithm (3/4)

- Case 1:

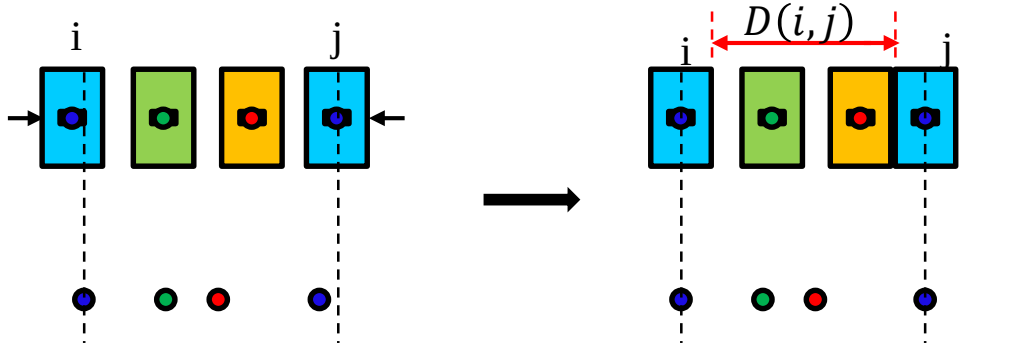


$$D(i,j) \geq w_p \times 2 + s_p \times 3$$

$$f(i,j) = 1$$

$$G(i,j) = +2$$

- Case 2:



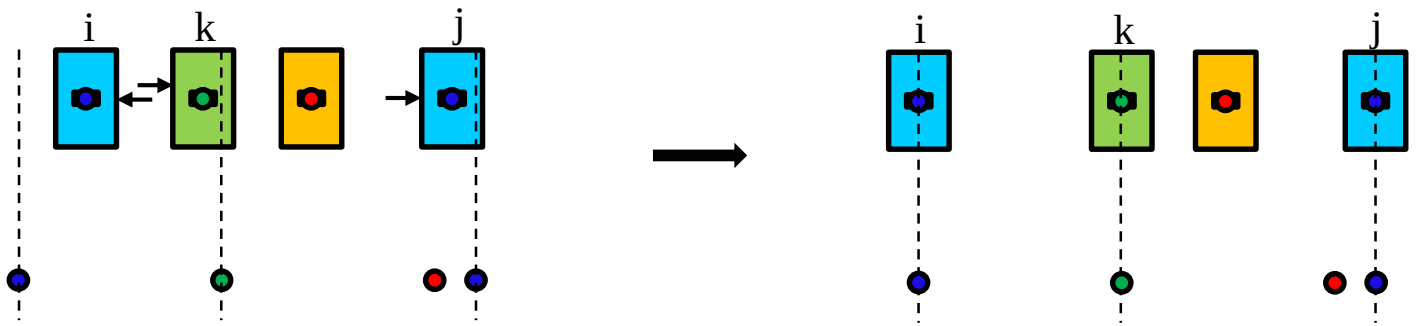
$$D(i,j) < w_p \times 2 + s_p \times 3$$

$$f(i,j) = 0$$

$$G(i,j) = -\infty$$

DP-based IO Planning Algorithm (4/4)

- Case 3:



$G(i,k) = +2$

$G(k,j) = +2$

$G(i,j) = G(i,k) + G(k,j) - 1 = +3$

Experimental results

Experimental Results (1/6)

- Test cases for RDL routing problem
  - Randomly generated by imitating real industrial cases

Case name	#Bumps	#IOs
fc1	84	36
fc2	312	108
fc3	722	177
fc4	1300	249
fc5	1624	284
fc6	2048	319
fc7	2450	354
fc8	2964	389

Experimental Results (2/6)

- The comparison of MCMF and ours

Case name	#Opened nets		CPU time	
	MCMF	Ours	MCMF	Ours
fc1	9	0	0.1	0.22
fc2	23	0	1.34	2.26
fc3	20	0	5.5	7.73
fc4	35	0	13.63	20
fc5	40	0	20.04	27.62
fc6	40	0	28.89	38.83
fc7	43	0	38	51.74
fc8	60	0	49.44	68.88
Average	34	0	19.62	27.16
Comp.	-	-	1.00	1.38

Experimental Results (3/6)

- The routing result with/without the bump sharing

Case name	Total wirelength (μm)		#Used bumps	
	W/O Sh	W/ Sh	W/O Sh	W/ Sh
fc1	16320.8	15877.5	51	46
fc2	49753.7	48751.7	146	135
fc3	77092.4	76150.4	234	219
fc4	113157	106075	336	313
fc5	132147	127706	379	352
fc6	133416	131466	424	395
fc7	153794	151883	472	440
fc8	156063	153299	518	484
Average	103968	101401	320	298
Comp.	1.00	0.97	1.00	0.93

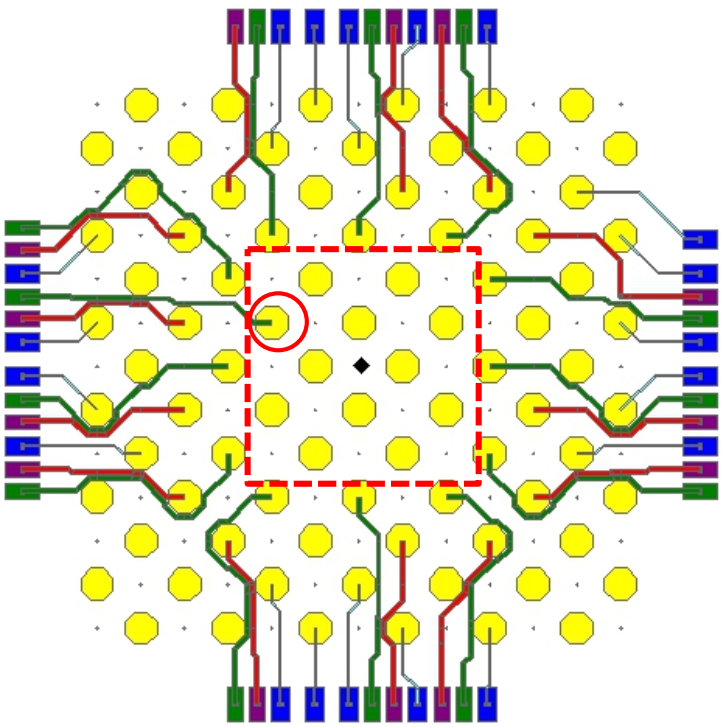
Experimental Results (4/6)

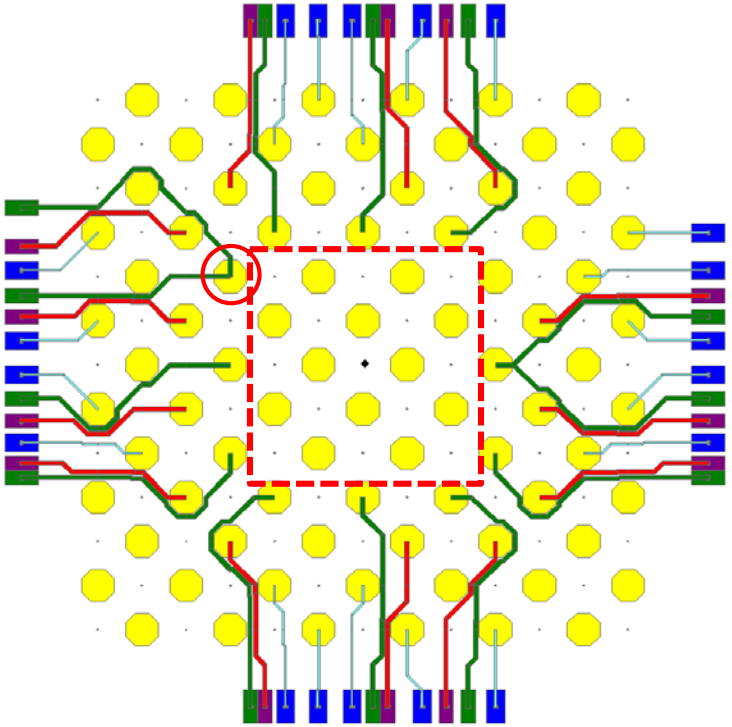
- The results with/without DP-based IO planning algorithm

Case name	Total wirelength (μm)		#Wire bends	
	W/O DP	W/ DP	W/O DP	W/ DP
fc1	15877.5	15304.8	46	22
fc2	48751.7	48044.1	122	78
fc3	76150.4	75253.2	199	134
fc4	106075	104660	297	197
fc5	127706	126309	333	201
fc6	131466	129766	376	244
fc7	151883	149293	394	267
fc8	153299	151151	437	278
Average	101401	99972.6	276	178
Comp.	1.00	0.99	1.00	0.64

Experimental Results (5/6)

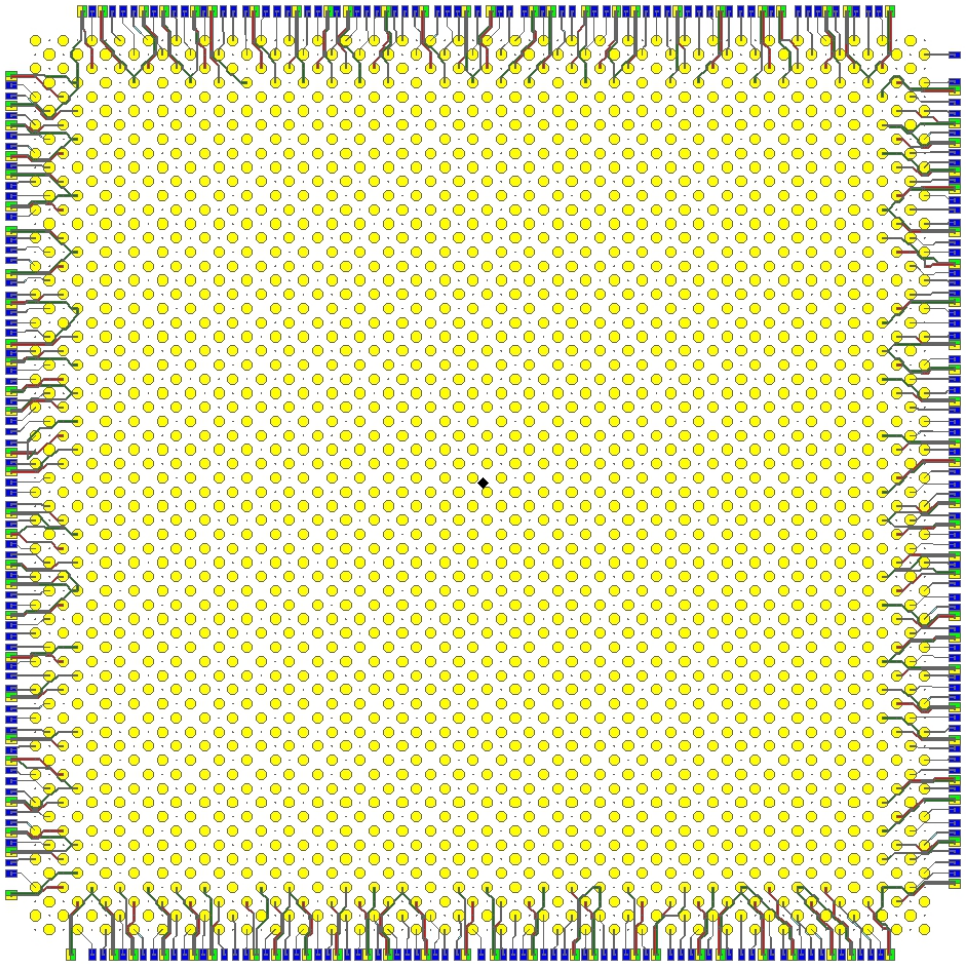
- The routing result of fc1





Experimental Results (6/6)

- The routing result of fc6



Conclusion

Conclusion

- A new flip-chip routing algorithm flow is proposed
  - Stage 1: We apply MCFN model to complete the global-routing based IO bump assignment and solve it by 0/1 ILP-based algorithm
  - Stage 2: The LP-based relay point insertion algorithm is utilized to determine all detailed routing paths, and those detailed routing paths are routed by two predefined topologies
  - Stage 3: DP-based IO planning optimization is used to further minimize the number of wire bends and total wirelength

Thanks for listening