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Exploration of Approximate Multipliers Design Space using Carry Propagation Free Compressors

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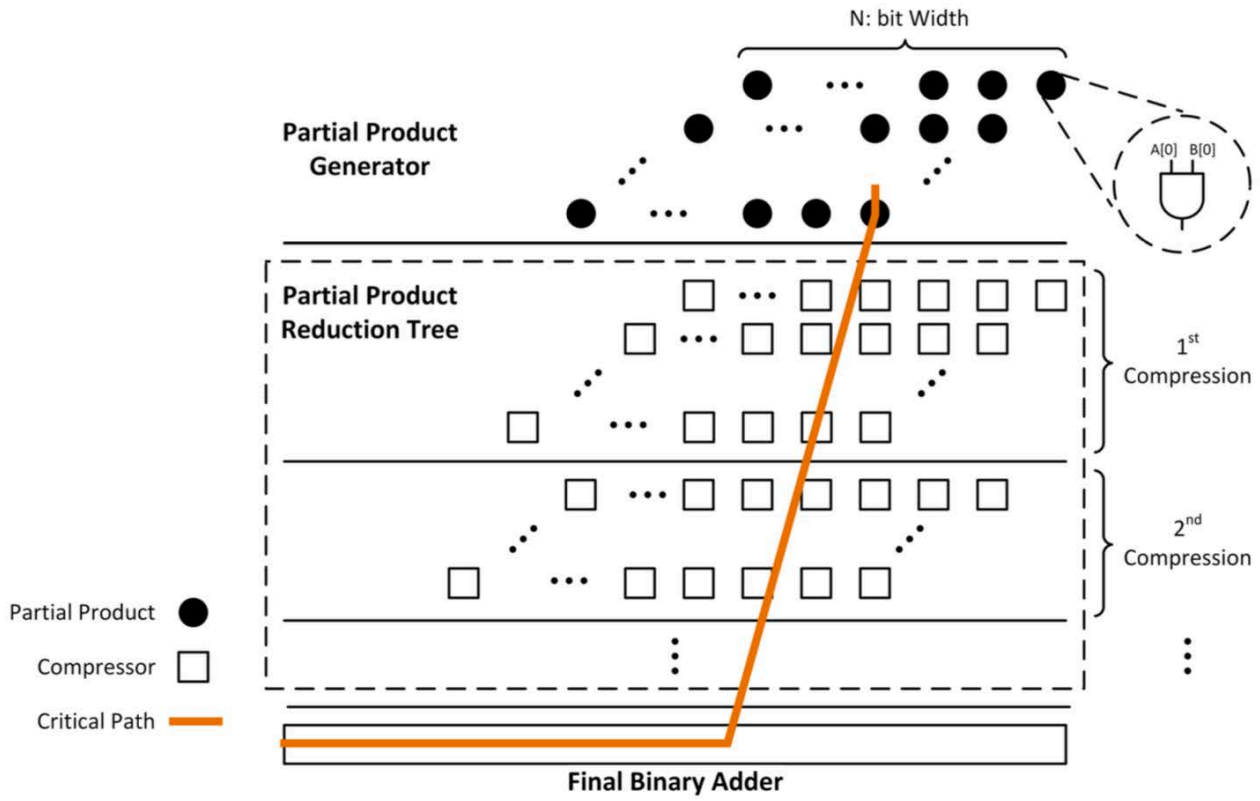
Approximate Arithmetic

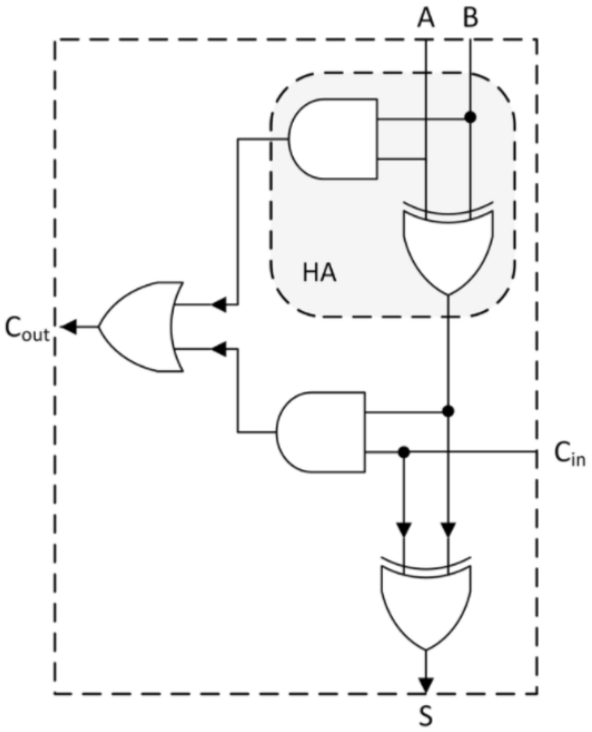
- Motivation
  - Error tolerant applications (e.g., Deep Learning)
  - Arithmetic accuracy as a parameter for HW design space exploration

- Contributions of this paper
  - Approximate Compressors (AXCs) for hardware multiplier design
  - Approximate multiplier design space exploration tool

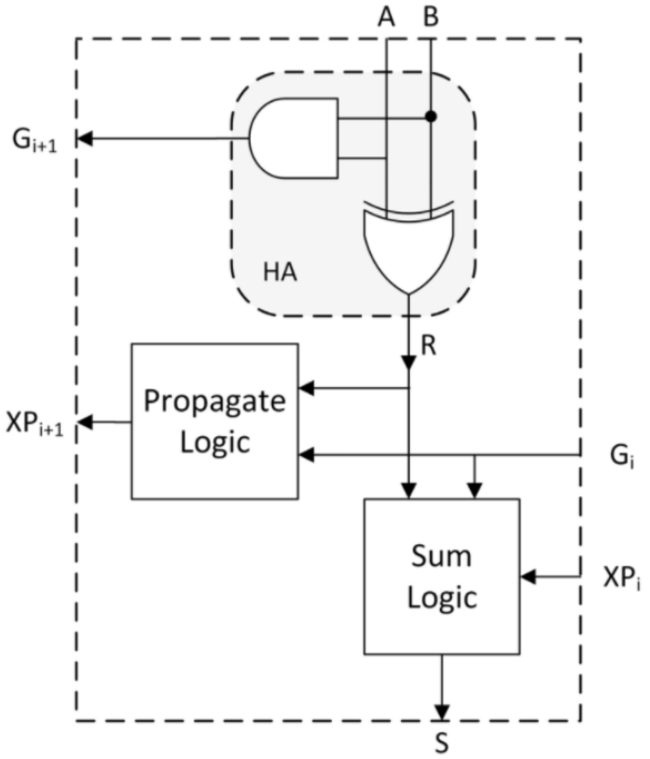
Fixed-Point Array Multiplier



Exact and Approximate Full Adders



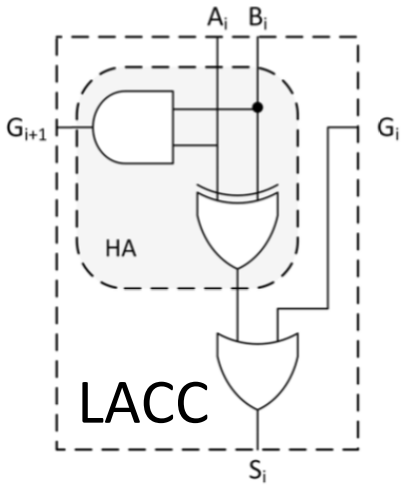
Exact Full Adder



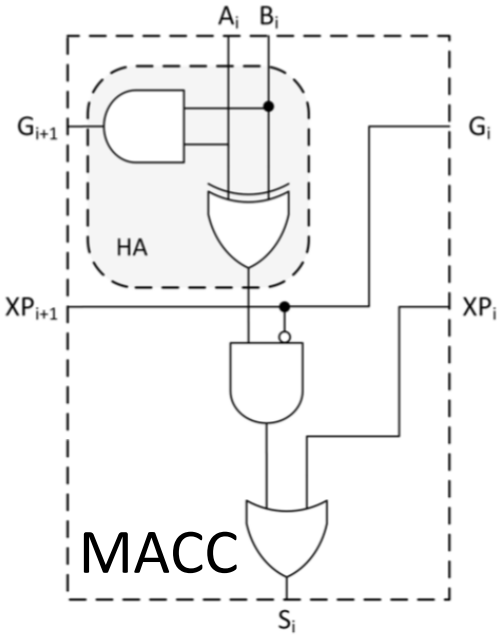
Generic Structure of AXCs

Approximate Compressors

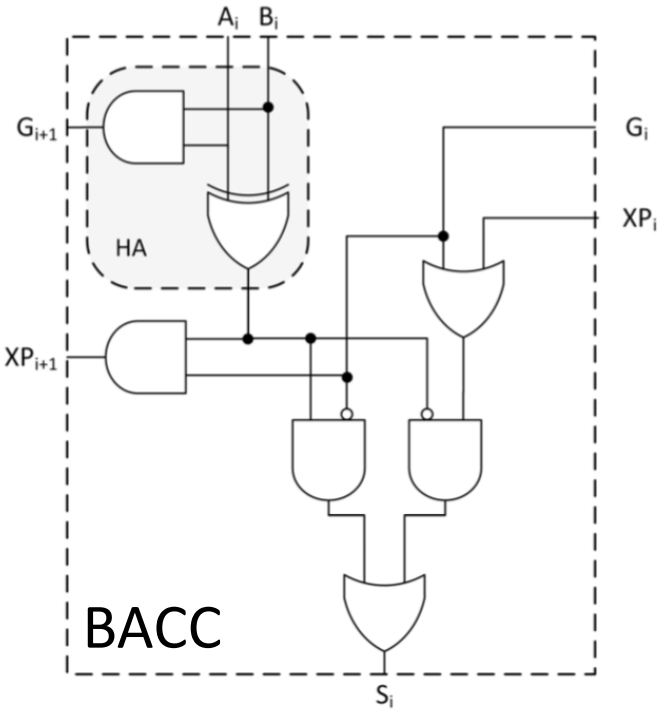
Little Approximate Compressor Cell



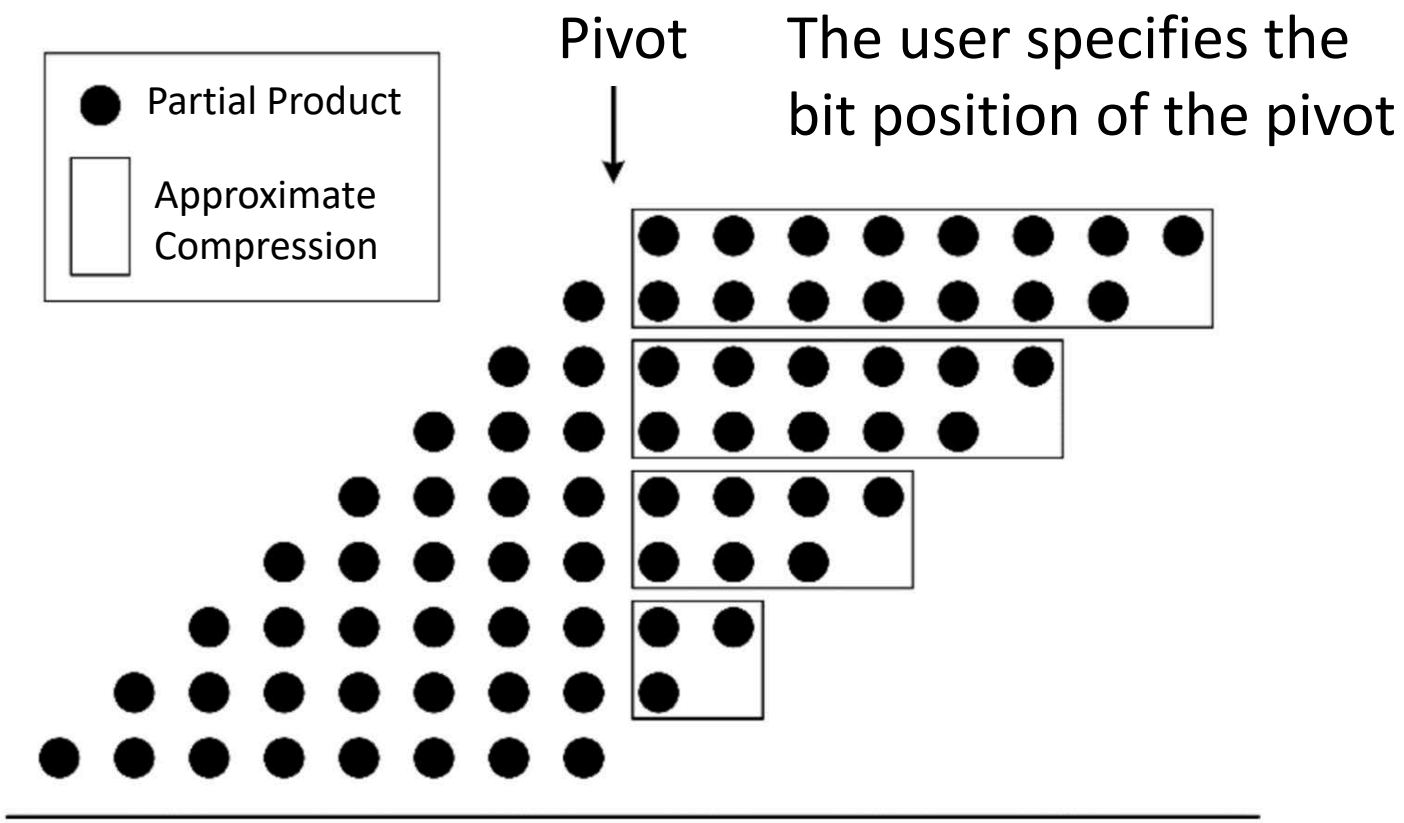
Medium Approximate Compressor Cell



Big Approximate Compressor Cell



Partial Product Tree Reduction using Approximate Compressors (AXCs)

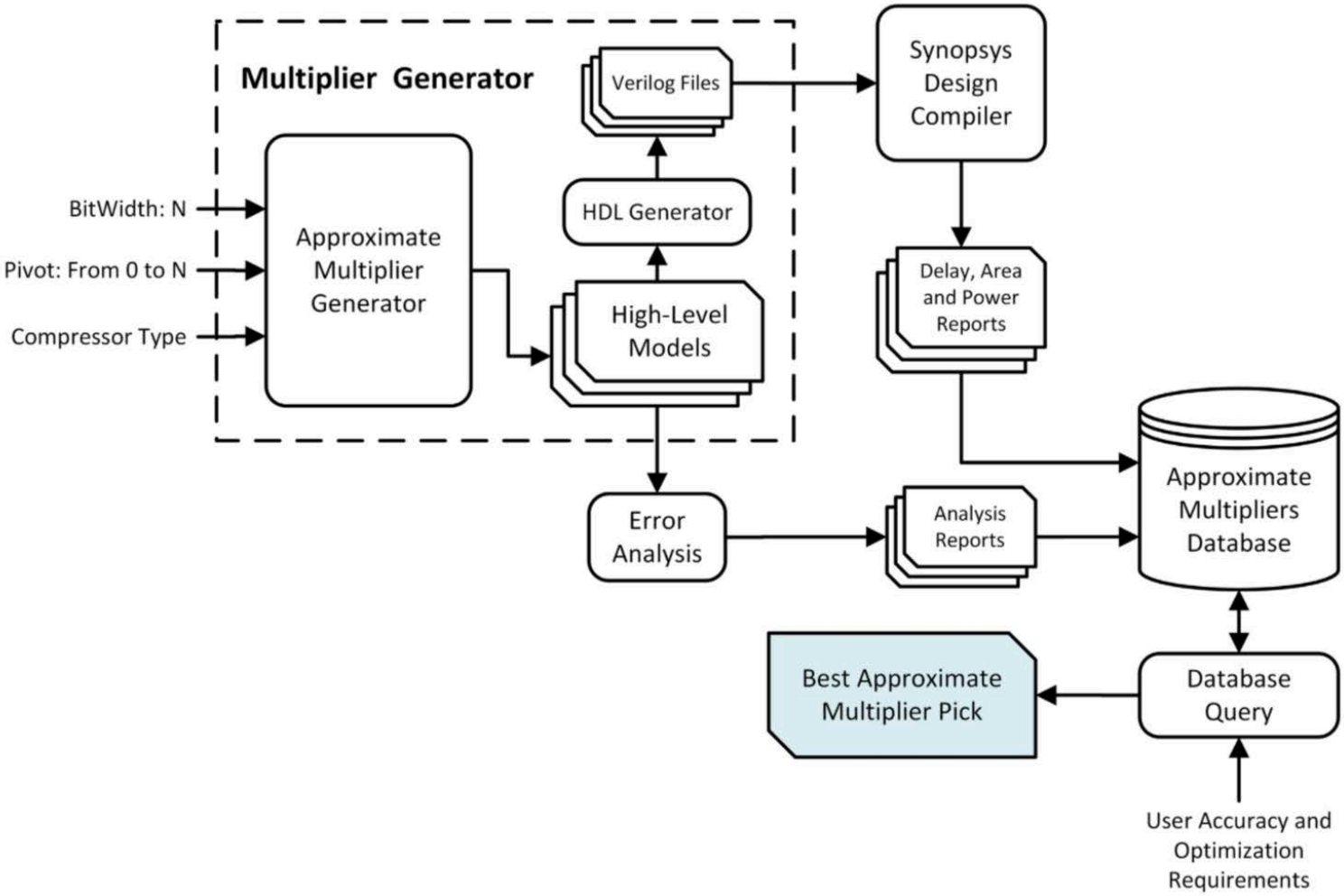


Approx. Partial Product Compression

- Non-iterative Approach
  - AXCs at first level; exact compression at subsequent levels

- Iterative Approach
  - OR-compressors at first level, AXCs at subsequent levels, or
  - AXCs at all levels

Approximate Multiplier Generation



Error Metrics

- $ED(x,y) = \left|P_{exact}(x,y) - P_{approx}(x,y)\right|$
- $RED(x,y) = \frac{ED(x,y)}{P_{exact}(x,y)}$
- $MRED = \frac{\sum_{x=0}^{2^{N-1}} \sum_{y=0}^{2^{N-1}} RED(x,y)}{2^{2N}}$

  Average of RED values across all possible input combinations

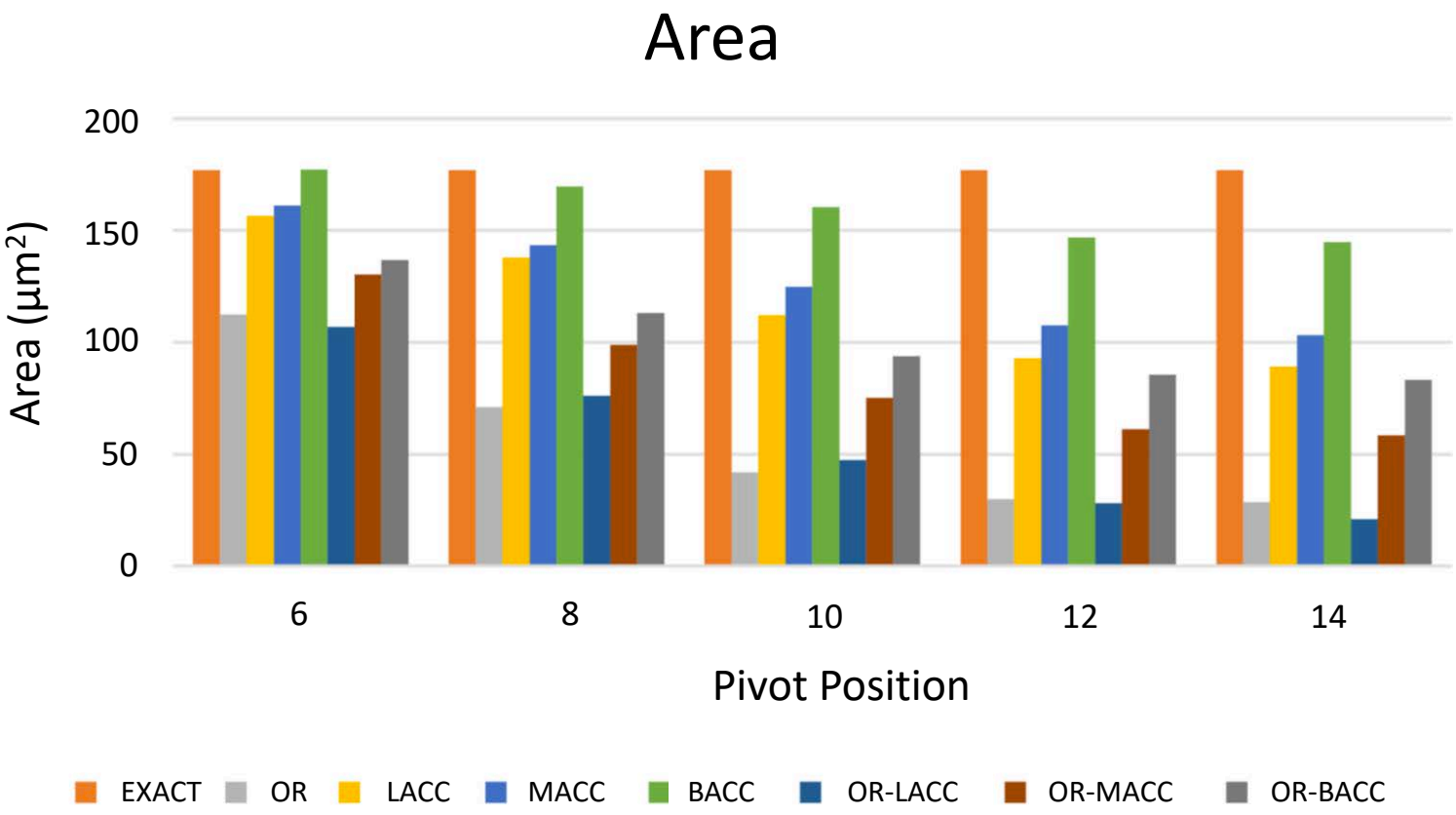
Comparison to Prior Work

8x8-bit Multiplier, No Pivot, Non-iterative Compression

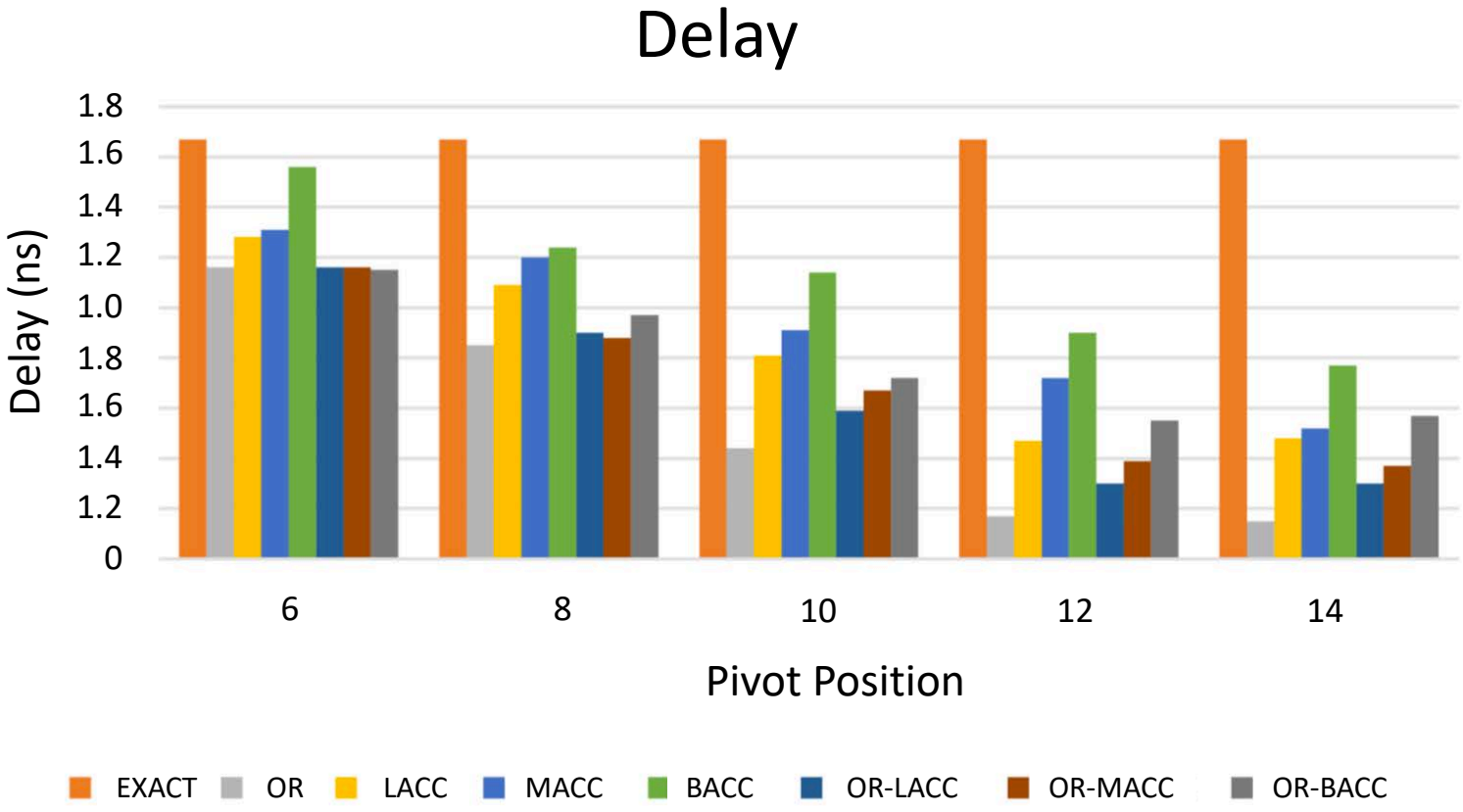
Type	%MRED	%ER	%RED	Delay (ns)	Area (μm^2)
OR [1]	1.98	49.11	33.20	1.19	105
LACC	1.44	38.01	44.44	1.34	126
MACC	0.94	32.65	32.54	1.45	151
BACC	0.46	15.82	26.37	1.41	168

- [1] I. Qiqieh, R. Shafik, G. Tarawneh, D. Sokolov, and A. Yakovlev, “Energy-efficient approximate multiplier design using bit significance-driven logic compression” - DATE 2017

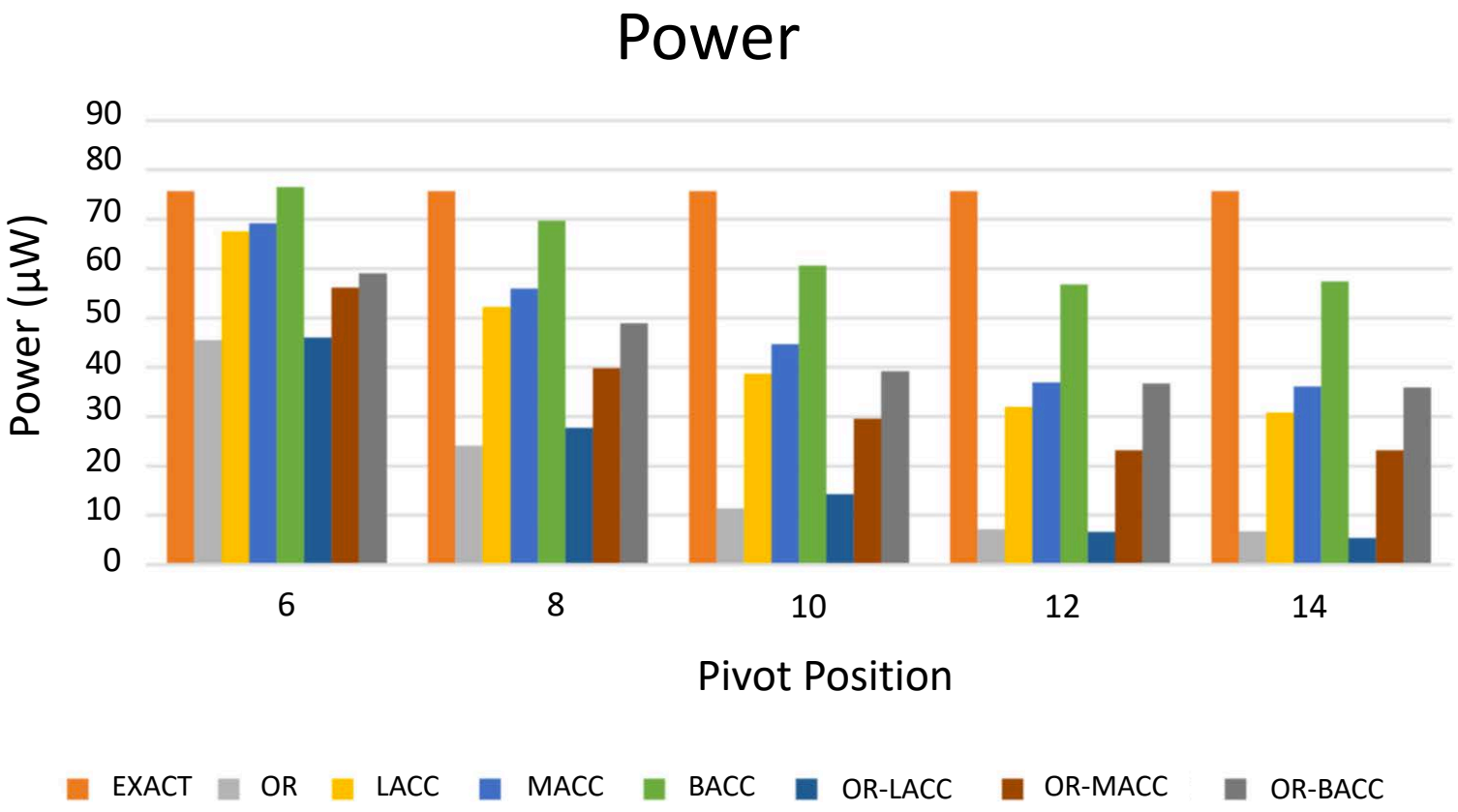
Experimental Results: 8x8-bit



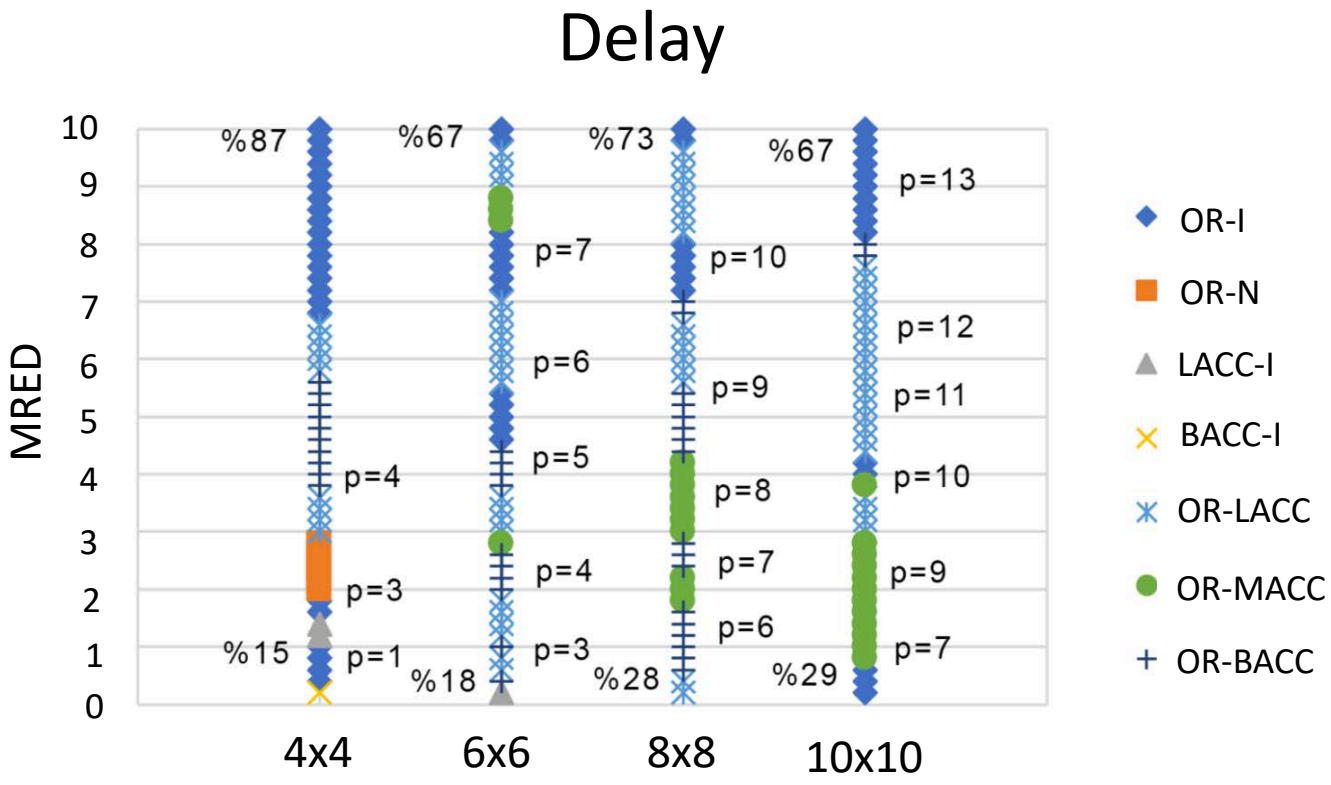
Experimental Results: 8x8-bit



Experimental Results: 8x8-bit



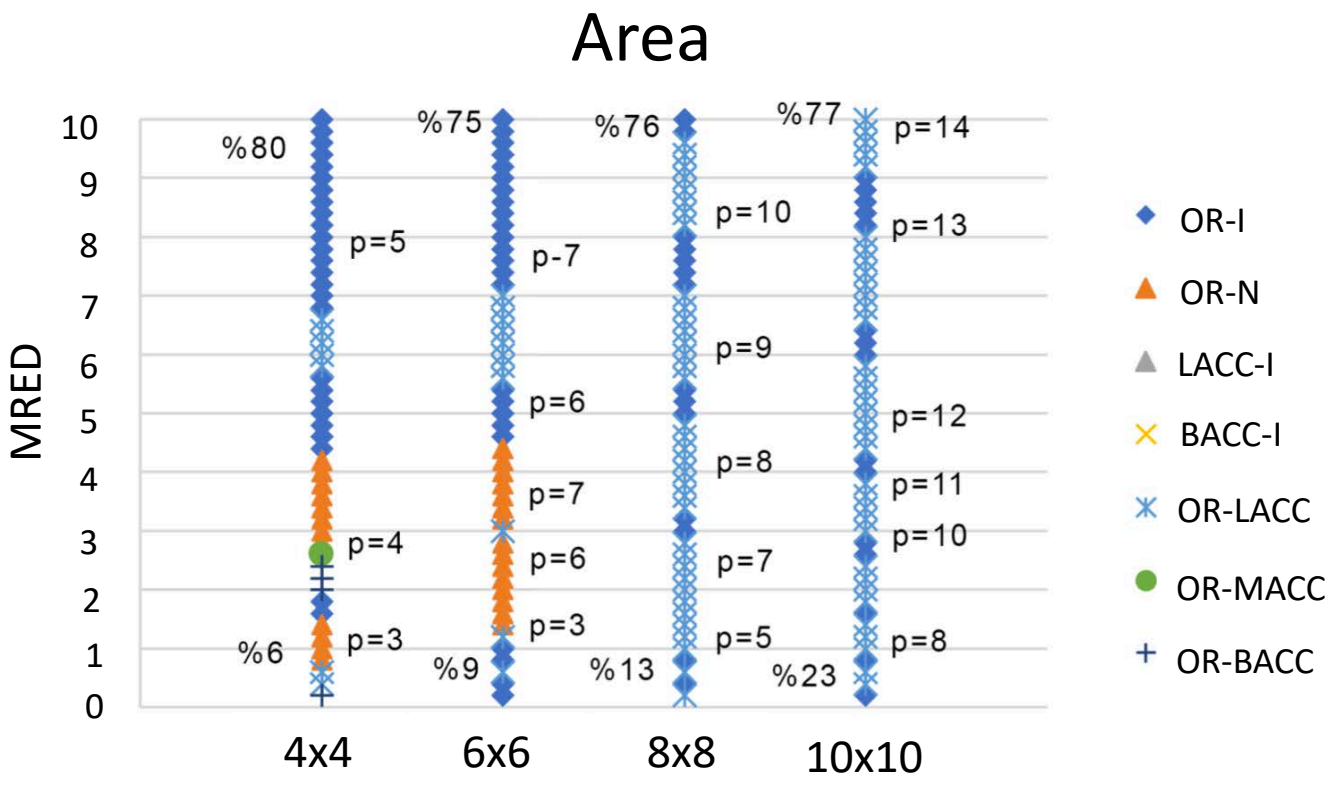
Experimental Results



User specifies bitwidth and MRED

Tool outputs multiplier with lowest delay

Experimental Results



User specifies bitwidth and MRED

Tool outputs multiplier with lowest area

Experimental Results

%MRED	Fastest	Delay Gain	Smallest	Area Gain
0.2	OR-LACC4	28.14%	OR-LACC4	13.74%
0.4	OR-LACC4	28.14%	OR-N6	18.29%
0.6	OR-BACC6	31.14%	OR-LACC5	26.83%
0.8	OR-BACC6	31.14%	OR-N7	29.18%
1.0	OR-BACC6	31.14%	OR-LACC6	39.57%
2.0	OR-MACC7	37.13%	OR-LACC7	50.18%
3.0	OR-LACC8	47.31%	OR-I7	50.75%
4.0	OR-LACC8	47.31%	OR-LACC8	57.08%
5.0	OR-BACC9	51.50%	OR-LACC8	57.08%

OR-LACC4: OR compressor for the first stage and LACC for the next ones with pivot=4.

Comparison to Prior Work

Ref. %MRED	Fastest			Smallest		
	Type	**Area**	**Delay**	**Type**	**Area**	**Delay**
1.98 [1]	OM7	+3.8%	-11%	OL7	-16%	-10%
3.25 [2]	OL8	-29%	-32%	O7	-37%	-28%
0.62 [3]	OB6	-4%	-1.7%	O5	-7%	+6%

OM7: OR-MACC with pivot=7

- [1] Qiqieh, et al.: DATE 2017
- [2] Kulkarni, Gupta, and Ercegovac: VLSI Design 2011
- [3] Liu, Han, and Lombardi: DATE 2014

Conclusion

- Tools, methodology needed to explore approximate arithmetic design space

- User needs to specify
  - Bitwidth
  - Desired MRED (or other error tolerance level)
  - Design objective (delay, area, etc.)

- Our tool explores a larger design space than existing approximate multiplier generators
  - We found specific instances that improve both area and delay compared to prior algorithms

Thank you

Questions?