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Low-power Implementation of Mitchell's Approximate Logarithmic Multiplication for Convolutional Neural Networks

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Computational Challenge in Machine Learning

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Machine Learning growing in diverse applications

Autonomous Driving, Face Recognition, Social Analysis...

Large amount of data and/or time constraint

Computationally costly and challenging!







Convolutional Neural Network (CNN)

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Popular model for Visual and Speech Recognition Large amount of multiply-accumulate(MAC)



Opportunities for Power Savings

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Perfect for hardware acceleration

- A lot of MAC operations
- Parallel and regular structure
- Suitable for Approximate Computing
 - Inherent error in machine learning
 - Applications can tolerate small errors
- Approximate multiplier for the CNN accelerator can reduce power consumption for datacenters and embedded systems





Services that use TPU

[1] Jouppi, Norman P., et al. "In-datacenter performance analysis of a tensor processing unit." Proceedings of the 44th Annual International Symposium on Computer Architecture. ACM, 2017.

Previous Approaches

- Introduction
- Previous Approaches
- Proposed Multiplier
- Experimental Results
- Conclusion

Previous Approaches

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Approximations based on logic bit flips demonstrated significant resource reduction, but not scalable [1,2]



[1] Du, Z., Palem, K., Lingamneni, A., Temam, O., Chen, Y., & Wu, C. (2014). Leveraging the error resilience of machine-learning applications for designing highly energy efficient accelerators. *Proceedings of the Asia and South Pacific Design Automation Conference, ASP-DAC*, 201–206.

[2] Mrazek, V., Sarwar, S. S., Sekanina, L., Vasicek, Z., & Roy, K. (2016). Design of power-efficient approximate multipliers for approximate artificial neural networks. Proceedings of the 35th International Conference on Computer-Aided Design - ICCAD '16

Previous Approaches

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 Approximations based on algorithms are scalable, but had shown inefficiency or CNN performance degradation [1,2]



[1] Lotrič, U., & Bulić, P. (2012). Applicability of approximate multipliers in hardware neural networks. Neurocomputing, 96, 57–65
 [2] Sarwar, S. S., Venkataramani, S., Raghunathan, A., & Roy, K. (2016). Multiplier-less Artificial Neurons Exploiting Error Resiliency for Energy-Efficient Neural Computing. Date 16, 0–5. Retrieved from http://arxiv.org/abs/1602.08557

Proposed Multiplier

Introduction
Previous Approaches **Proposed Multiplier**Experimental Results
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Approximate Log Multiplication

Based on the approximate logarithm

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Reduces logarithm to LOD and Shifter operations



Mitchell, J. N. (1962). Computer Multiplication and Division Using Binary Logarithms. *Electronic Computers, IRE Transactions on, EC-11*(4), 512–517. http://doi.org/10.1109/TEC.1962.5219391

Approximate Log Multiplication

- Multiplication → Addition in Log Domain
- Worst case relative error = 11.1%

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error

Mitchell Log Multiplier

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- Logic optimization of LOD and **ENC**
 - Fast and efficient fully parallel LOD
 - OR-Tree encoder

Shift amount calculation

 \square (n-k-1) = not(k) when n is a power of 2

3 2 1 0
• =
$$m_{i-1,j} + m_{i-1,j+2^{i-1}}$$

• = $h_j = \begin{cases} z_j & j = n-1 \\ \hline m_{\log(n),j+1} \cdot z_j & j < n-1 \end{cases}$

4-bit parallel LOD

n-1



Mitchell Decoder

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Two cases for decoding

- Large Characteristic
- Small Characteristic

Only AND needed for MSBs





Zero Detection Unit

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Critical to CNN accuracy [1]

Output error of neurons in the hidden layer



[1] Mrazek, V., Sarwar, S. S., Sekanina, L., Vasicek, Z., & Roy, K. (2016). Design of power-efficient approximate multipliers for approximate artificial neural networks. *Proceedings of the 35th International Conference on Computer-Aided Design - ICCAD '16*, 1–7.

Power and Area Savings

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Synthesis using Synopsys Design Compiler

- 32nm tech library from Synopsys
- 250 MHz Clock

Up to 76.6% Power Savings at 32 bits

	8-bit			16-bit			32-bit		
	Exact	Our Design	lter. Log	Exact	Our Design	lter. Log	Exact	Our Design	lter. Log
Mean Rel. Error	0 %	3.77 %	0.83%	0 %	3.83 %	0.99%	0 %	3.87 %	N/A
Worst Rel. Error	0 %	11.11%	6.25%	0 %	11.11%	6.25%	0 %	11.11%	6.25%
Cell Area (um ²)	403	312	872	1681	909	2189	6409	2161	7220
Critical Path (ns)	1.07	1.13	1.75	2.23	2.31	3.77	3.78	3.70	4.00
Tot.Power (mW)	0.269	0.197	0.544	1.240	0.549	1.310	6.02	1.41	4.64
Power Savings		26.8%	-102%		55.7%	-5.6 %		76.6%	22.9%

Experimental Results

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Accuracy Evaluation on CNNs

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Caffe

Berkley Vision and Learning Centre

Caffe's floating-point matrix multiplication replaced by Fixed-point C++ Subroutines

Image Dataset	CNN	Layers
MNIST Handwritten Digit Recognition	LeNet	$\begin{array}{l} \text{Convolution} \rightarrow \text{Pooling} \rightarrow \\ \text{Convolution} \rightarrow \text{Pooling} \rightarrow \\ \text{FC} \rightarrow \text{ReLU} \rightarrow \text{FC} \end{array}$
CIFAR-10 Object Recognition	Cuda- convnet	$\begin{array}{l} \text{Convolution} \rightarrow \text{Pooling} \rightarrow \text{ReLU} \rightarrow \text{LRN} \rightarrow \\ \text{Convolution} \rightarrow \text{ReLU} \rightarrow \text{Pooling} \rightarrow \text{LRN} \rightarrow \\ \text{Convolution} \rightarrow \text{ReLU} \rightarrow \text{Pooling} \rightarrow \text{FC} \end{array}$



CNN Top-1 Accuracy Comparison

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MNIST





CNN Top-1 Accuracy Comparison

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Top-1 accuracies with 10 integer bits and 22 fractional bits

Dataset	Reference Floating- point	Our Design	Exact Fixed-point	Iterative Logarithm (2 stage)
MNIST	99.02 %	99.02 %	99.02 %	99.02 %
CIFAR-10	81.43 %	81.43 %	81.89 %	81.71 %

- Our design shows no performance degradation for MNIST and CIFAR-10 datasets
- In CNNs, the error associated with approximate multipliers can sometimes help produce correct predictions
- Correct zero handling is very important for CNNs

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- Optimized Mitchell Log Multiplier for CNN Inference
- Significant power reduction expected at little to no degradation in CNN inference performance
- More scalable than the gate-level approximation
- Better power savings or CNN accuracy compared to the state-of-the-art algorithmic approximations

Thank you!

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Q & A

Backup: Comparison of LOD

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Previous Approach







16-bit Kogge-Stone Adder

$$\begin{split} m_{i,j} &= \begin{cases} z_j, & i = 0 \\ m_{i-1,j}, & i > 0, (n-1-j) < 2^{i-1} \\ m_{i-1,j} + m_{i-1,j+2^{i-1}}, & i > 0, (n-1-j) \ge 2^{i-1} \\ \forall i, 0 \le i \le \log(n), \forall j, 0 \le j < n \end{cases} \\ h_j &= \begin{cases} \frac{z_j, & j = n-1 \\ (m_{\log(n),j+1}) \cdot z_j, & j < n-1 \end{cases} \end{split}$$