Mechanical Strain and Temperature Optimization for Thin-Film Transistor Based Pseudo-CMOS Logic Array

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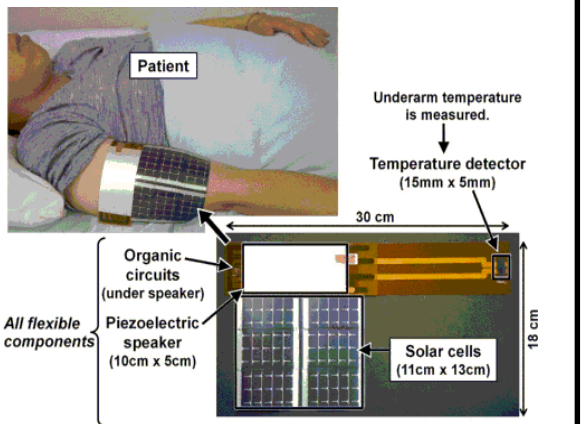
Outline

- **Background and Motivation**
- **TFT based pseudo-CMOS logic array**
  - Array circuit
  - Interconnect architecture
- **Mapping problem formulation of logic array**
- **Mapping algorithms for logic array**
- **Experiments**
- **Conclusion**

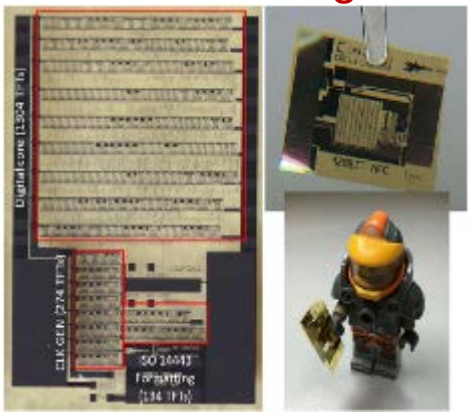
Background: Thin-film Transistor (TFT)

Fever alarm armband



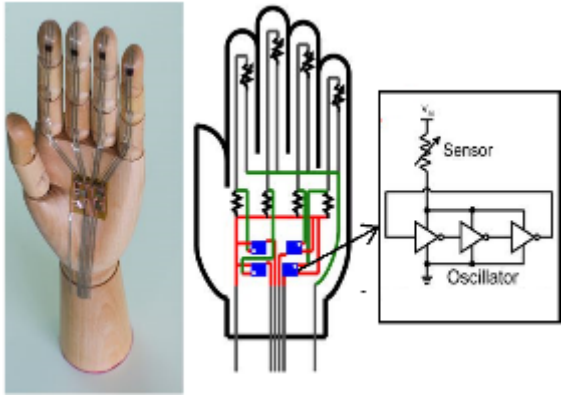
F. Fuketa et al., ISSCC 2015

RFID tag



K. Myny et al., ISSCC 2017

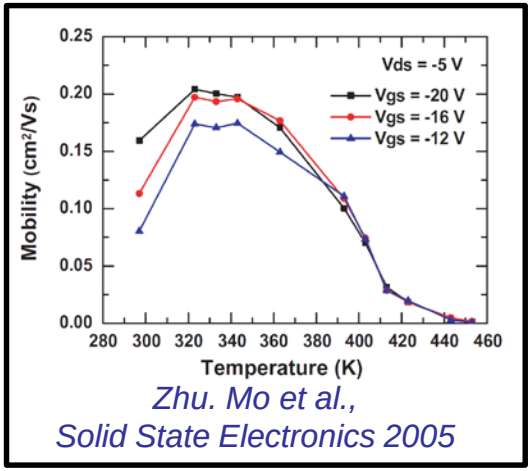
E-skin



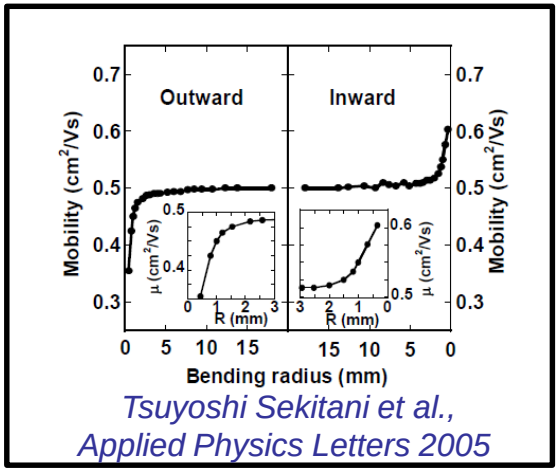
B. Tee et al., Science 2015

TFTs are essential to flexible and sensing applications.

However, TFTs have yield problem and are sensitive to temperature and strain…



Zhu. Mo et al.,
Solid State Electronics 2005



Tsuyoshi Sekitani et al.,
Applied Physics Letters 2005

Temperature for OTFT: >100% change @200K range

Bending for OTFT: ~20% change@15mm radius

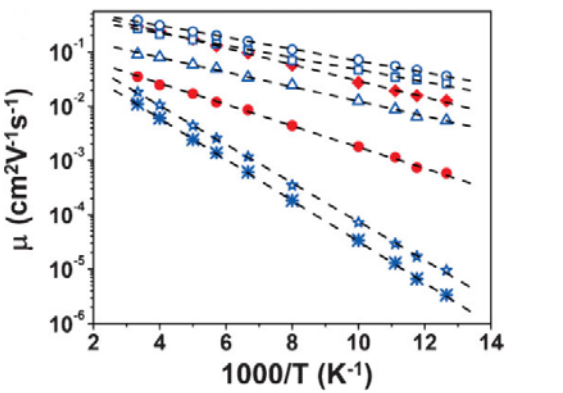
Temp and strain effects on TFTs

Range of change in mobility of TFT technologies [11]

TFT technology	Compressive strain	Tensile strain
a-Si TFT	-26%	7.6%
OTFT	20%	-30%
poly-Si TFT	44%	-44%

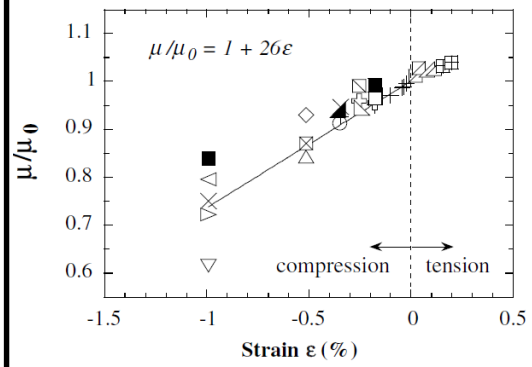
Many works study the TFT mobility under temp & strain

OTFT



Letizia J A et al., Advanced Functional Materials 2010

a-Si TFT



Gleskova, H et al., J. Non-Cryst 2004

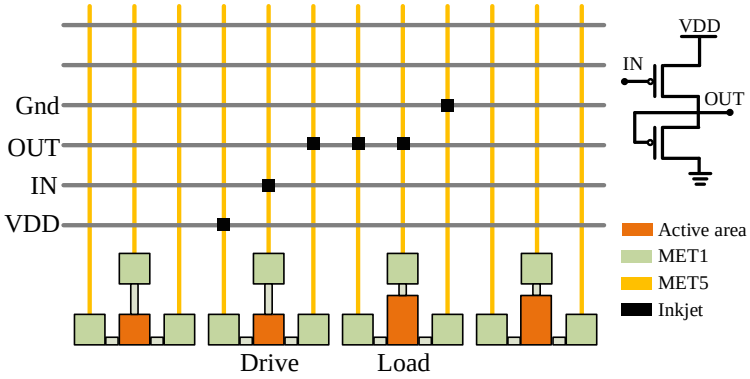
$$\mu_{\text{eff}} = \mu_0 \exp\left(\frac{-E_A}{kT}\right)$$

$$\mu/\mu_0 = 1 + 26\varepsilon$$

μ_0: original mobility
T : temperature
E_A: energy difference between trap state and conduction band edge

Circuit level optimization to release some of these problems?

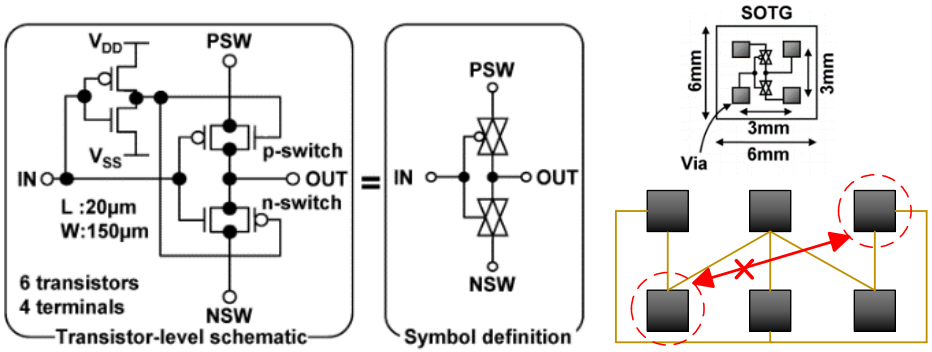
Motivation: TFT logic array challenges



Inkjet-configurable gate array (IGA)

- Transistor level implementation
- Pre-fabricated interconnections
- Large area overhead

J. Carrabina et al., TETC 2016



Sea-Of-Transmission Gates (SOTG)

- Gate level implementation
- Complementary devices
- Routability problem

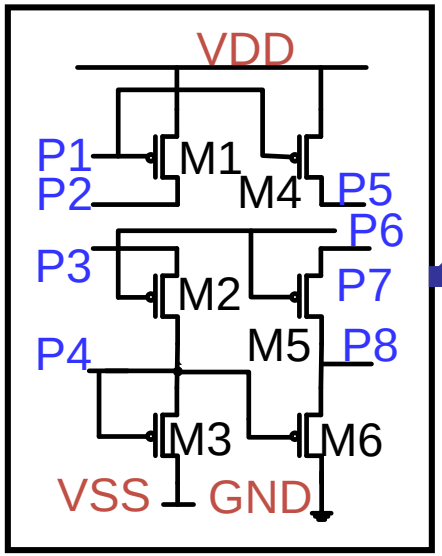
K. Ishida et al, JSSC 2011

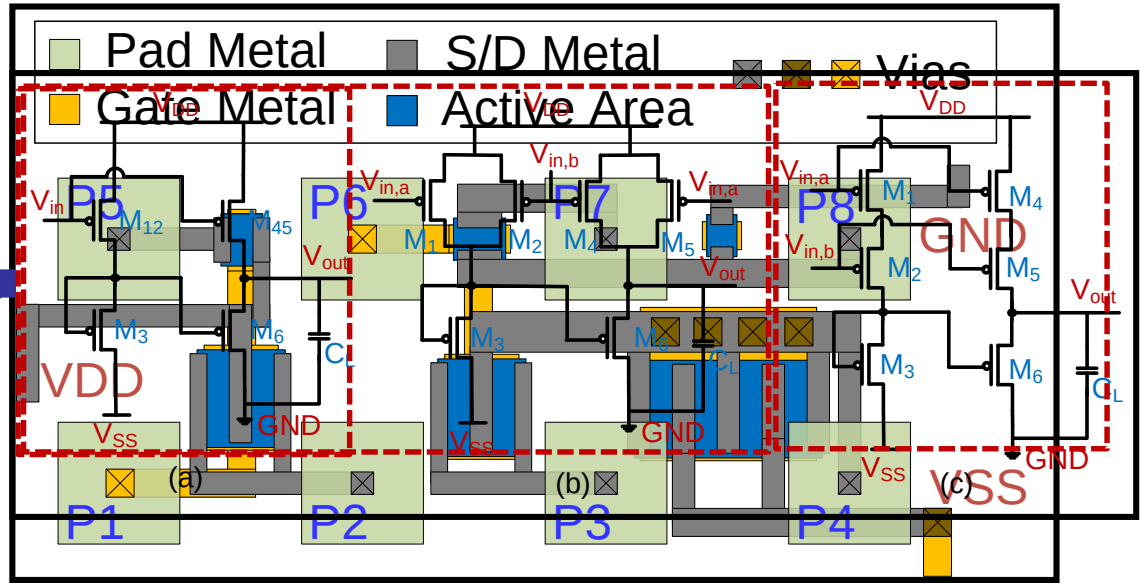
Logic array of TFT

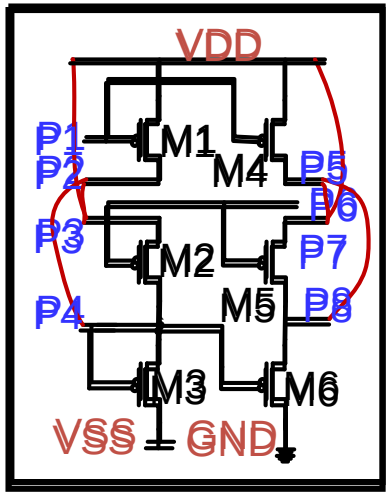
- Low cost: print wire with inkjet printer and metallic inks “at home”
- Customizable: similar to the concept of FPGAs
- Robust: programmability to overcome yield problem

Mapping algorithms for logic array are still missing.

Pseudo-CMOS logic array cell



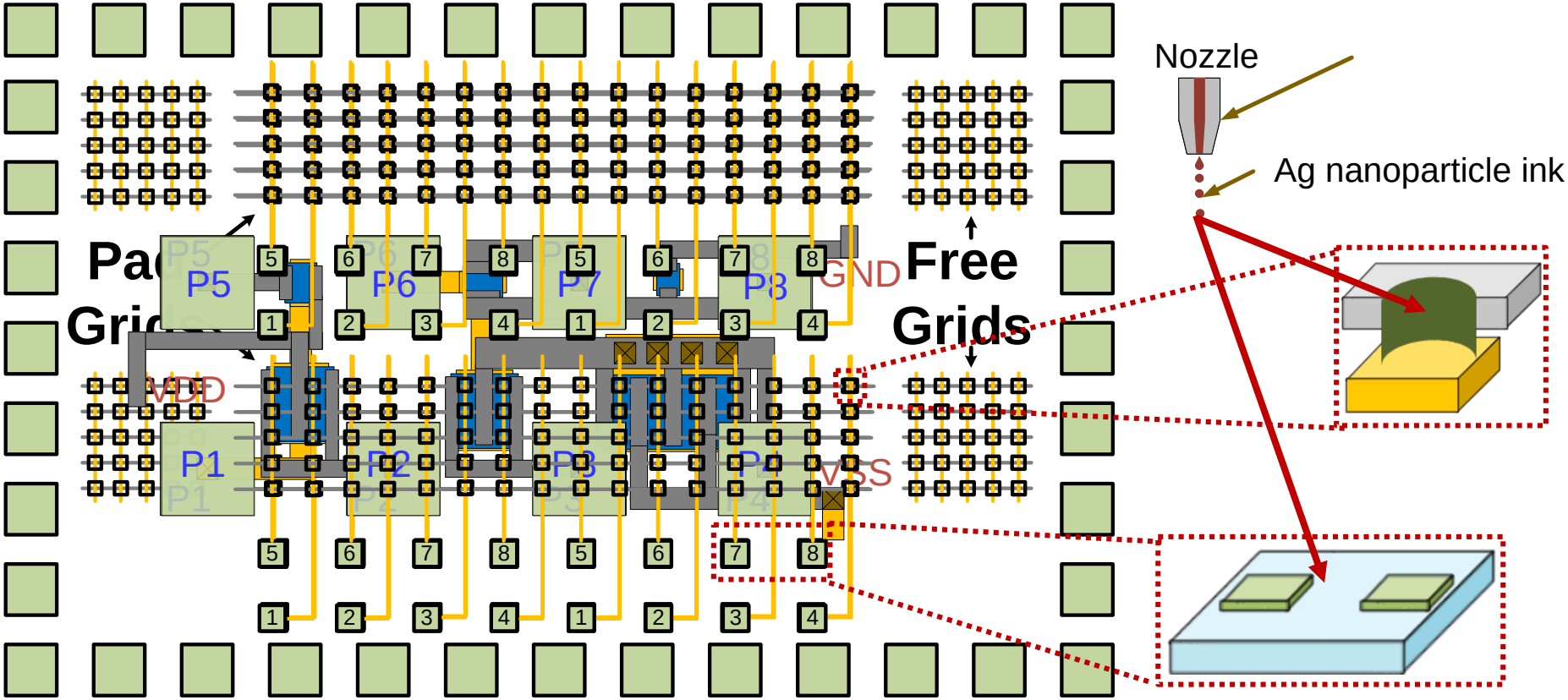




Logic cell	Program method	Unused TFTs
NAND/INV1	P_2-P_4, P_5-P_8, $P_{3/7}$-V_{DD}	-
NOR/INV2	P_2-P_3, P_5-P_7	-
INV3	$P_{3/7}$-V_{DD}	M_1, M_4
INV4	P_2-P_4, P_5-P_8	M_2, M_5

Qinghang Zhao et al., DAC 2016

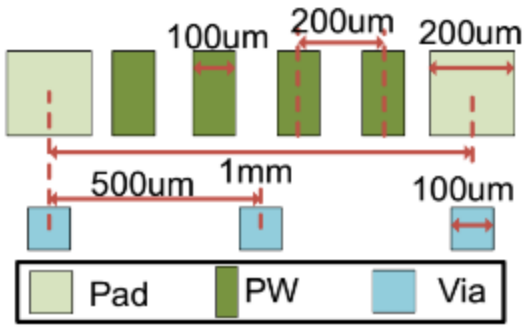
Interconnect architecture



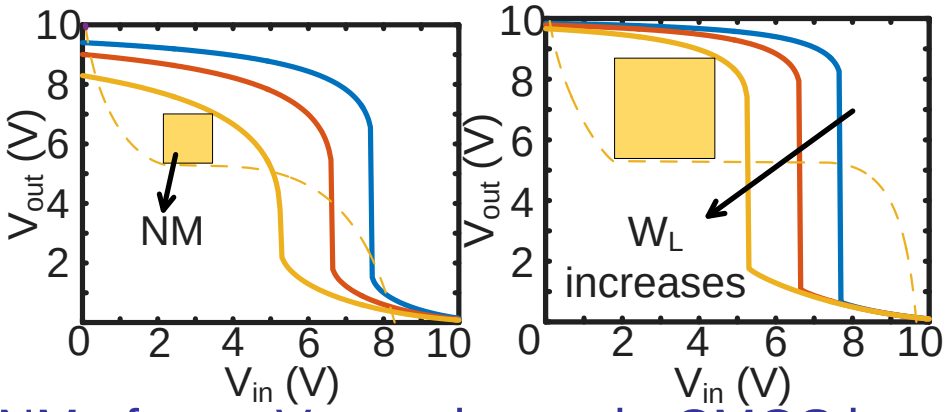
- **Pre-fabricated wires (GWs) ensure the routability.**
- **Printed wires (PWs) reduce the area overhead.**

Qinghang Zhao et al., DAC 2016

Array architecture comparison



Process parameters



NM of zero-V_{GS} and pseudo-CMOS inverter

NM is greatly improved compared with zero-V_{GS} logic.

Area and routability comparison with IGA and SOTG

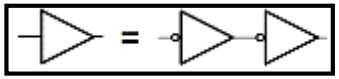
Circuit	IGA [7]		SOTG [8]		Pseudo-CMOS logic	
	TFT	Area[1]	TFT	Area[1]	TFT	Area[1]
RO15	60	1344	90	80	90	205
Counter4	200	4375	144	128	216	736
MUL3	414	20400	–[2]	–[2]	486	3570

[1] mm^2. [2] not routable.

Qinghang Zhao et al., DAC 2016

- **Noise margin is improved by pseudo-CMOS logic with unipolar devices**
- **Compared with IGA, 80% area is reduced with pseudo-CMOS logic array.**
- **Compared with SOTG, the routability is ensured.**

Design flow



Logic array design

Process parameters

Fabrication

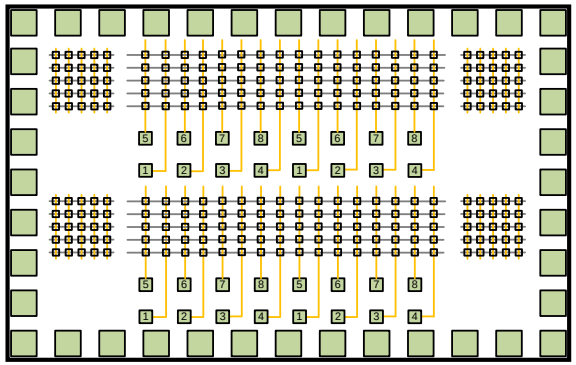
Device yield

Printing resolution

…

Circuit design

Logic array on foil



Synthesis

Test & Charcterization

Probe station & tools

Gate level netlist

Characterized logic array

Inkjet printer

Cell mapping

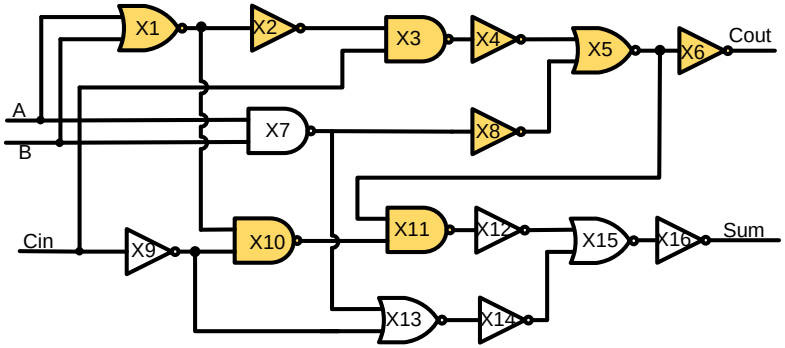
Wire routing

Implemented circuit

Cell mapping algorithms consider temp & strain effects

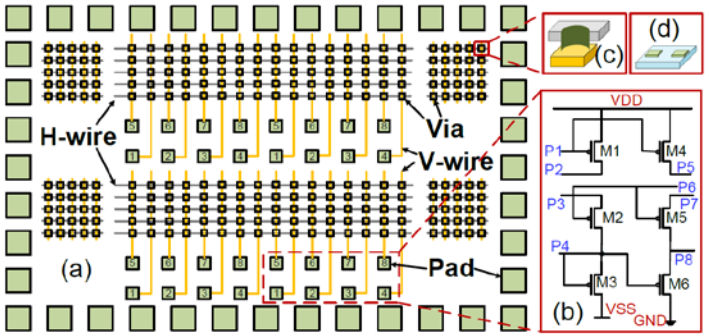
The defects and performance of TFTs/array cells are identified through test & characterization, hence improving circuit yield.

Mapping problem formulation



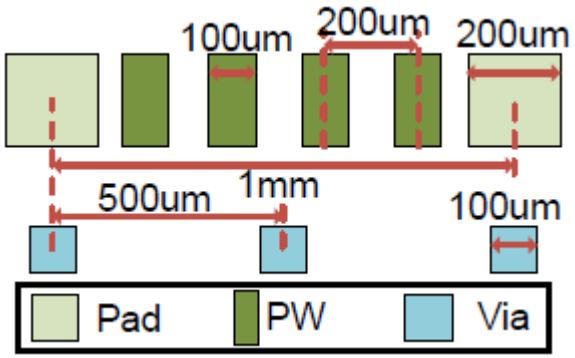
Netlist

?

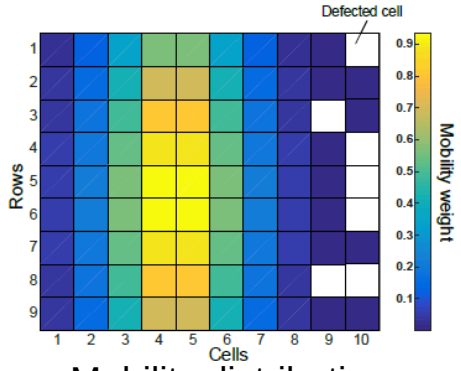


Logic array

- **Assumption**
  - Logic array has been tested and characterized
  - Strain & temp condition are pre-determined
- **Input**
  - Gate level circuit netlist represented by a graph $G(V, E)$
  - Parameters of logic array including
    - Array sizes and H-wire number
    - Size of pads and vias, pitch between pads
    - Capacity of each rows $|R_i|$ determined by test
    - Mobility weights w_{ij} evaluated by strain and temperature (w_{ij} shows average mobility of one cell)

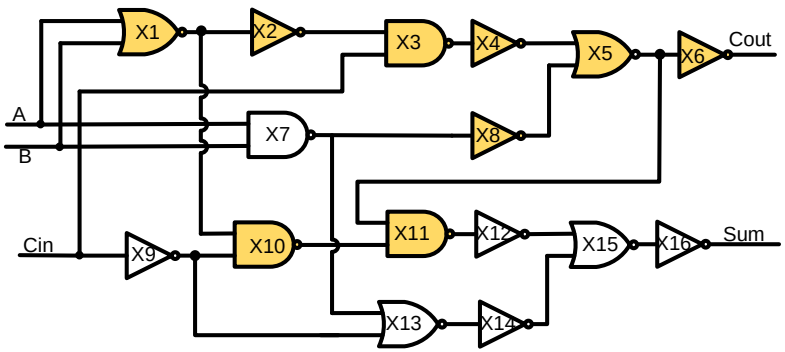


Design parameters of layout



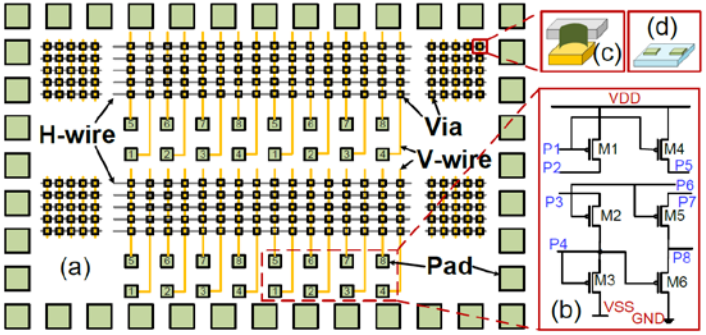
Mobility distribution

Problem formulation in 2 steps



$G(V, E)$

?

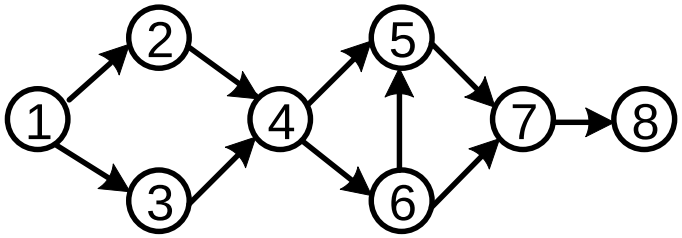


logic array

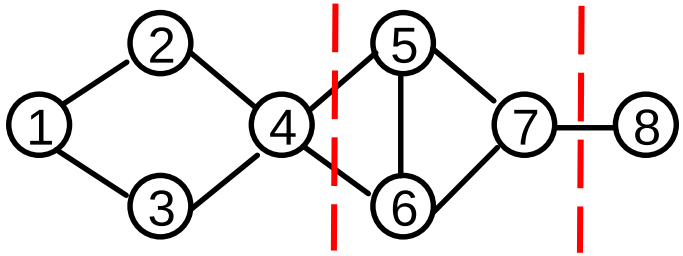
- **Inter-row problem (clustering)**
  - Minimum Cut: Given $G = (V, E)$, partition V into k disjoint sets $\{G_1, \dots, G_k\}$ such that the sum of $e(G_i, G_k)$, i.e., the number of edges in $\{(x, y) \in E | x \in G_i, \ y \in G_k\}$, is minimized
  - Capacity Constraints: $|G_i| < |R_i|$
- **Intra-row problem (mapping)**
  - MAP: $G \rightarrow R, MAP(g_i) = r_j, \forall g_i \in G, \exists r_j \in R$
  - Maximum flow: find a mapping function to maximum circuit performance
  - Minimum cost: find a mapping function to minimize routing cost

Goal: Maximum circuit performance with temp & strain consideration and enable routability.

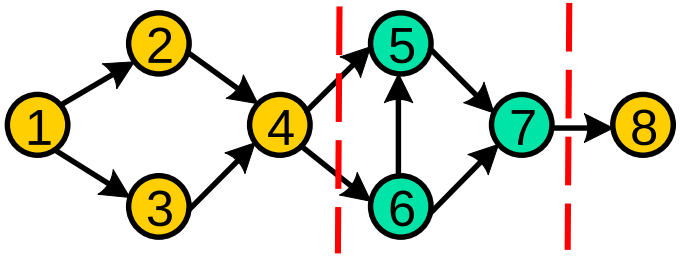
Algorithm for inter-row clustering



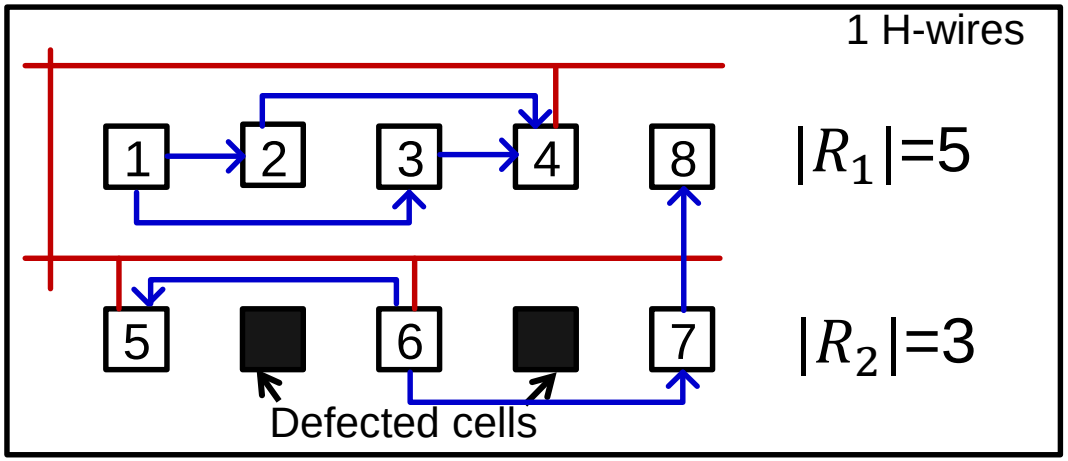
Circuit netlist



Simple min-cut clustering Spectral clustering cost



Adjustment according to capacity



Goal of spectral clustering:

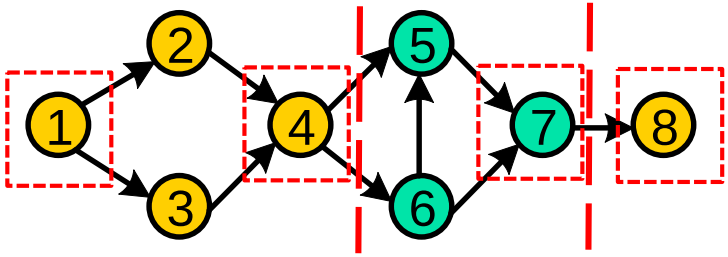
$$Minimize\ RatioCut = \sum_{i=1}^{k} \frac{cut(A_i, \overline{A_i})}{|A_i|}$$

Adjusted spectral clustering

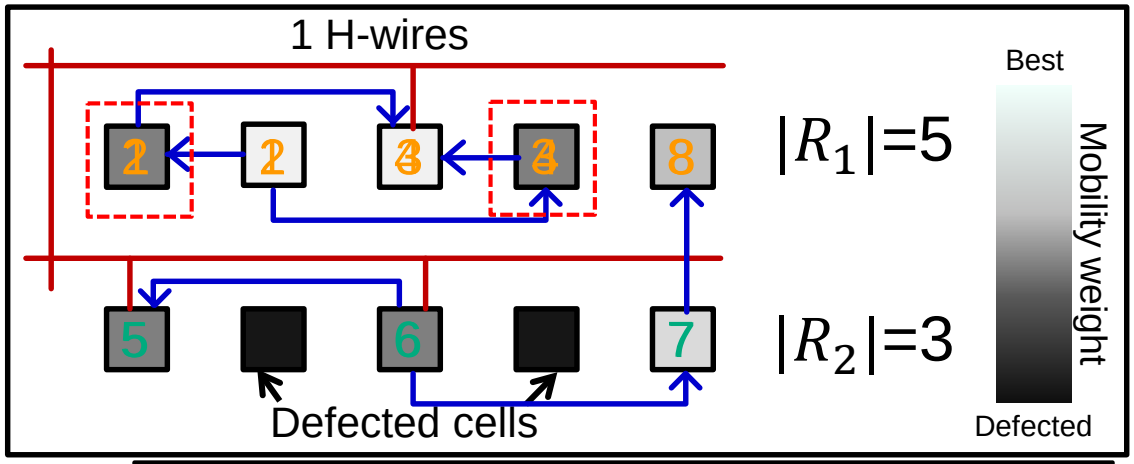
1. Describe circuit with undirected graph
2. Compute normalized graph Laplacians
3. Compute first k eigenvectors as $U \in R^{n \times k}$
4. Let y_i be the i-th row of U, cluster points y_i with k-means algorithm into k clusters
5. Adjustment according to row capacity, i.e., remove one farthest point in one cluster to anther if needed

Q: How to improve circuit performance with mobility variation

Algorithm for intra-row mapping



Adjustment according to capacity



Critical path (cp):

$1 \to 2 \to 4 \to 6 \to 5 \to 7 \to 8$

$1 \to 3 \to 4 \to 6 \to 5 \to 7 \to 8$

Sub-critical path (sp):

$1 \to 2 \to 4 \to 5 \to 7 \to 8$

$1 \to 3 \to 4 \to 5 \to 7 \to 8$

$1 \to 2 \to 4 \to 6 \to 7 \to 8$

$1 \to 3 \to 4 \to 6 \to 7 \to 8$

Define important degree of gate g_i

$$d(g_i) = a|\{cp_k | g_i \in cp_k\}| + b|\{sp_k | g_i \in sp_k\}|, a > b$$

$$d(g_1) = d(g_4) = d(g_7) = d(g_8)$$

$$> d(g_5) = d(g_6) > d(g_2) = d(g_3)$$

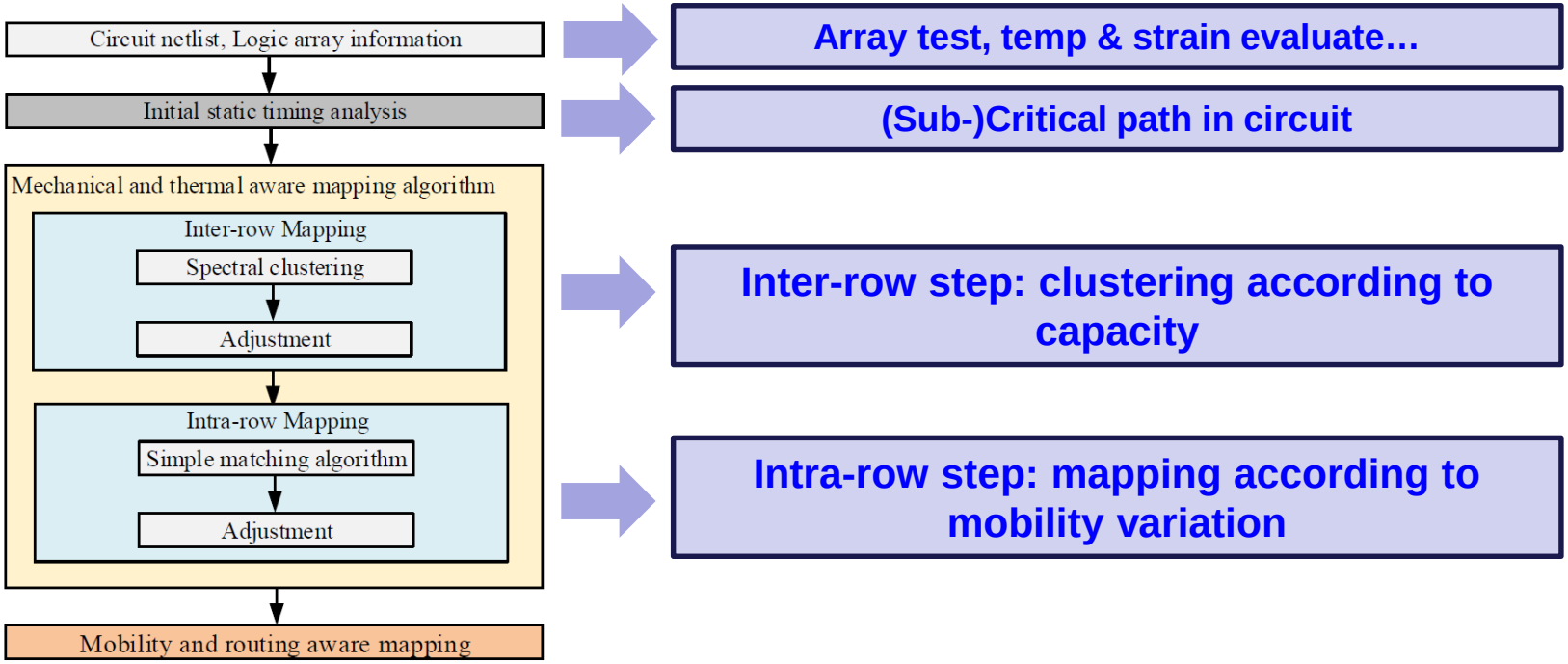
Key idea: improve circuit performance with limited routing resource

Intra-row mapping

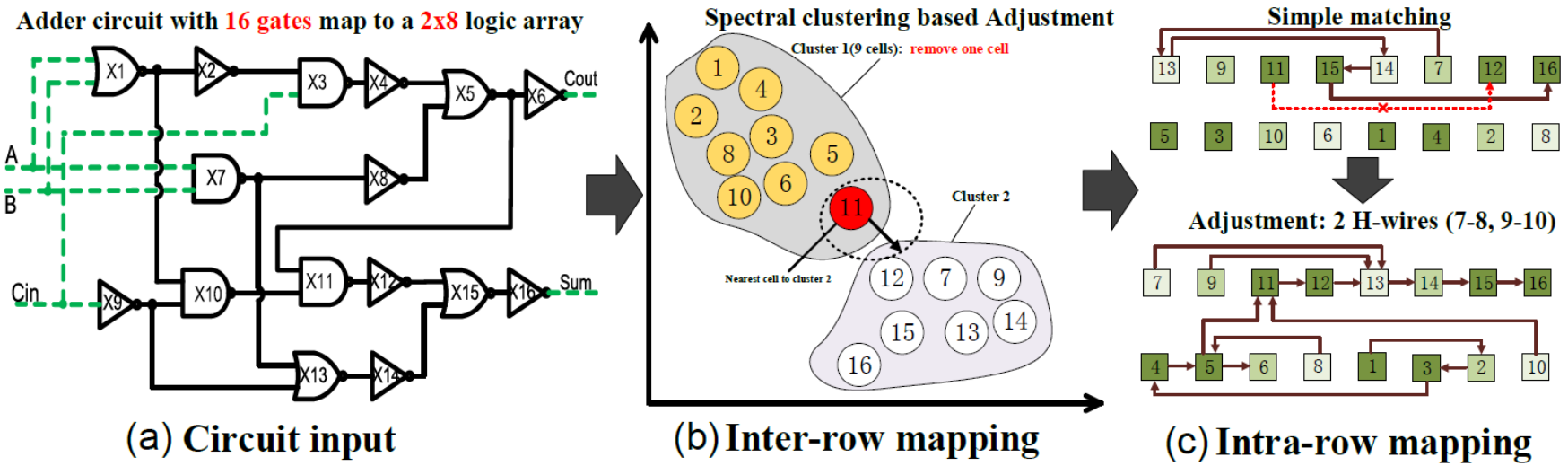
1. Static timing analysis of netlist
2. Calculate important degree of each gate
3. Mapping in order according to d and mobility weight w
4. GW assignment and one layer routing
5. If unroutable, take a heuristic method

```
while MAP.routability == False do
    for each row R in logic array do
        for each unroutable g_j mapping to r_j do
            Find r_k ∈ R that |w_j − w_k| < ε_0;
            Exchange(w_j, w_k) to calculate E.routcost;
            if E.routcost ≤ R.routcost then
                MAP(g_i) = r_k, MAP(g_k) = r_i;
                Update R.routcost;
            end
        end
    end
    Increase(ε_0);
end
```

Algorithm flow and a design case

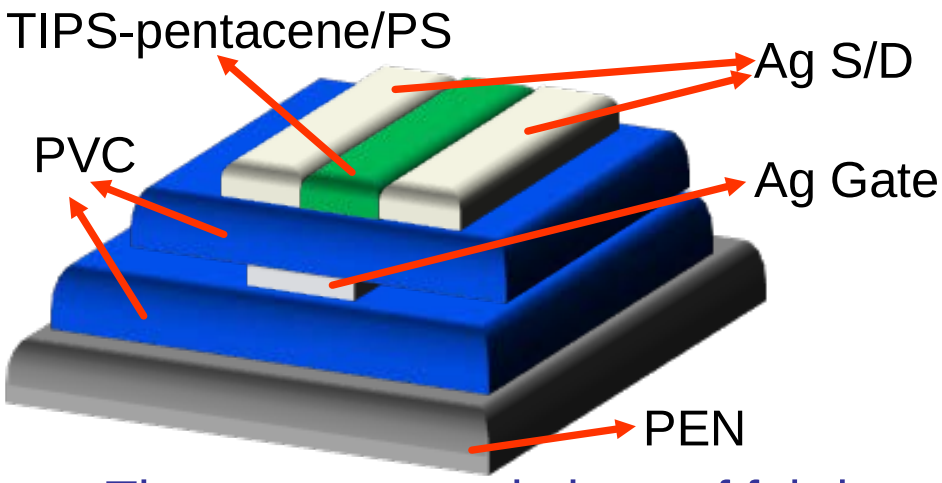


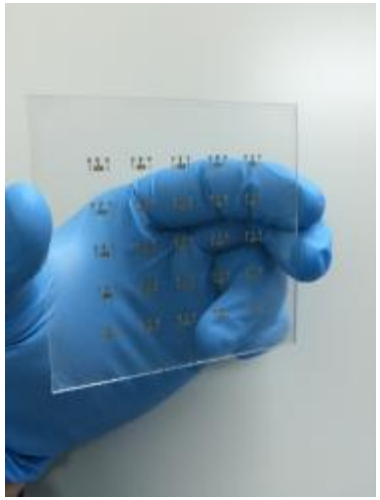
Algorithm flow



(a) Circuit input (b) Inter-row mapping (c) Intra-row mapping

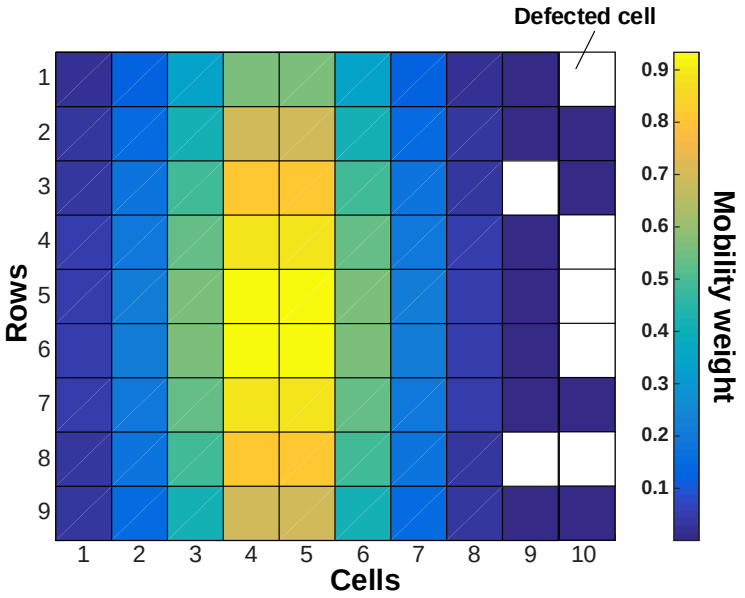
Experiment setup



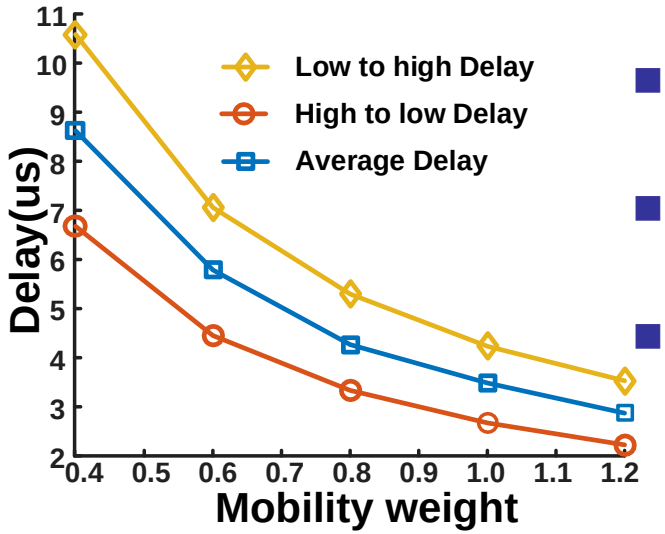


- Printed & all solution process
- p-type
- μ: 0.6cm^2/Vs

The structure and photo of fabricated SAM OTFT



Mobility distribution in experiment



Mobility effect on inv cell delay

- Level 40 HP TFT model
- VSS=-10 & VDD=5V
- Delay evaluated by mobility weight

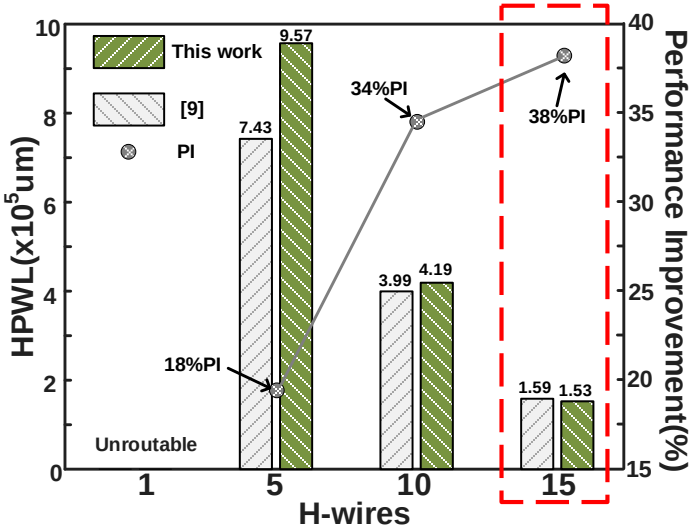
Experiment

Nearly same HPWL of printed wire but 38% PI

Information of benchmark circuits

Circuit	# of INV	# of NAND	# of NOR	Array size
Adder2	8	4	4	2×10
Counter4	8	24	4	4×10
Mul3	36	33	12	9×10

*#: Number of



Implement of 3-bit multiplier with different H-wire numbers

Trade off the routing resources and circuit performance effectively

Comparison with [9] (DAC2017's work) and this work

Circuit	H-wires	HPWL($\times 10^5 \mu m$)		Critical Path Delay(μs)		PI
		[9]	Proposed	[9]	Proposed	
Adder2	1	0.53	0.58	31.14	22.13	41%
	3	0.49	0.54			
Counter4	4	1.11	2.70	76.12	54.34	40%
	8	0.91	2.51			
Mul3	4	8.56	10.92	69.20	74.35	7%
	13	1.67	1.92		95.54	38%

*Performance Improvement (PI): $(\frac{Delay\ of\ [9]}{Delay\ of\ this\ work} - 1) \times 100\%$

*HPWL: Half perimeter wire length of printed wires

*VDD/VSS/GND/INPUT/OUTPUT terminals are not included in H-wire number

Conclusion

- Architecture of pseudo-CMOS logic array based on TFTs is reviewed
- 2-steps mapping algorithms considering mechanical strain and temperature effect on TFTs are proposed for a pseudo-CMOS logic array
  - Inter-row clustering algorithm to overcome the defected cells effect
  - Intra-row mapping algorithm to deal with the mobility variation problem
- Experiment shows this work can effectively improve circuit performance while enable routability

Reference

[1] E. Cantatore et al., “A 13.56-mhz rfid system based on organic transponders,” IEEE Journal of Solid-State Circuits, vol. 42, no. 1, pp. 84–92, 2006.

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