Hewlett Packard Enterprise

UCSB

STANFORD

香港科技大學
THE HONG KONG UNIVERSITY OF SCIENCE AND TECHNOLOGY

Process Design Kit for Flexible Hybrid Electronics

Leilai Shao[1], Tsung-Ching Jim Huang[2], Ting Lei[3], Ray Beausolail[2], Zhenan Bao[3], and Kwang-Ting Cheng[1,4]

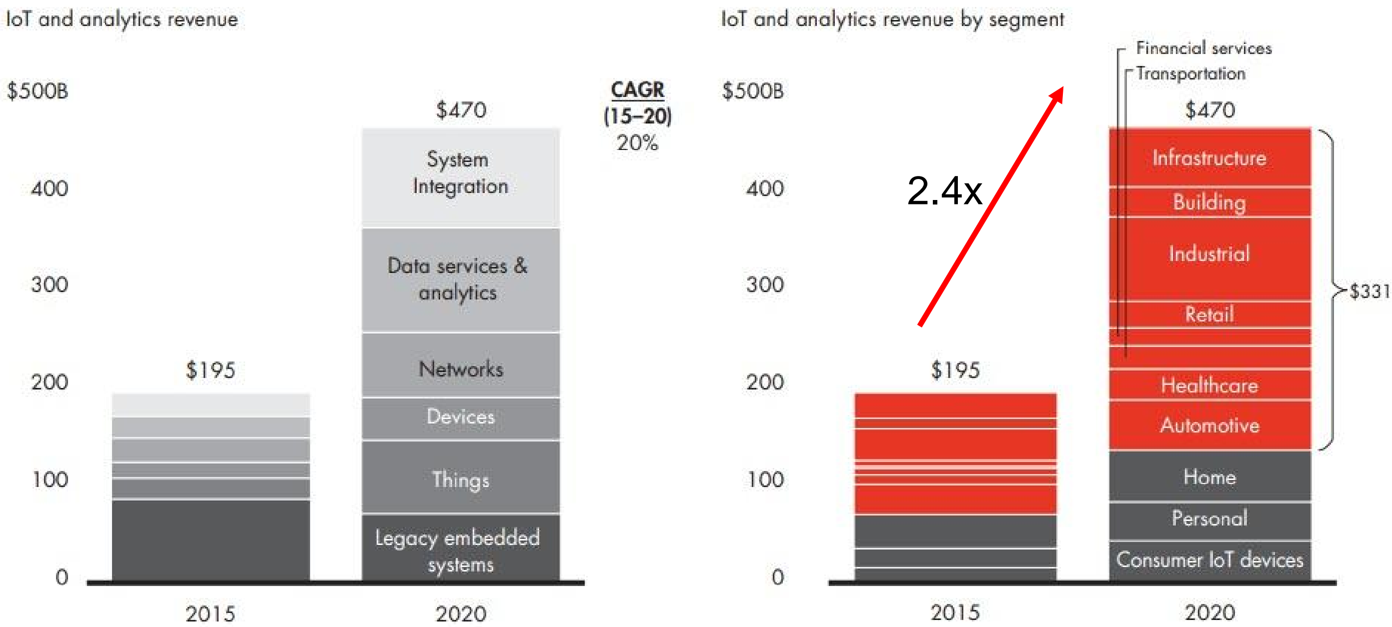
[1]Electrical and Computer Engineering, UC-Santa Barbara, USA
[2]Hewlett Packard Labs, Hewlett Packard Enterprise, USA
[3]Chemical Engineering, Stanford University, USA
[4]Electronic and Computer Engineering, HKUST, China

IEEE ASP-DAC 2018

Outline

- Introduction
  - Flexible hybrid electronics (FHE)
  - Design challenges and opportunities for flexible hybrid electronics
  - Process design kit for FHE Manufacture-Design Ecosystem (FHE-PDK)
- Driving Technology: Carbon-nanotube devices and design rules
  - Comparison among thin-film transistor (TFT) technologies
  - Carbon-nanotube thin film transistors (CNT-TFTs)
  - Carbon-nanotube resistors
- Process Design Kit Implementation
  - Device modeling for CNT based passive and active devices
  - Design verification (DRC/LVS/LPE) for printed carbon-nanotube circuits
- Conclusion and Future Outlook

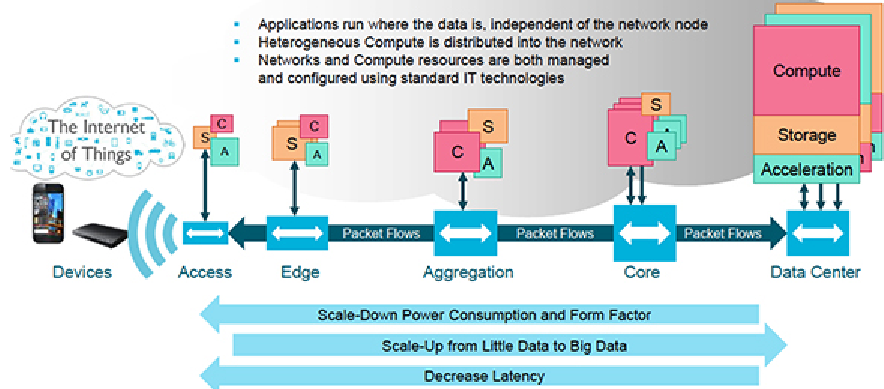
IoT Market Growth by Market Segments 2015-2020



Intelligent IoT Infrastructure with IoT Nodes

Node #1
Node #2
Node #3
Node #4
Node #5
Node #6
Node #7
Node #8
AI Cloud /HPC Unit

Supervise
Control
Update

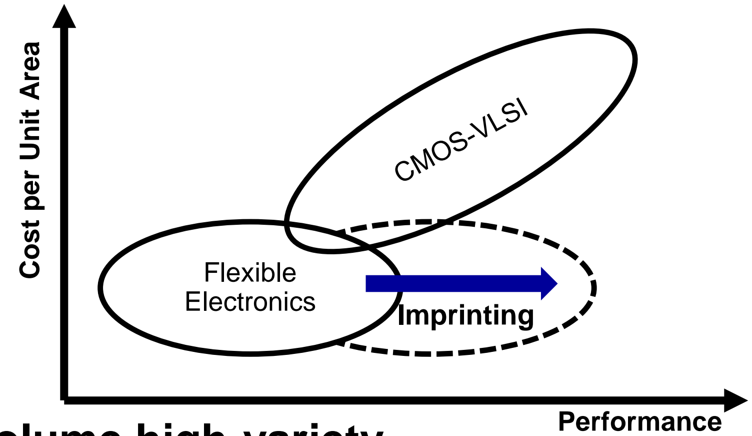


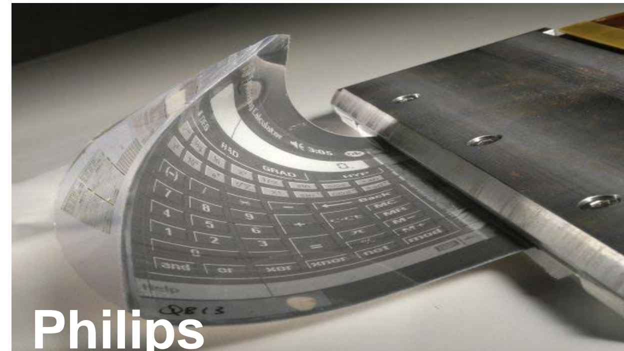
Source: ARM

IIoT nodes and edges are capable of sensing and performing applications and analytics locally where the data is generated for actionable insights. IIoT node/edge only updates key information to the cloud with to enhance data security, reduce latency, and save power.

Flexible Electronics for Edge Computing/IoT

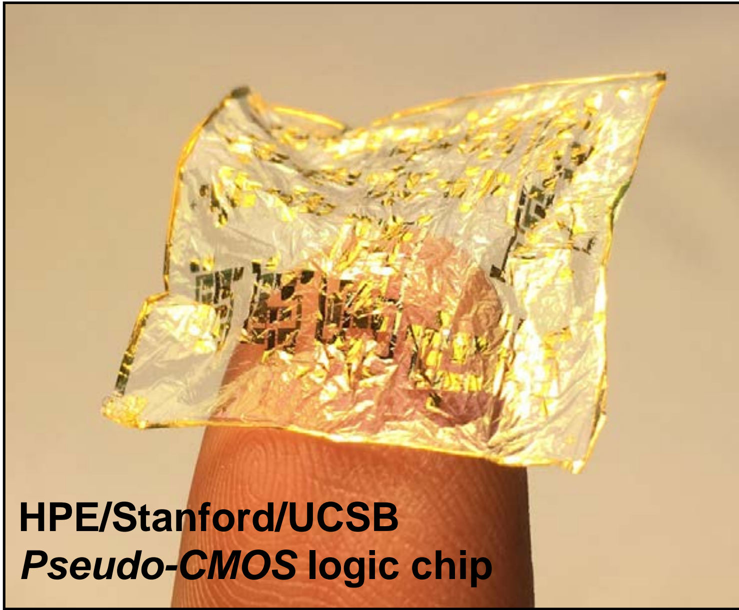
- Printable, light-weight and low-cost
- Bendable, stretchable, and durable
- Suitable for high-volume manufacturing
  - Industrial-grade multi-jet printing
  - Roll-to-roll imprinting (nano-to-micro scale)
- Complementary to Si-CMOS VLSI
  - Low non-recursive expense (NRE) for small-volume high-variety



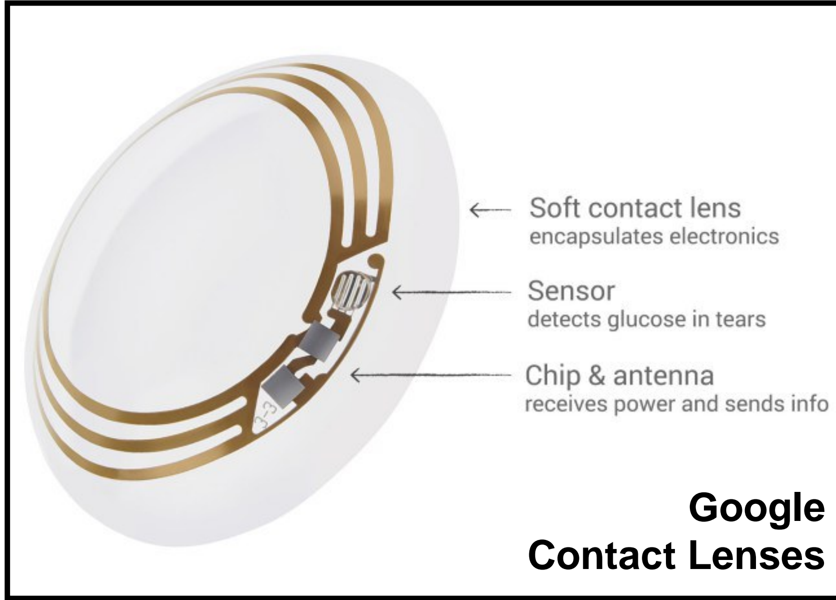


Flexible Hybrid Electronics for Intelligent IoT Nodes

– By heterogeneous integration of flexible active and passive devices (ex. transistor, interconnect, resistor, capacitor, antenna, and battery etc) with ultra-thin low-power silicon chips, our research goal is to bring the machine intelligence to various "things" and make them smarter with learning



Carbon-Nanotube Logic



Glucose Sensor SOC

NextFlex is Established by US DoD/FlexTech in 2015

Mission:
Usher in the era of "electronics on everything" and advance efficiency of our world

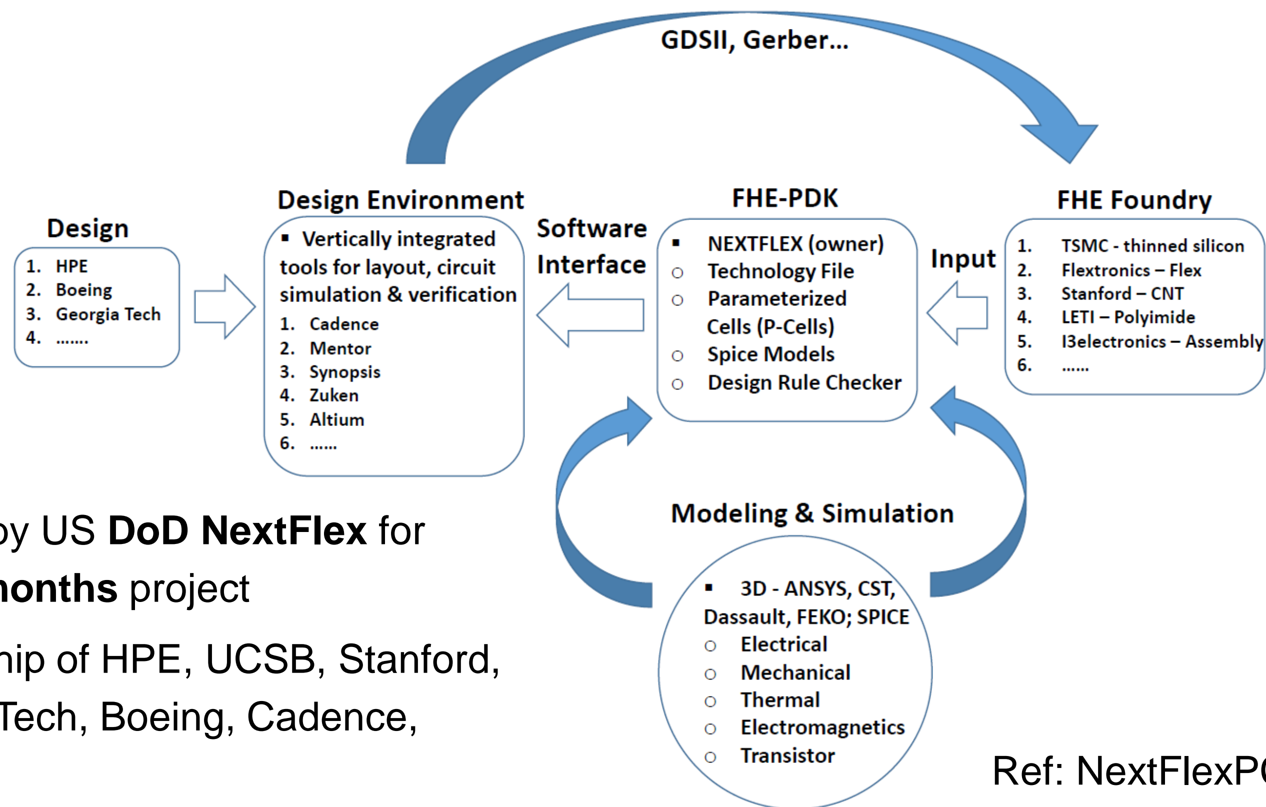
ABOUT NEXTFLEX
BUILDING THE NEXT BIG THING IN FHE

The formation of NextFlex has been a benefit to the rapidly expanding field of Flexible Hybrid Electronics (FHE).

Formed in 2015 through a cooperative agreement between the US Department of Defense (DoD) and FlexTech Alliance, NextFlex is a consortium of companies, academic institutions, non-profits and state, local and federal governments with a shared goal of advancing U.S. Manufacturing of FHE. By adding electronics to new and unique materials that are part of our everyday lives in conjunction with the power of silicon ICs to create conformable and stretchable smart products, FHE is ushering in an era of "electronics on everything" and advancing the efficiency of our world.

$75M federal fund
$181M with cost-share
2015 – 2020
Self-sustainable afterward

Process Design Kit for Flexible Hybrid Electronics

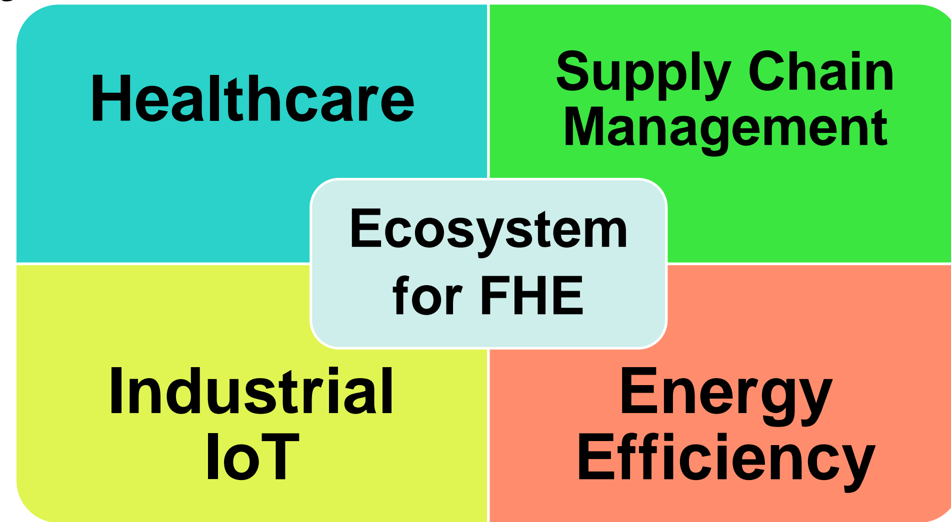


- Funded by US **DoD NextFlex** for **$3M/18months** project
- Partnership of HPE, UCSB, Stanford, Georgia Tech, Boeing, Cadence, ANYSYS
- Open-source to NextFlex members

Ref: NextFlexPC2.0 Proposal

Open Ecosystem for Flexible Hybrid Electronics

- Create an ecosystem connecting applications/product companies and third party OEM/ODM vendors
- Interface between system architect/circuit designer and manufacturer
- Protecting IP from competitors; open-source for R&D purposes



Driving Technology:
Carbon-nanotube Flexible Electronics

Comparison Among Flexible Thin-Film Transistors

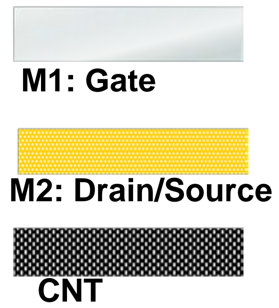
TFT Technology	Amorphous Si	Metal-Oxide	SAM-Organic	Ink-Jetted Organic	Carbon Nanotube
Process Temperature	250 ℃	< 100 ℃	< 100 ℃	Room Temp.	Room Temp.
Process Technology	Lithography	Roll-to-Roll Lithography	Shadow Mask	Ink-Jet Printing	Roll-to-Roll/Inkjet /Lithography
Feature Size	8 μm	2 μm	50 μm	50 μm	2 μm
Substrate	Glass/plastics	Glass/plastics	Wafer/plastics	Glass/plastics	Wafer/plastics
Device Type	N-type	N-type	N/P-type	P-type	N/P-type
Supply Voltage	20V	5V	2V	40V	2V
Mobility (cm^2/Vs)	1	10	0.01/0.5	0.01	>25
Cost / Area	Medium	Low	Low	Low	Very Low
Lifetime	Good	Good	Poor/Medium	Poor	Poor/Good

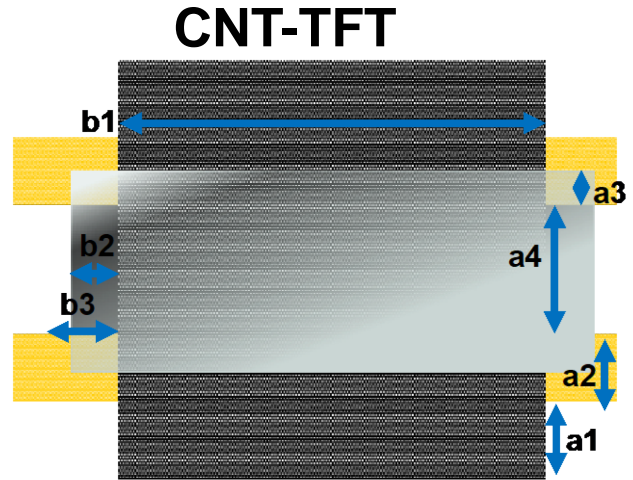
Design Challenges for Flexible Hybrid Electronics

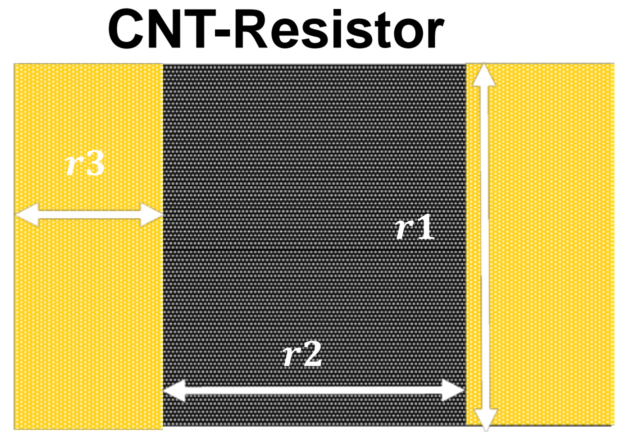
- **Circuit design:**
  - –Slow carrier mobility (~ 1-25 cm^2/Vs) → limited operation speed
  - –Large feature size (L_{MIN} ~ 20 μm) → large parasitics (R/C)
  - –Mono-type devices → poor noise margin; high static power
  - –Inferior reliability (bias-stress or chemical) → poor operation lifetime
  - –Large process variations (>50%) → device mismatches
- **Design Verification:**
  - –Lack of design rule checking → prone to manufacturing yield loss
  - –Lack of layout versus schematics checking → prone to design errors
  - –Lack of layout parasitic extraction → inaccurate simulation results
  - –Lack of co-simulation environment of printed circuit and silicon chips → need to perform physical verification and simulation separately; lower productivity

Carbon-nanotube Active and Passive Devices

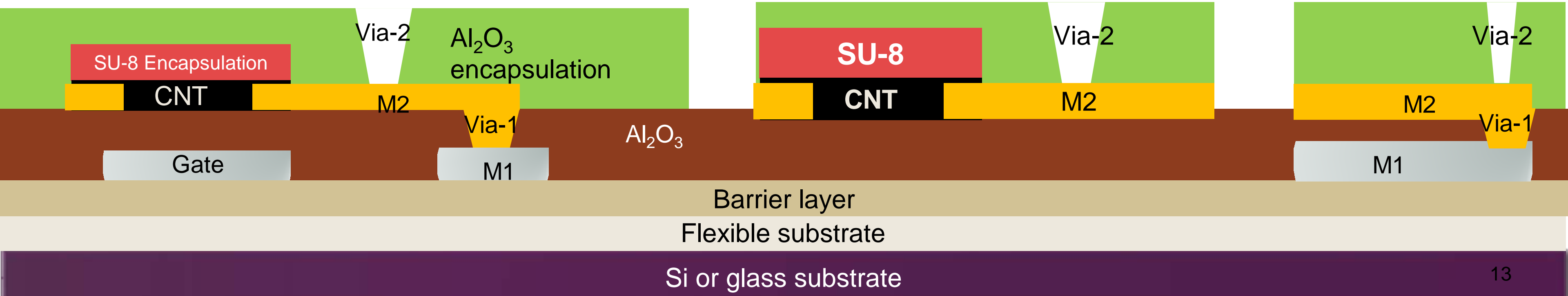
Top View:







Cross View:



Ultra-thin Flexible CNT-TFTs on 1-μm Thick Foil

Photo for Ultra-thin flexible CNT-TFTS

- **P-type device only**
- **High mobility ~25cm²/Vs**
- **Low operation voltage ~2V**
- **ON/OFF ratio ~ 10^2**

Measured CNT-TFT I-V curves, channel=25um

V_{DS} = -0.5, ..., -2V

$-I_D$ (Aμm^{-1})

10^{-7} 10^{-8} 10^{-9} 10^{-10} 10^{-11}

V_{GS}

-2 -1.5 -1 -0.5 0 0.5 1

V_{DS}

-2 -1.5 -1 -0.5 0

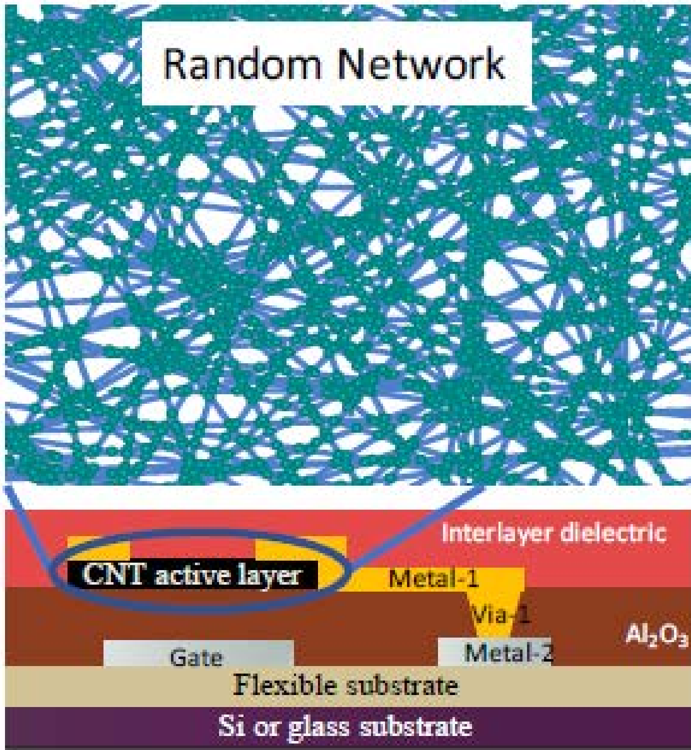
V_{GS} = 0, -0.5, ..., -2V

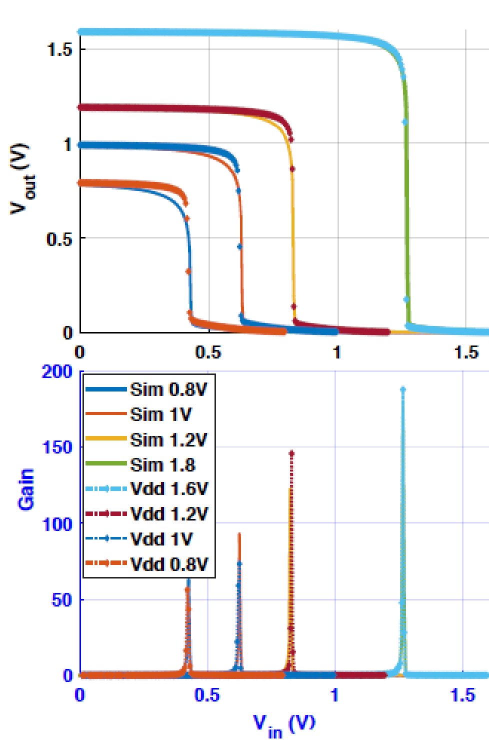
$-I_D$ (Aμm^{-1})

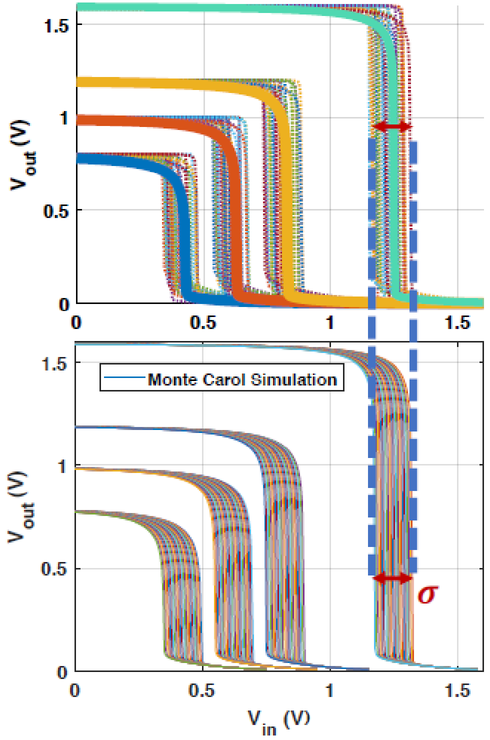
2.5 2 1.5 1 0.5 0

$\times 10^{-7}$

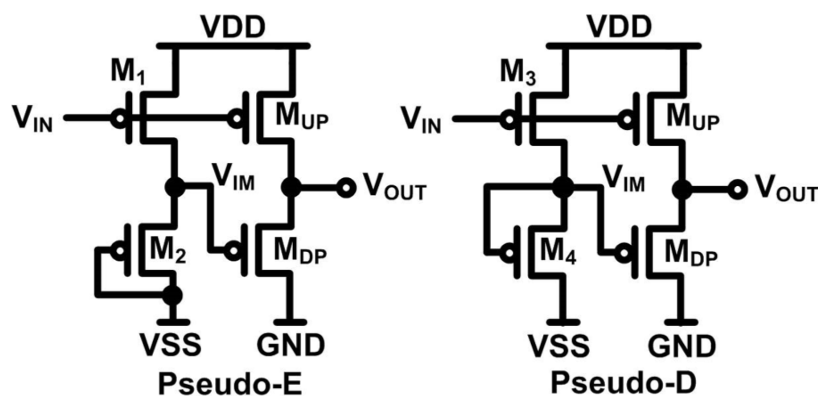
Ultra-Low Voltage (0.8V) Pseudo-CMOS CNT Circuits







Pseudo-CMOS for Printable Circuits



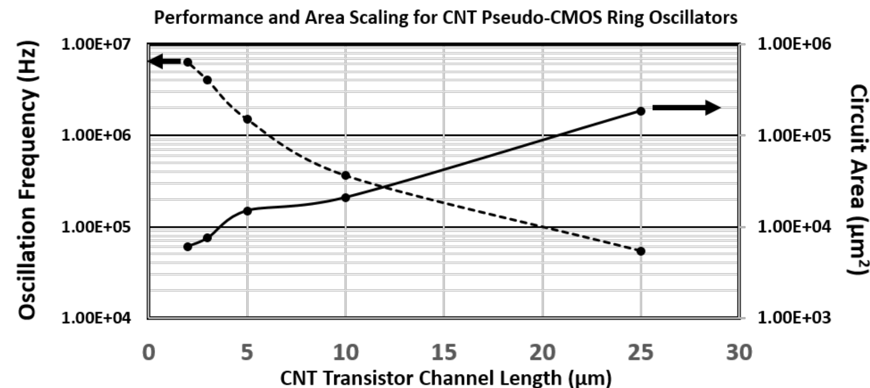
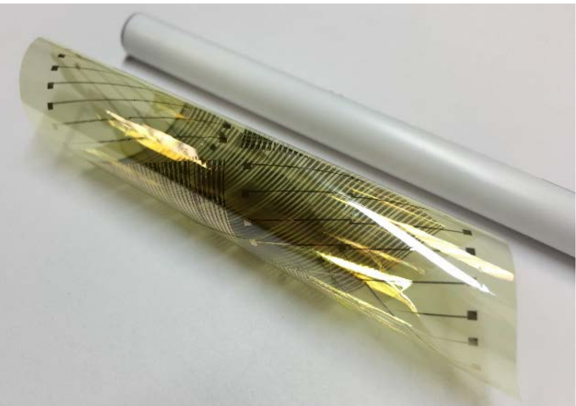


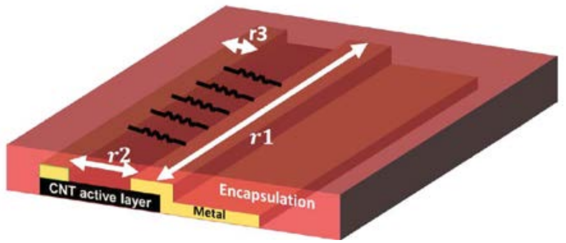
Table 1: Comparison of State-of-the-art Flexible NFC and RFID Tags.

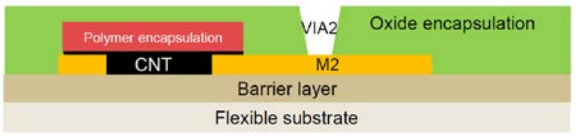
Design Example	NFC [2]	NFC [3]	NFC [4]	RFID [5]	RFID [6]
Logic Style	Pseudo-CMOS	Pseudo-CMOS	Pseudo-CMOS	Diode-load	Zero-VGS
Circuit Area (mm^2)	50.55	10.9	15.8	8.05	70
# of Supply Voltages	3	3	3	2	2
Ring-Osc Stage Delay (ns)	2.4	63	570	349	909000
Data Rate (kb/s)	105.9	396.5	43.9	71.6	0.05
Power (mW)	7.5	64	63.5	93.2	0.02

Source: [2-4] K. Myny et al, ISSCC17', 16', 15'; [5] B. Yang et al, ETRI Journal; [6] H. Ozaki et al, VLSI'11

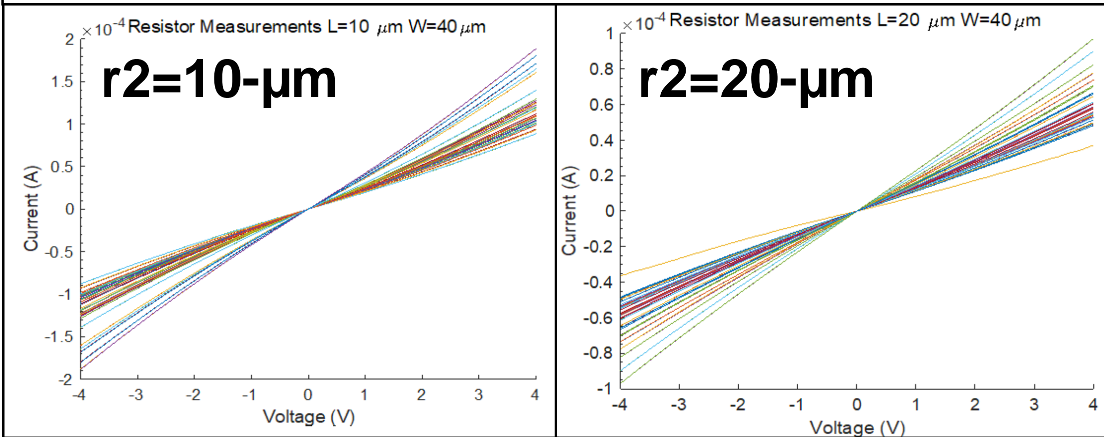
Flexible Carbon-Nanotube Resistor Array

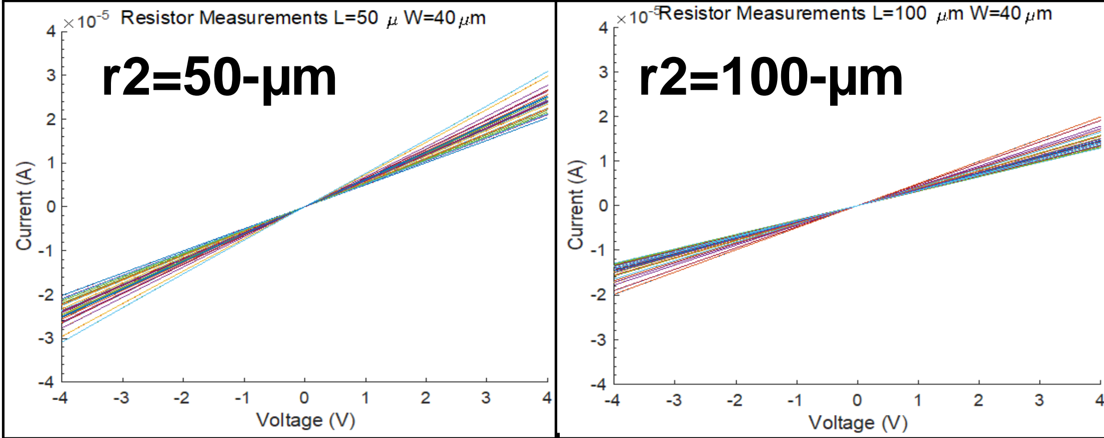






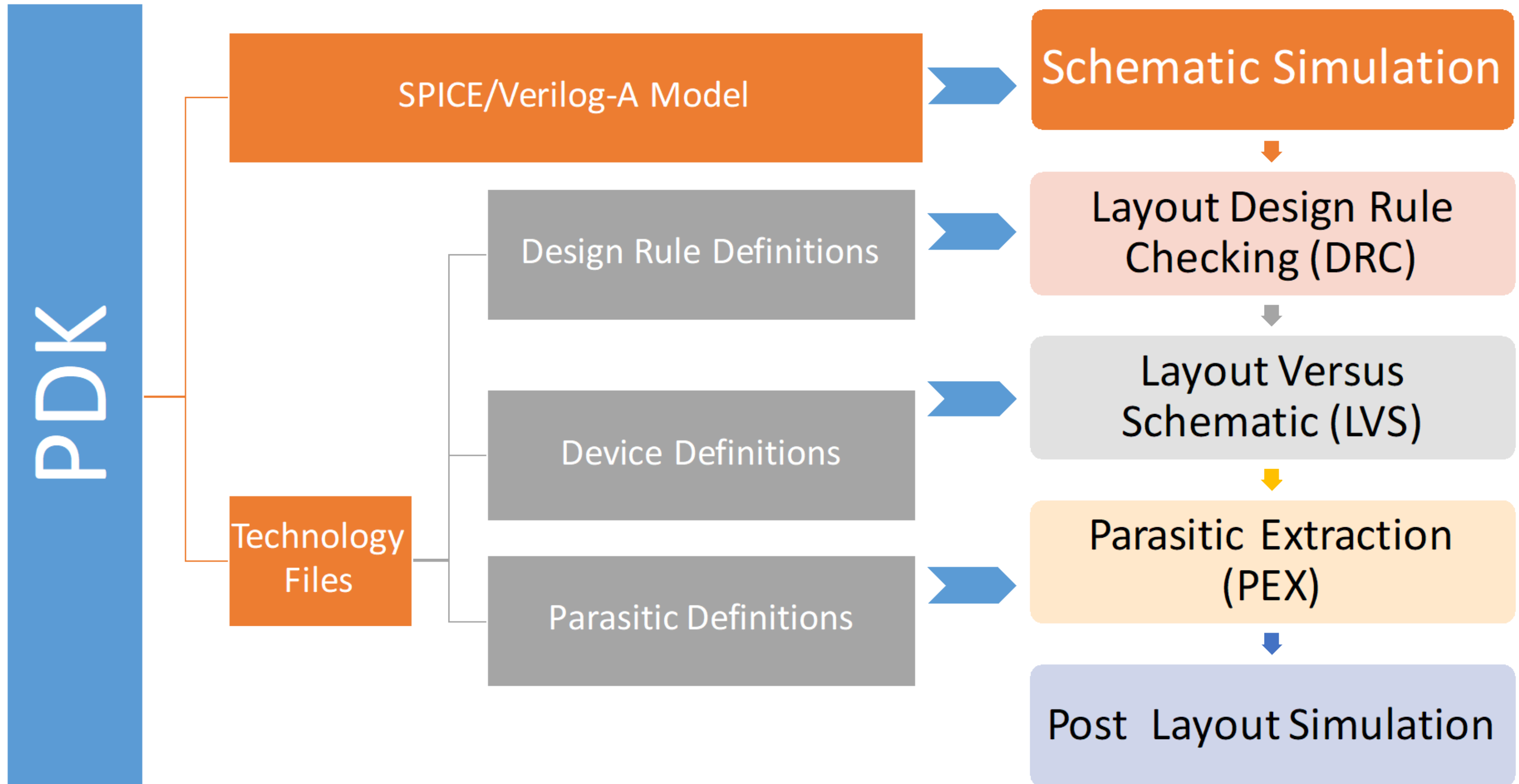
Measured I-V curves for CNT Resistor Array



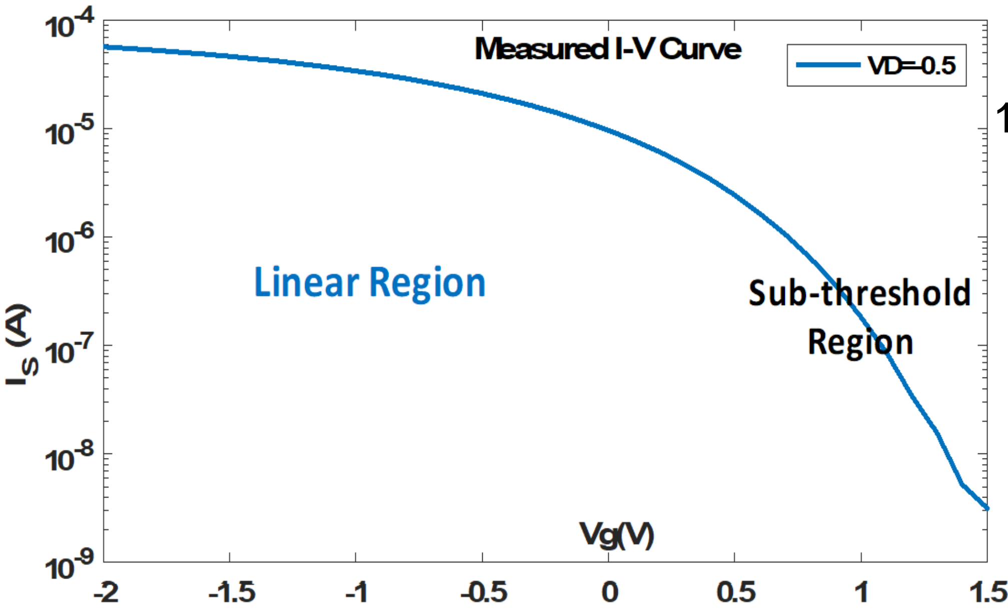


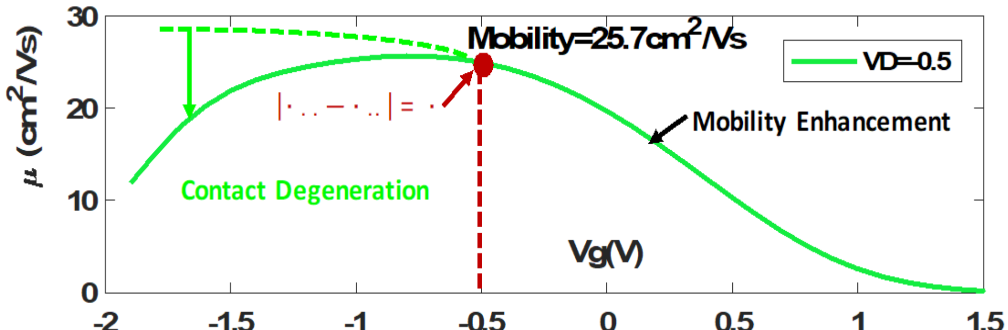
FHE-PDK Implementation

Database Structure for FHE-PDK



CNT-TFT Modeling





Observations:

1. Mobility enhancement at low gate bias
   - Most acceptable theories are tail-distributed traps (TDTs) and variable range hop-ping (VRH). Both indicate the mobility dependency on gate voltage by Eq. (1) .

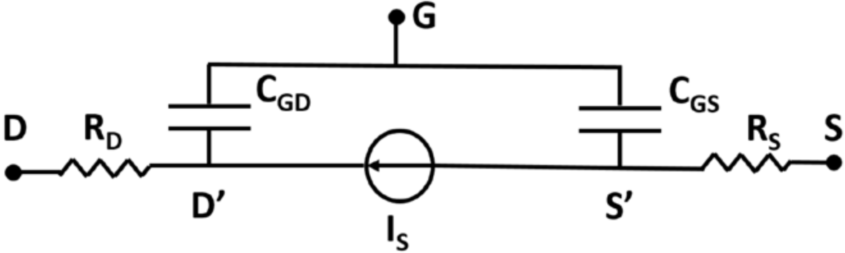
$$\mu = \begin{cases} \mu_0(V_G - V_{th})^\gamma, & \text{N-type TFT} \\ \mu_0(V_{th} - V_G)^\gamma, & \text{P-type TFT} \end{cases} \tag{1}$$

2. Mobility degeneration at high gate bias:
   - The degeneration of mobility at high V_{SG} can be explained by the contact resistances $R_C=R_S+R_D$ at source/drain terminals;
   - The contact resistances will cause a degeneration of the effective mobility as shown by Eq. (2)-(3).

$$\tilde{I}_{SD} \approx \frac{WC_{ox}\mu}{L\{1+kR_C(V_{th}+V_{SG})\}}\{(V_{th}+V_{SG}) - \frac{1}{2}V_{SD}\}V_{SD} \tag{2}$$

$$\frac{\tilde{I}_{SD}}{I_{SD}} \approx \frac{\tilde{\mu}}{\mu} = \frac{1}{1+kR_C(V_{th}+V_{SG})};\ k = \frac{W}{L}C_{ox}\mu \tag{3}$$

CNT-TFT Model Validation



Compact Model Schematic

$$I_{SD} = \frac{k}{\gamma+2}(f(V_G,V_S)^{\gamma+2} - f(V_G,V_D)^{\gamma+2})(1+\lambda V_{SD})$$

$$f_{\lim}(V_G,V) = SS\ln[1+\exp(\frac{V_{th}-V_G+V}{SS})]$$

Current Model

- Based on previous two observations, a compact model for CNT-TFT is presented here.
- Good match between measurements and model further validate our analysis

Model Validation

Transfer Curve V_S=0V, V_D=-0.5V

Measure
Model
I_{SD} (A)
10^{-4}
10^{-6}
10^{-8}
10^{-10}
-2
-1
0
1
V_{GS}

V_{GS}
-2
-1
0
1
2
Measure
Model
I_{SD} (A)
6
4
2
0
-2
$\times 10^{-5}$

CNT-TFT Model Validation and Parameter Extraction

- A wide range of VGS ∈ [−2, 0]V and VDS ∈ [−4, 0]V, covering sub-threshold, linear and saturation, are investigated;
- Device parameters are extracted out of 52 fabricated CNT-TFTs, where a Gaussian distribution is assumed for process variations. All extracted parameters are summarized in Table III, where the mean value μ and standard deviation σ are provided.

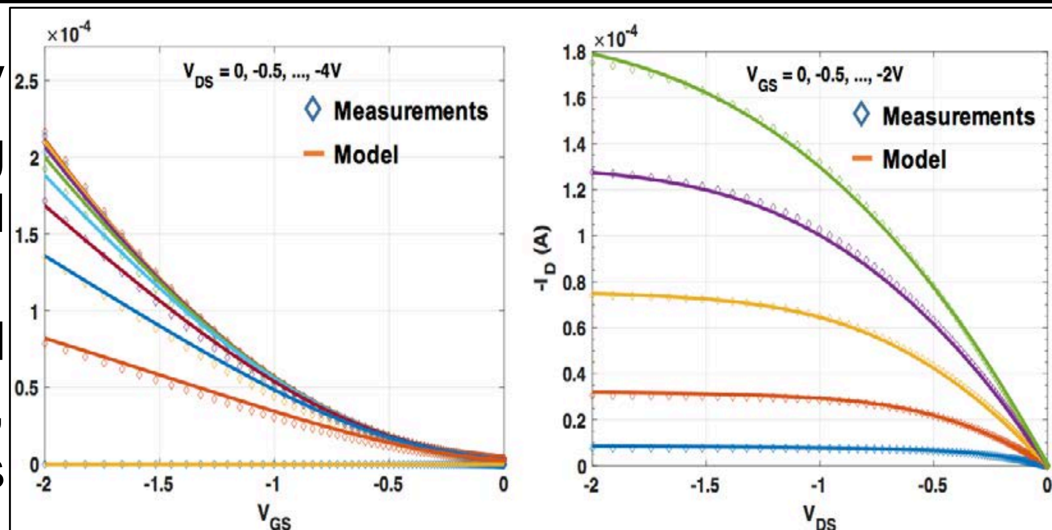
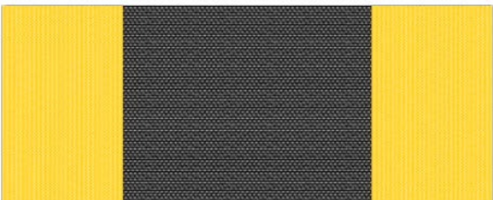
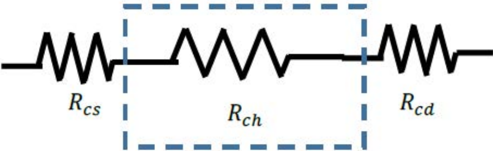


TABLE III: Parameters extracted from 52 fabricated CNT-TFTs

Model Parameter	Notation	[μ, σ] Unit
Channel Length	L	[25, -] um
Channel Width	W	[125, -] um
Gate S/D Overlap	L_{ov}	[10, -] um
Gate Unit Capacitance	C_{ox}	[200, -] nF/cm^2
Threshold voltage	V_{th}	[0.5, 0.102] V
Sub-threshold Swing	SS	[0.28, 0.0388] V/dec
Effective Mobility	μ_0	[25.69, 0.19] cm^2/Vs
Contact Resistance	R_C	[1531, 291] Ω
Channel Length Modulation	λ	[0.064, 0.0185] V^{-1}
Factor of Gate Dependent mobility	γ	[0.20, 0.116] (-)

CNT-Resistor Modeling





Simplification: high frequency components, such as parasitic capacitor and inductor are ignored here.

$$R_{toal} = \frac{R_c}{W} + \frac{R_{ch}L}{W}$$

Decomposition:

- R_{total} is composed of contact resistance R_c and channel resistance R_{ch}.
- R_c and R_{ch} can be extracted from the right figure, where the slope determines the R_{ch} and intersection determines the R_c.s

Res$_{total}$ KΩ v.s. Channel Lenght W=40um

Res_{toal} = 2.46*L + 4.78

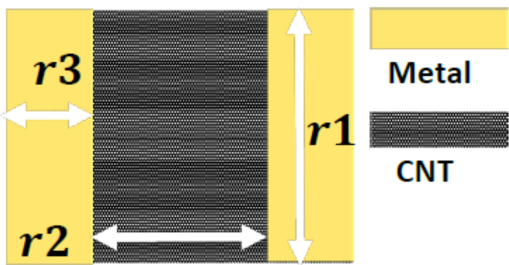
Res$_{total}$ KΩ

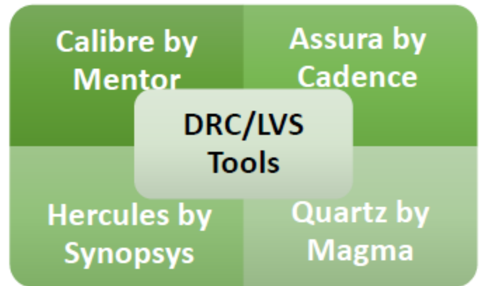
350
300
250
200
150
100
50
0

0 20 40 60 80 100

Channel Length μm

Physical Verification Implementation Procedures





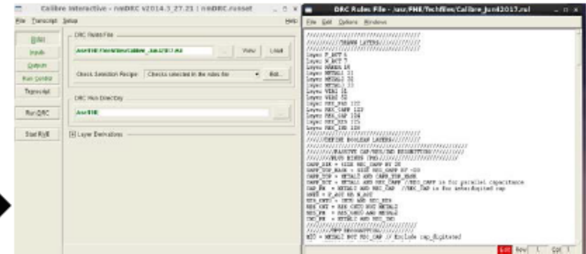
Design Rules Based on Fabrication Results

Translate to Standard Verification Rule Format(SVRF)

Implement in Mentor (Interoperable with other tools)

Design Rules	Descriptions	Dimensions (μm)
r1	Res Width	4 - 200
r2	Res Length	10 - 100
r3	Metal enclosure	2 - 100

Basic Components of Rule Files
Pseudo-Code
Layer Assignments
Global Layer Definitions
Include Statements
Rule Check Statements {
Local Layer Definitions
Layer Operations
Rule Check Comments
}

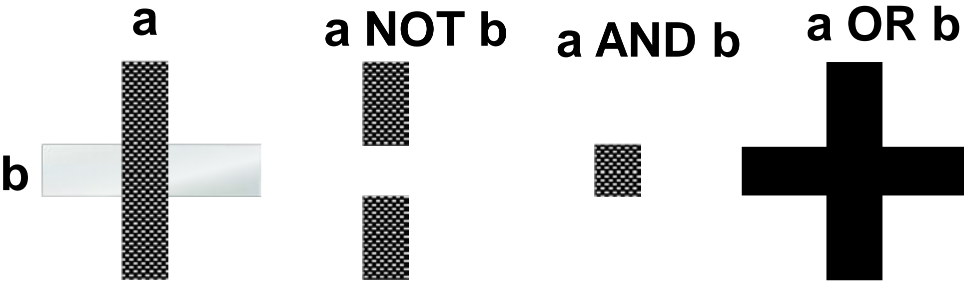


Mentor Calibre DRC Interface

technology files

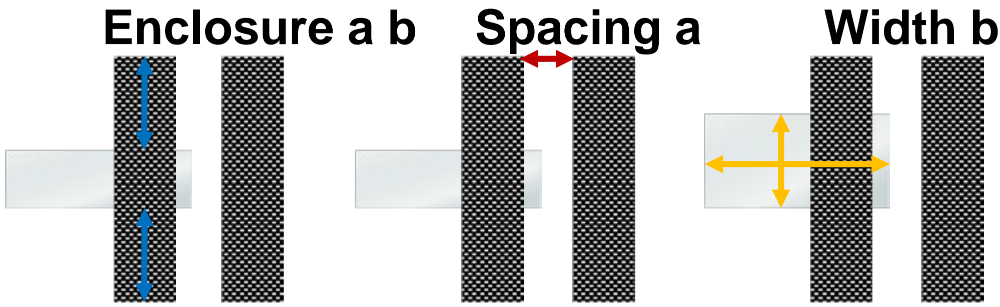
Layer Derivation and Design Rule Checking

Layer Derivation Operators:
NOT, AND & OR



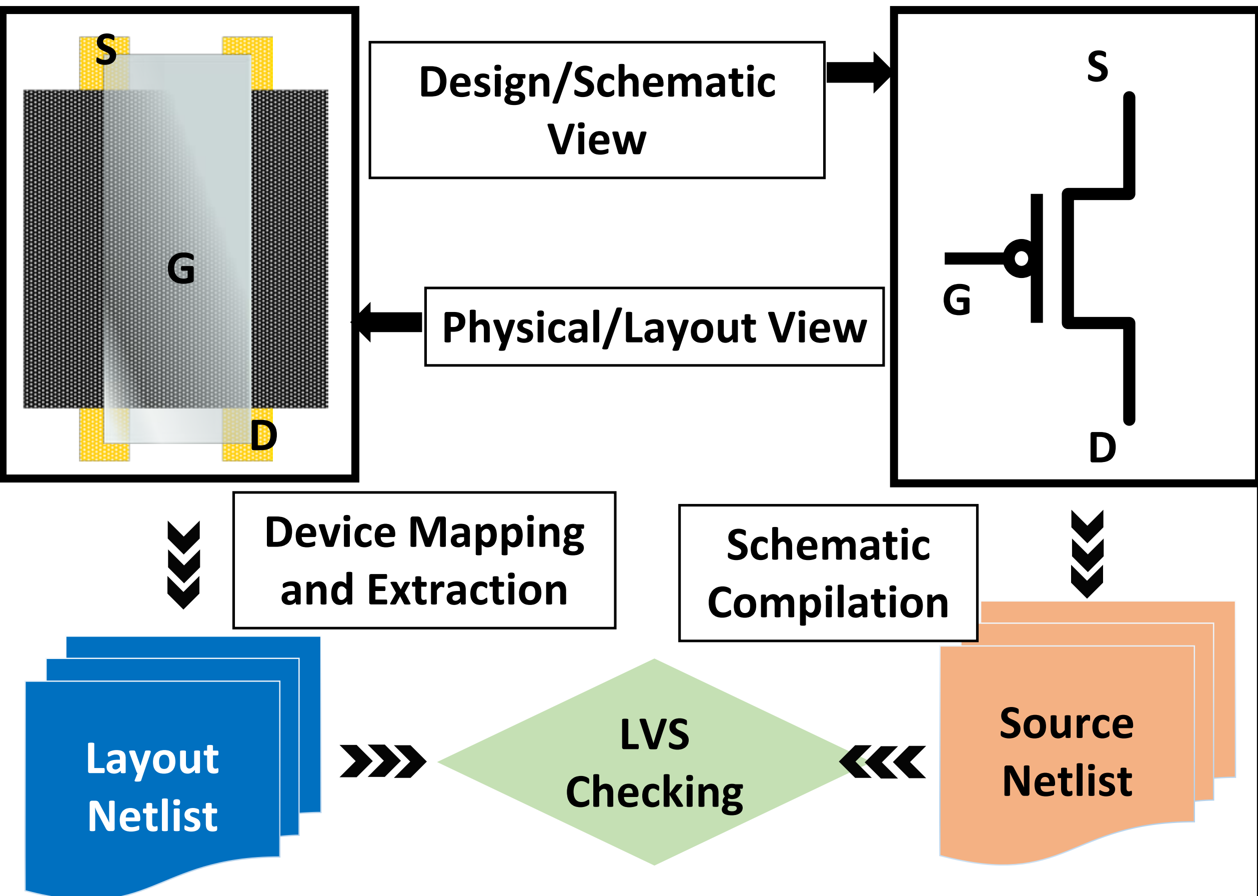
Layer Derivation of CNT-TFTS
Temp = CNT AND Gate
Channel = Temp NOT Metal1
SD = Metal2 AND CNT

Rule Checking Operators:
Enclosure, Spacing and Width



Once the critical regions, such as channel, gate and source/drain, are derived, it is straightforward to perform design checking.

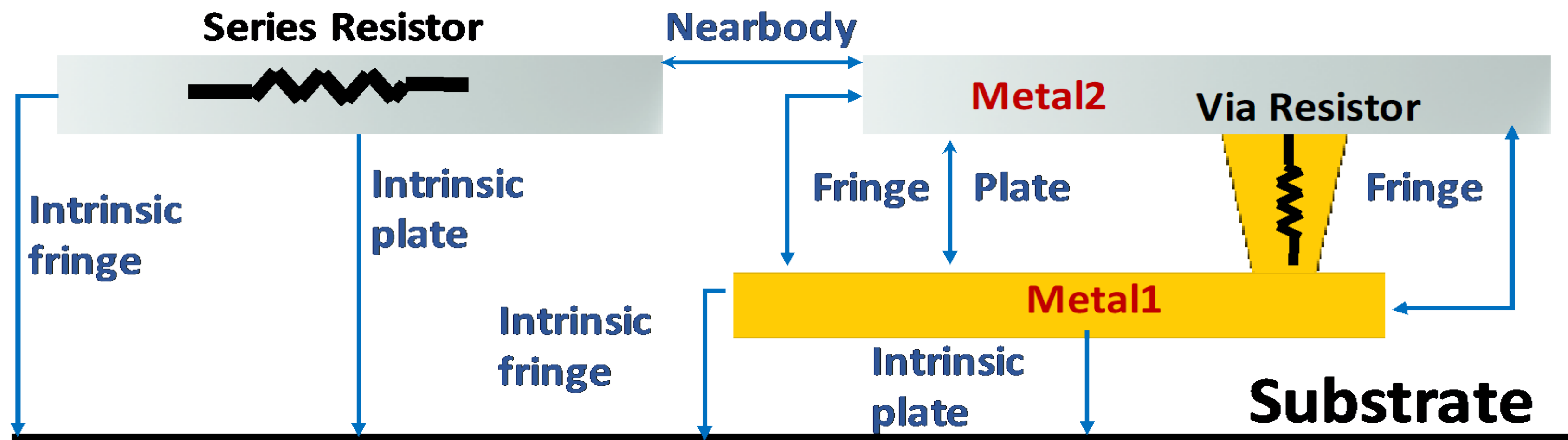
Device Recognition and Layout versus Schematic



Device Recognition (Layout ⇔ Netlist Mapping)
Gate ⇔ G
SD ⇔ S/D

1. With defined recognition rules, netlists are extracted from both the schematic and the layout.
2. Then, both netlists are converted into graphs and graph isomorphism is used to check their equivalence.

Parasitic Definition and Layout Parasitic Extraction



Parasitic Definition
Parasitic capacitor : intrinsic or coupling $C = C_{plate} * Area() + C_{fringe} * Perimeter()$
Parasitic resistor : conducting layers or vias $R = R_{Sheet} * Length()/Width()$

1. **Similar to device recognition, parasitic are extracted from the layout.**
2. **Post-simulation can be performed for more accurate results**

Parameterized Cell (P-Cell) for CNT Resistors

Apply To: only current | instance
Show: system ✓ user ✓ CDF

Browse | Reset Instance Labels Display

Property	Value	Display
Library Name	FHE-PDK-Lib	off
Cell Name	res_cnt	off
View Name	symbol	off
Instance Name	I2	value

Add | Delete | Modify

User Property	Master Value	Local Value	Display
interfaceLastCh.	1 15:00:21 2017		off

CDF Parameter of view: Use Tools Filter

Parameter	Value	Display
Length	10u M	
Width	4u M	off
Contact Width	2u M	off
Sheet Resistance	136.6K Ohms	off
Multiplier	1	off

OK | Cancel | Apply

Channel Width

Channel Length

Contact Width

Sheet Resistance

Note: All parameters not in the geometry space (ChL [10,100] um, ChW[4,200] um, CW[2,10] um) will cause an warning/error

CDF Parameter of view: Use Tools Filter

Parameter	Value
Length	10u M
Width	4u M
Sheet Resistance	136.6K Ohms
Multiplier	1

Channel Length=10um

CDF Parameter of view: Use Tools Filter

Parameter	Value
Length	20u M
Width	4u M
Sheet Resistance	126.5K Ohms
Multiplier	1

Channel Length=20um

CDF Parameter of view: Use Tools Filter

Parameter	Value
Length	50u M
Width	4u M
Sheet Resistance	135.2K Ohms
Multiplier	1

Channel Length=50um

CDF Parameter of view: Use Tools Filter

Parameter	Value
Length	100u M
Width	4u M
Sheet Resistance	103.1K Ohms
Multiplier	1

Channel Length=100um

Sheet Resistance will automatically change once changing the parameters based on the measurements and linear interpolation in the geometry space (ChL [10,100] um, ChW[4,200] um, CW[2,10] um)

Conclusion and Future Outlook

- **FHE is emerging for sensing and computing virtually anywhere**
  - **US FHE-MII (*NextFlex*) established in 2015 to promote this field by collaboration (government/industry/academia)**
  - **We aim to bring machine intelligence to billions of intelligent IoT nodes**
- **Solutions to solve circuit design and verification challenges**
  - **Compatible with ink-jet printing and roll-to-roll imprinting for mass production**
  - ***Pseudo-CMOS* circuits demonstrated for RFID/NFC/Healthcare/Energy**
  - **LSPC (IMEC ISSCC'17) using *Pseudo-CMOS* and > 2,000 TFTs becomes reality**
- **Process design kit for flexible hybrid electronics (FHE-PDK)**
  - **Spice models for printed active and passive components**
  - **Design rules and checking (DRC/LVS/LPE) for printed TFT circuits**
  - **Integrated environment for printed circuit and silicon chip co-development**