From Silicon to Printed Electronics: A Coherent Modeling and Design Flow Approach Based on Printed Electrolyte Gated FETs

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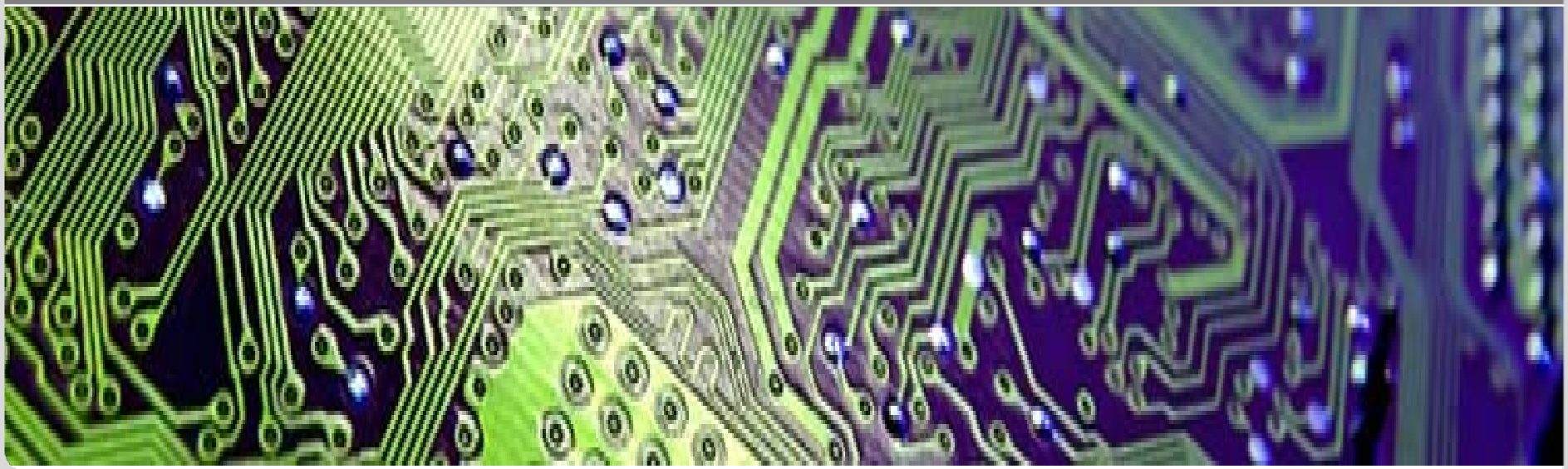


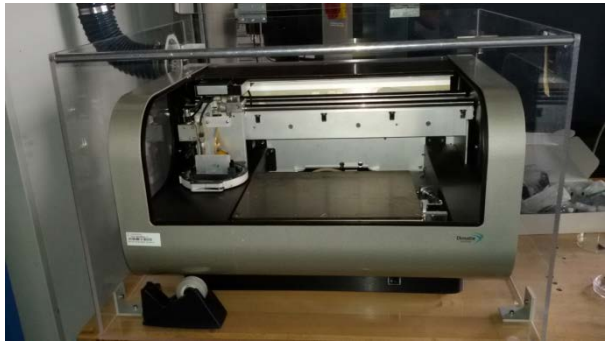
Outline

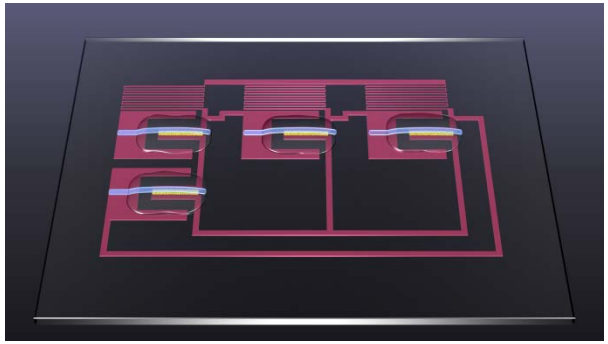
- Printed/organic electronics
- Electrolyte-gated transistors (EGFETs) based on oxide semiconductors
- Ring oscillator structure
- EGFET modelling
- Process Design Kit (PDK)
- Future Applications
- Summary

Overview: Printed electronics

- Devices are processed from solutions (inks).
- Circuits or electrical components can be printed on rigid or flexible substrates.
- Fabrication costs are potentially low compared to silicon based devices.

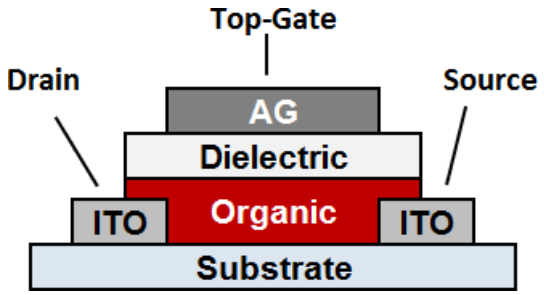
Ink preparation → Printing → Device characterization





Organic field-effect transistors

- Low mobility organic, p-type semiconductors are used as channel material.
- Inefficient gating results in applications with high supply voltage requirements (> 10 V).



Organic field-effect transistor (OFET)

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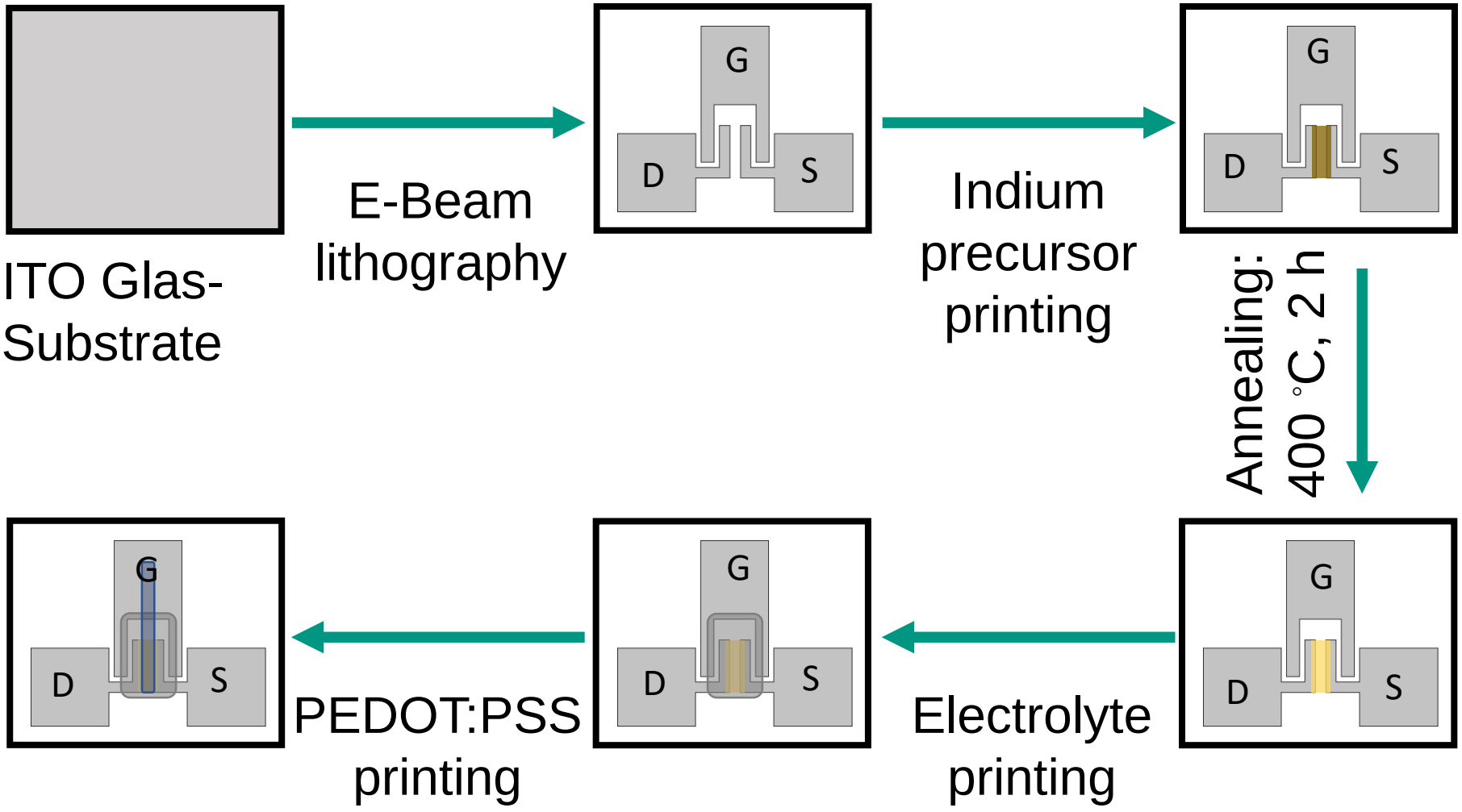
Electrolyte-gated transistors

- The channel is replaced with indium oxide (In_2O_3), which has high intrinsic mobility.
- Electrolyte-gating provides high gate-capacitance.
  - Therefore, the supply voltage is reduced to values ~ 1.0 V.

Organic field-effect transistor (OFET)

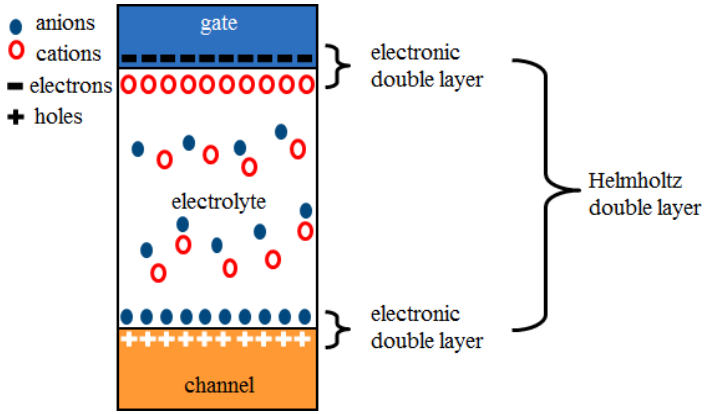
Electrolyte-gated field effect transistor (EGFET)

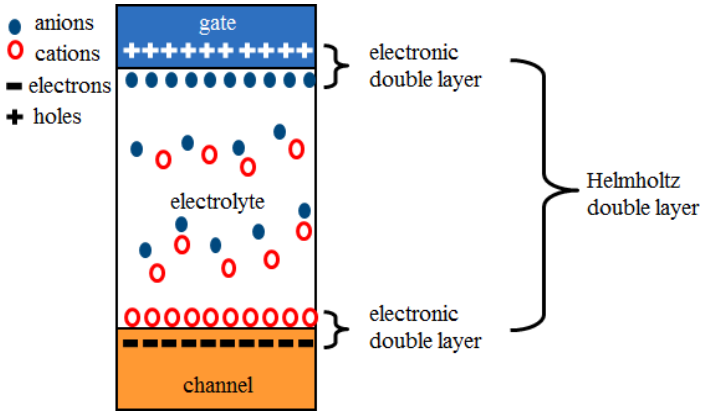
EGFET fabrication



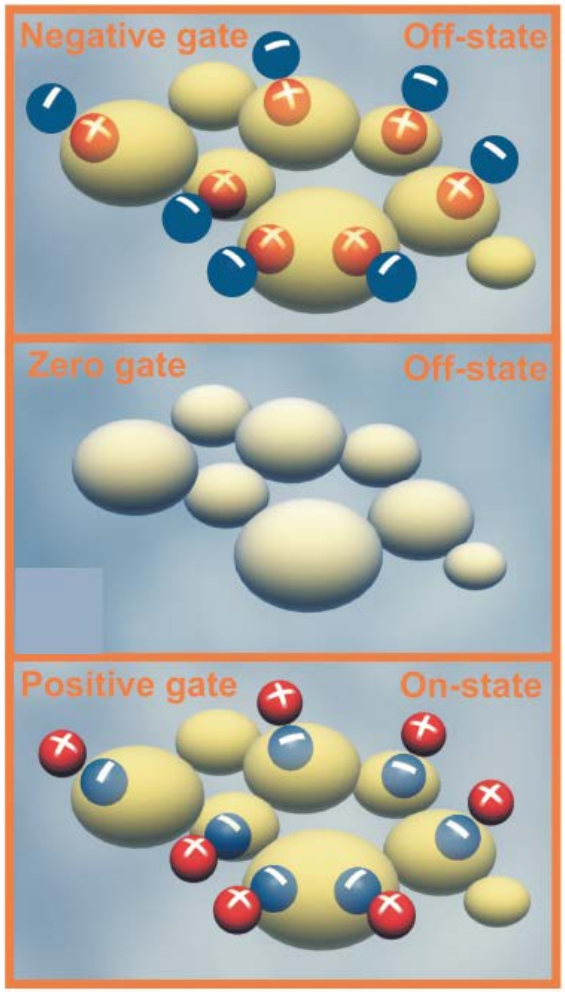
The Helmholtz double layer

- Ions of opposite polarity as the gate bias are attracted to the gate-electrolyte interface.
- Counter ions are aligning at the electrolyte-semiconductor interface.
  - Charge accumulation happens inside the channel.





Indium oxide as channel material



- At negative bias, holes are accumulated in the channel.
  - Holes are not mobile since indium oxide is an electron conductor.
- At zero gate bias, non charges are present inside the channel.
- At positive gate bias, electron accumulate inside the channel.
  - Current is able to flow between the drain and source electrodes.

[S. Dasgupta et al., ACS Nano, 10.1021/nn202992v]

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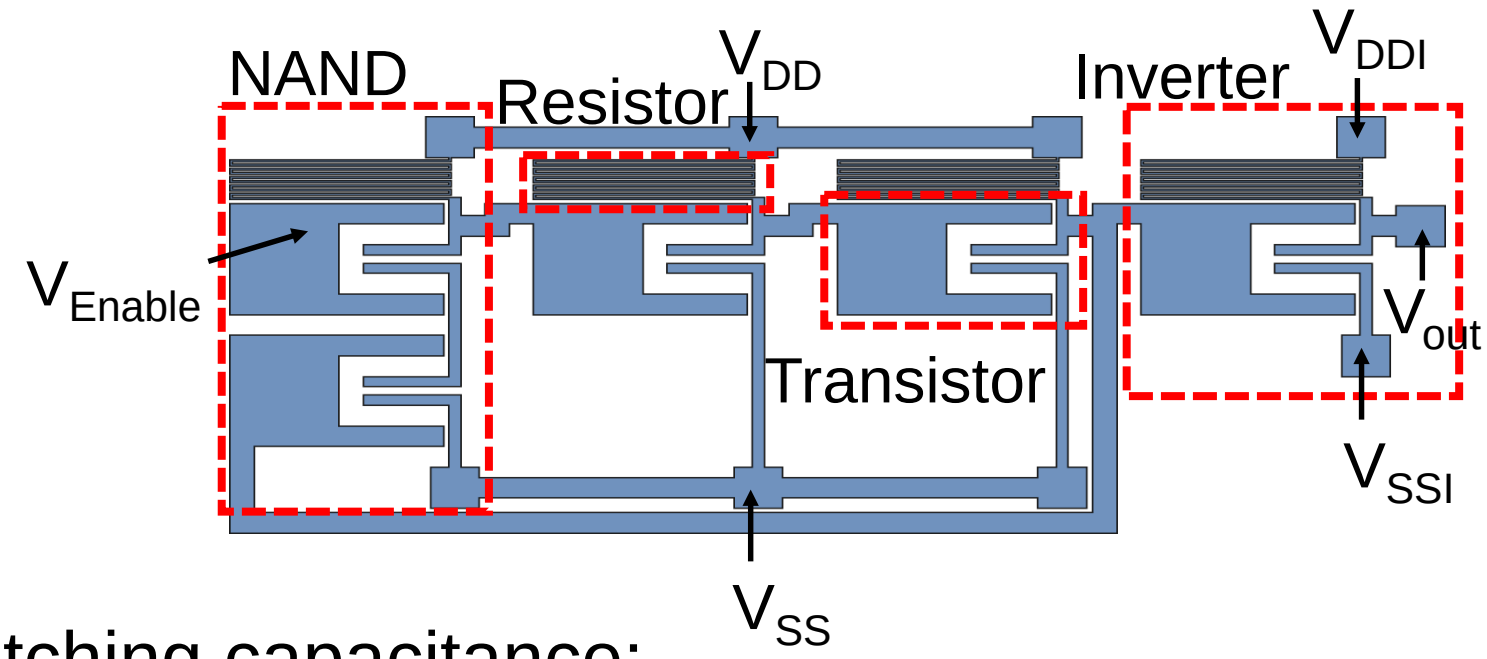
Ring oscillator characterization



Switching capacitance:

$$C_{sw} = \frac{I_{DDA} - I_{DDQ}}{(2\alpha+1)V_{DD}f}, \text{ with } f = \text{frequency}$$

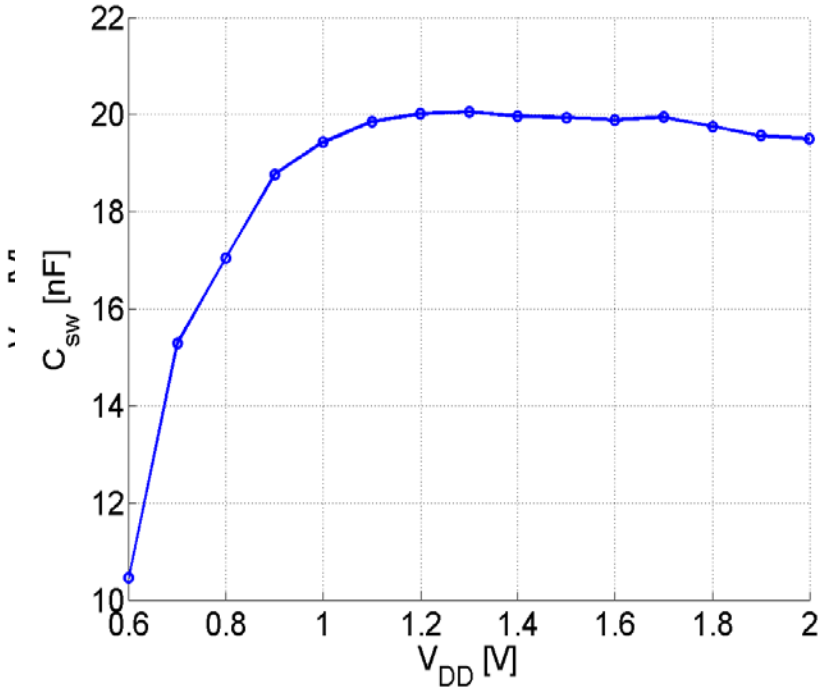
Switching resistance:

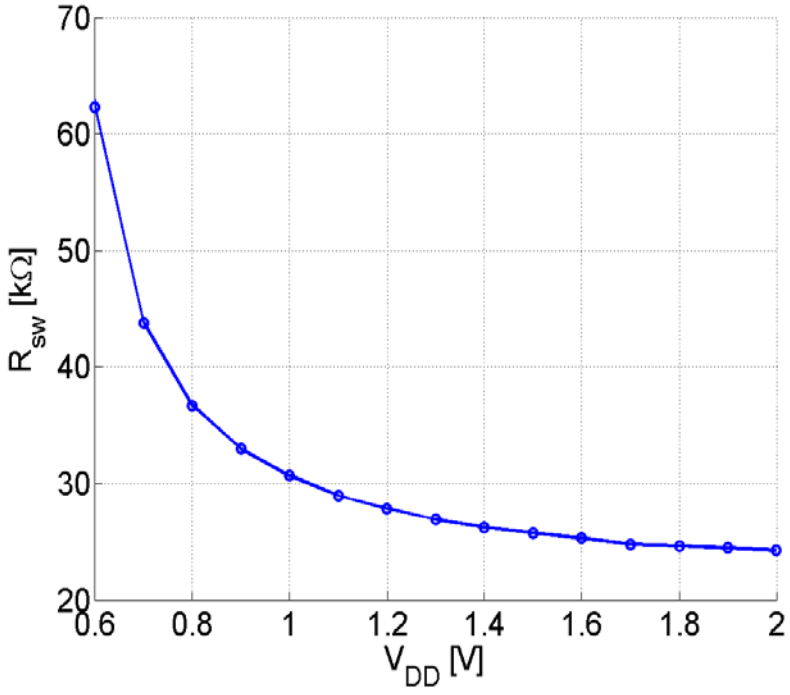
$$R_{sw} = \frac{\tau_p}{C_{sw}}, \text{ with } \tau_p = \frac{1}{2(2\alpha+1)f}$$

[G. C. Marques et al., Applied Physics Letters, 111(10), 102103, 2017]

Experimental ring oscillator results

- The switching capacitance saturates at ~ 20 nF.
- The switching resistance saturates at ~ 25 kΩ.





[G. C. Marques et al., Applied Physics Letters, 111(10), 102103, 2017]

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EGFET Curtice based model

Below-Threshold

Modeled with the subthreshold equation:

$$I_{DS} = I_s e^{\frac{V_{GS}-V_{th}}{nV_{thermal}}} \tanh(\alpha V_{DS})(1+\lambda V_{DS})$$

Near-Threshold

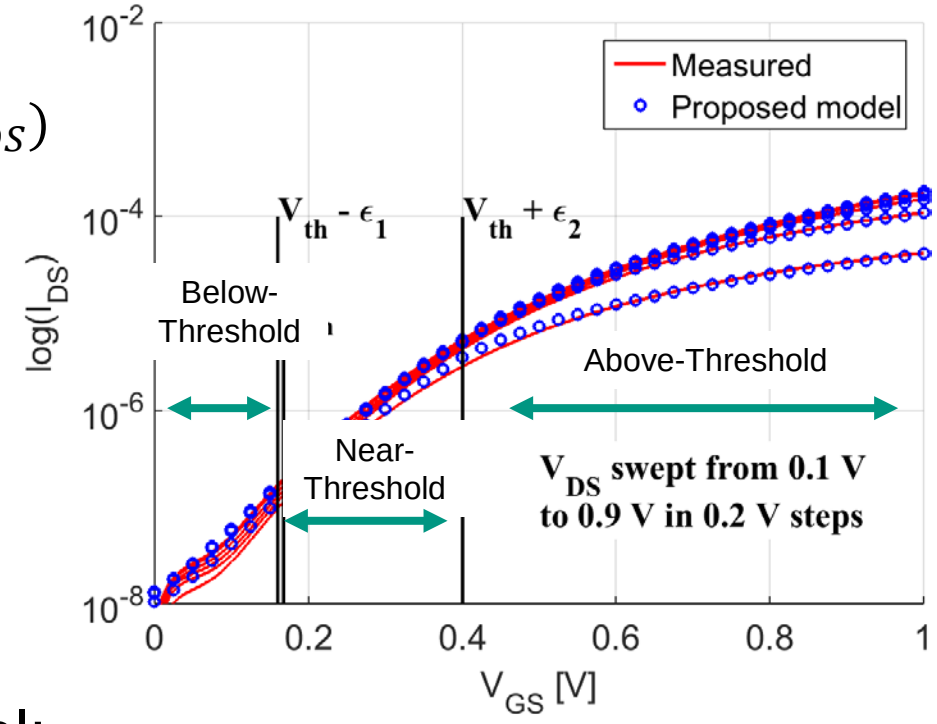
Modeled with a cubic interpolation:

$$I_{DS} = \left(aV_{GS}{}^3 + bV_{GS}{}^2 + cV_{GS} + d\right) \cdot \\ \cdot \tanh(\alpha V_{DS})(1+\lambda V_{DS})$$

Above-Threshold

Modeled with the Curtice model:

$$I_{DS} = \beta(V_{GS}-V_{th})^{\gamma}\tanh(\alpha V_{DS})(1+\lambda V_{DS})$$



[G. C. Marques et al., IEEE TED, 10.1109/TED.2016.2621777]

EKV based EGFET model

- Single equation for all operation regimes of transistor.
- Updated EGFET model for simulation of printed transistors and their process variations.

Drain Current Equation:

$$I_{DS} = I_o \left[ln\left(f_3 + e^{(v_p - v_s)/2}\right)^{\gamma} - ln\left(f_3 + e^{(v_p - v_d)/2}\right)^{\gamma} \right]$$

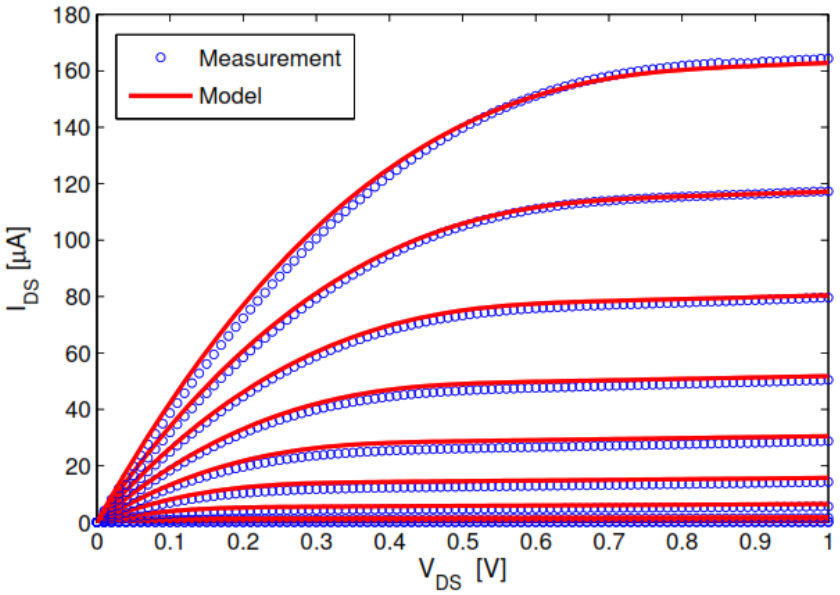
where,

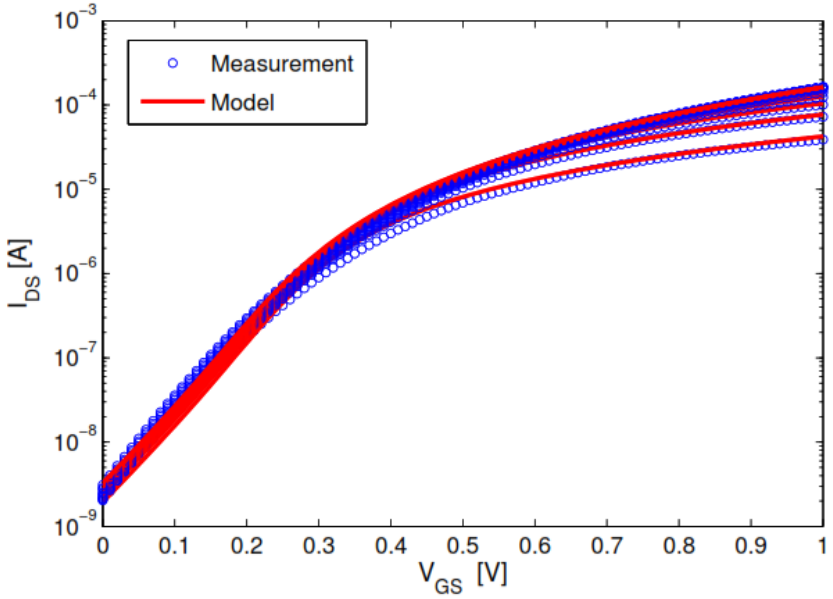
$$I_o = 2nf_1 \frac{W}{L} \emptyset_t^2 \qquad v_p \approx \frac{V_{GS} - (V_{TH} - f_4 V_{DS})}{\frac{n}{f_2}\emptyset_t} \emptyset_t^2$$

[F. Rasheed et al., IEEE TED, 10.1109/TED.2017.2786160]

EKV based EGFET model

- Model parameters contains empirical and fitting parameters to match measurement curve.
- It can be extended to model process variations in printed transistors.





[F. Rasheed et al., accepted by IEEE TED]

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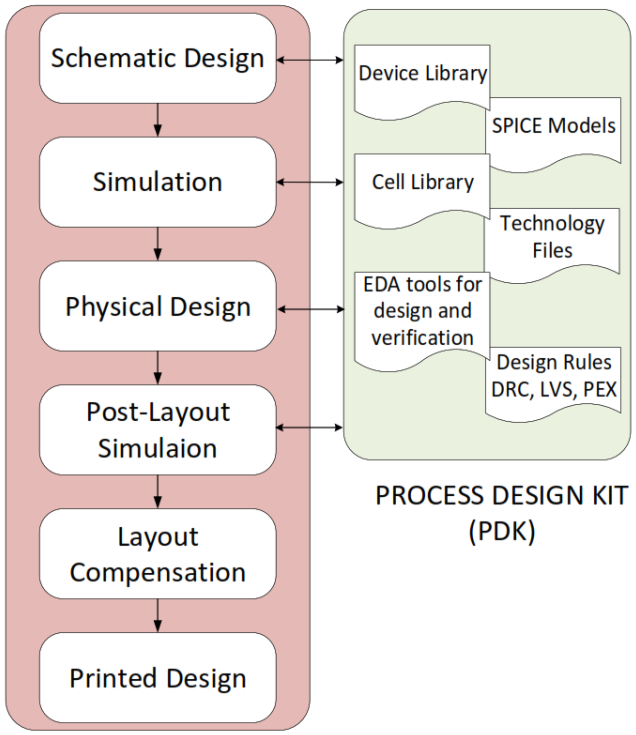
Process Design Kit (PDK)

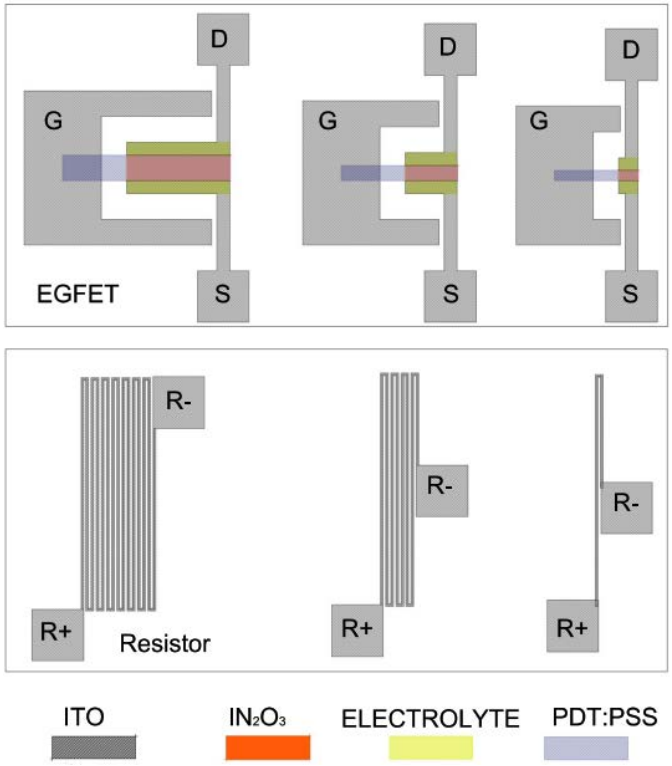
- In general PDK is comprised of two components group:
- Front-end components:
  - Devices symbol
  - Standard cells
  - Models
- Back-end components:
  - Technology and display files
  - Verification rules deck (DRC,LVS,PEX)
  - Parameterized cell (Pcell)



Printed electronics design flow including PDK

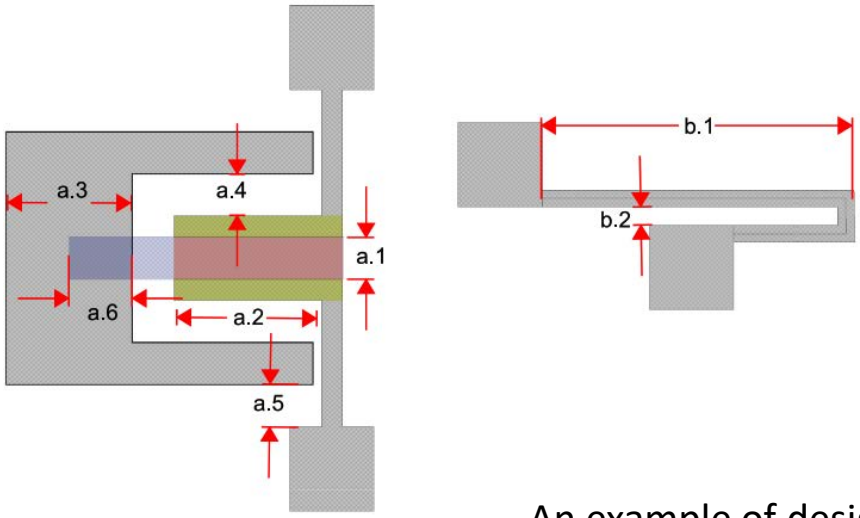
PDK – Parametrized Cell

- We have already developed in-house PDK for our process technology.
- N-type EGFET and resistor model as well as their Pcells are integrated in our design environment.



PDK – DRC/LVS

- DRC and LVS rules are also added for available layers.



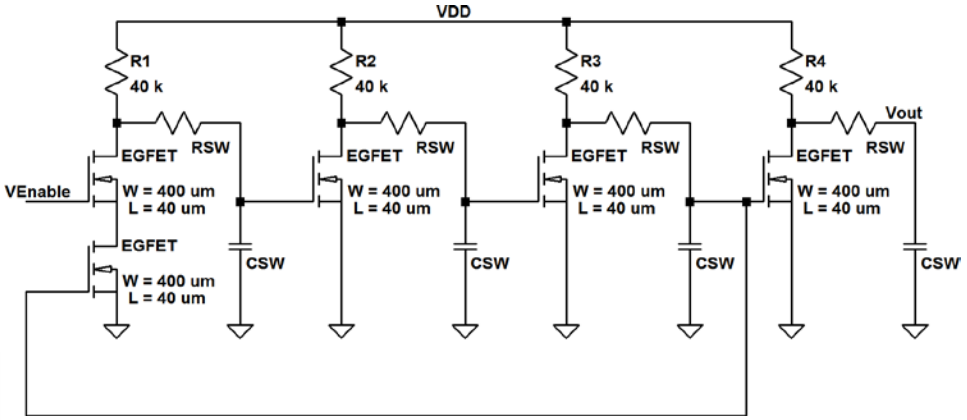
Design Rules	Comments
a.1	Channel length
a.2	Channel width
a.3	Gate electrode width
a.4	Separation between gate-electrode and electrolyte
a.5	Separation between gate-electrode and drain/source-electrode
a.6	Overlap of PEDOT:PSS and gate-electrode
b.1	Resistance strip length
b.2	Spacing between resistance strip

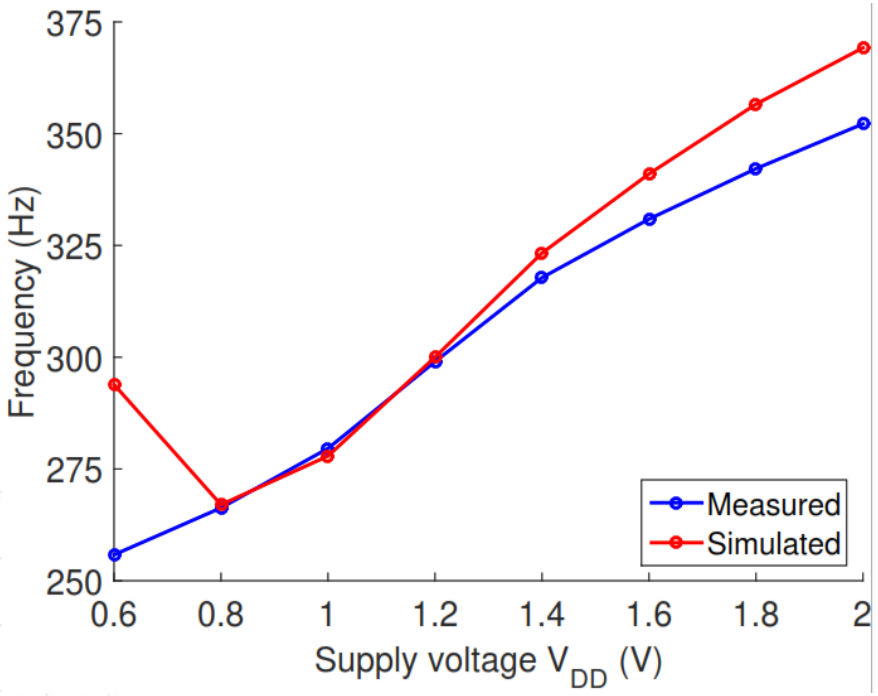
An example of design rules for our printed process

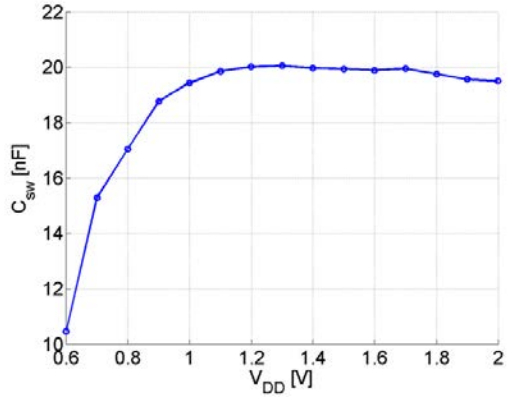
DRC = Design Rule Check
LVS= Layout versus Schematic

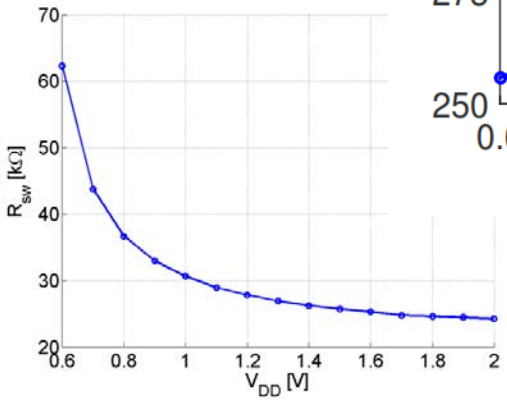
Hardware-software correlation

The measured and simulated frequency differ by 4.7% only.









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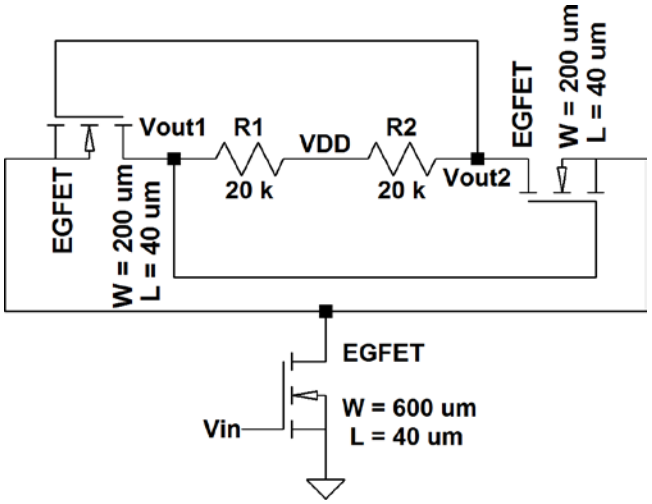
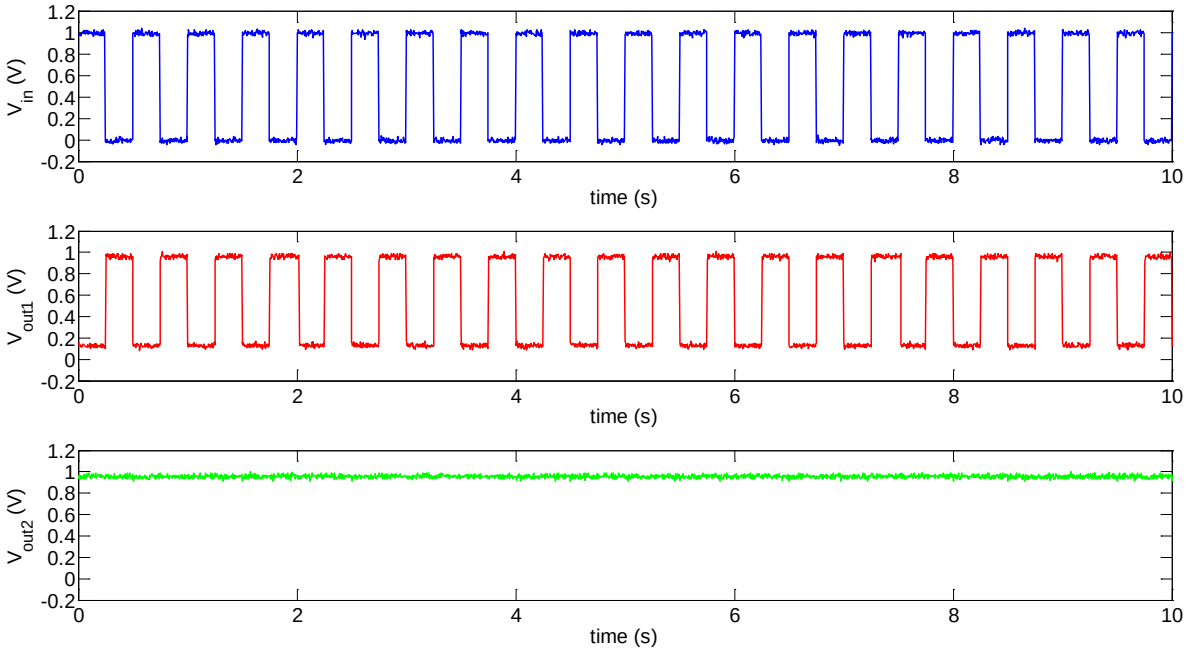
Physically Unclonable Functions (PUF) based on EGFETs

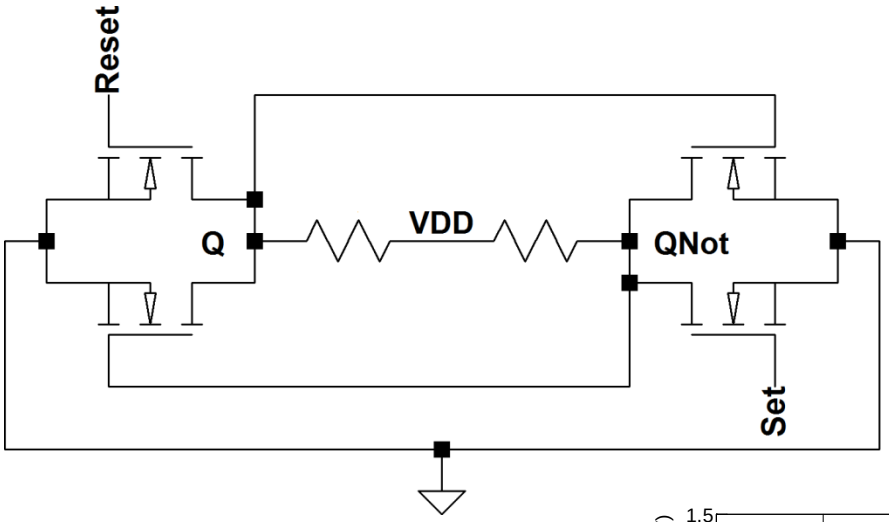
EGFETs are promising candidates for PUF based security applications due to the huge process variation.

Supply voltage: 1.0 V





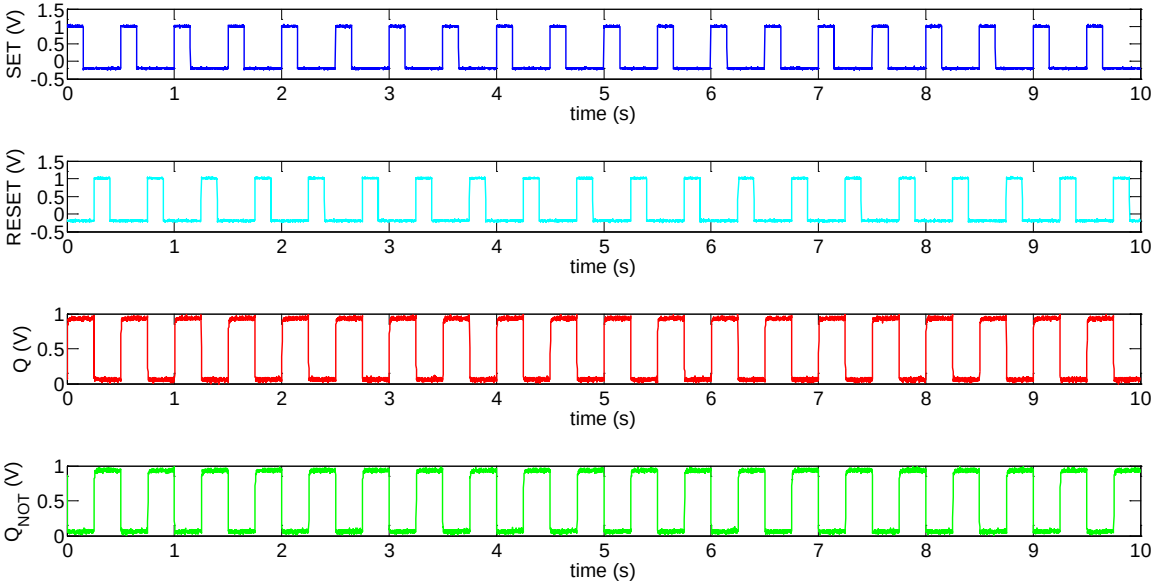
Latch based on EGFETs



Latches with EGFETs as main elements show promising results and opens the door for fil flop designs.

Supply voltage: 1.0 V

Resistors: 9.5 kΩ
EGFETs: W = 600 μm
L = 40 μm



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- Electrolyte-gating reduces the required supply voltages to values ~ 1.0 V.
- Oxide semiconductors yield high performance devices in the printed electronics domain.
- Process Design Kits (PDK) are useful tool for designers to develop new applications.
- Potential applications for EGFET technology was shown:
  - Ring oscillator
  - Physically Unclonable Function (PUF)
  - Latch

Thank you for your attention!!!

Acknowledgement

HELMHOLTZ GEMEINSCHAFT

MERAGEM