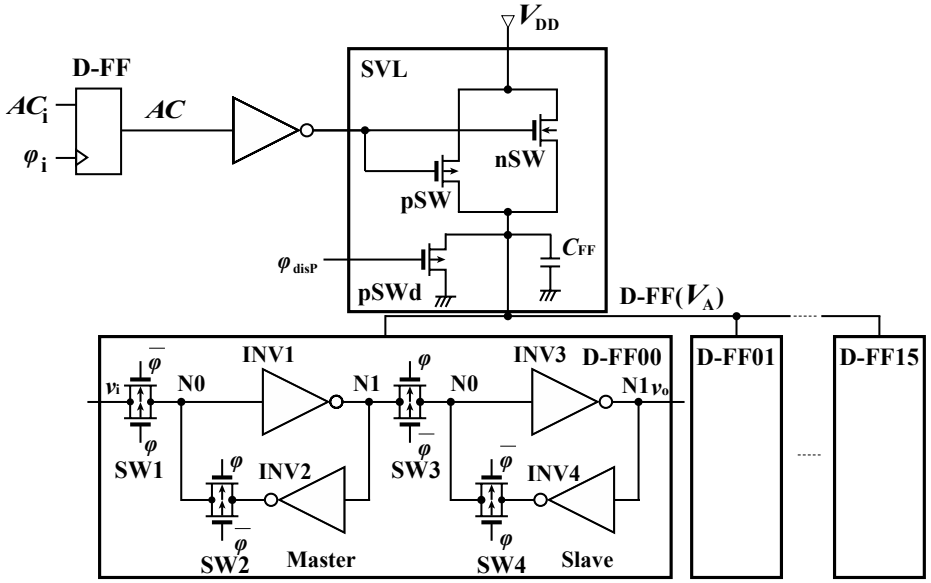
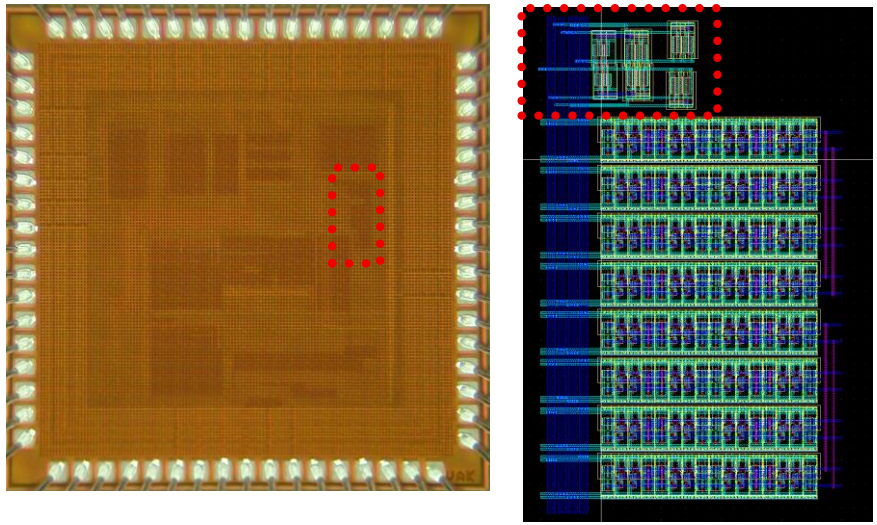
Low Standby Power CMOS Delay Flip-Flop with Data Retention Capability



SVL



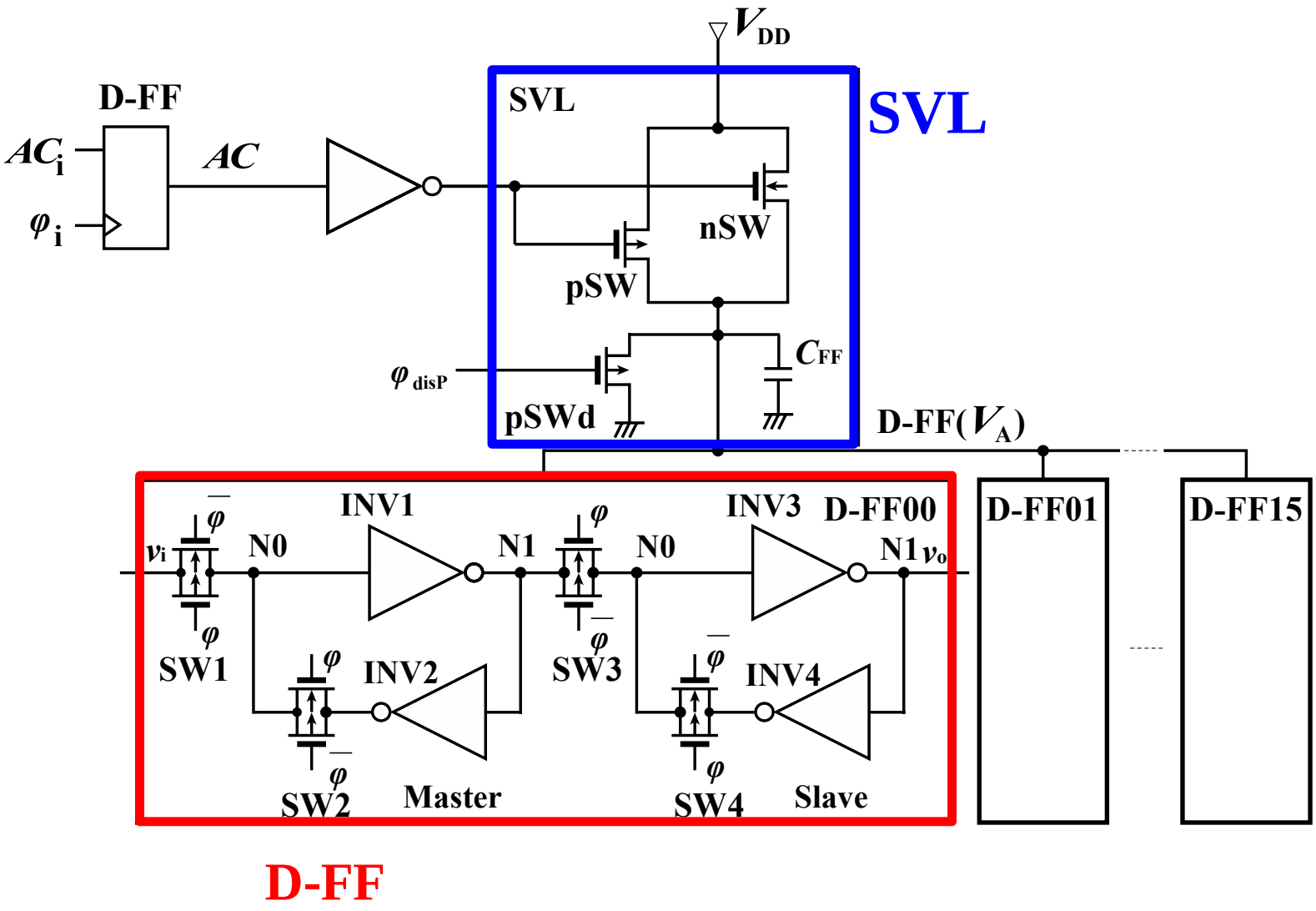
D-FF: 16-bit Master & Slave

SVL : 1 for 16-bit

Silicon Area: 937 μm^2

Area Overhead of SVL: 11.62%

Newly Developed D-FF



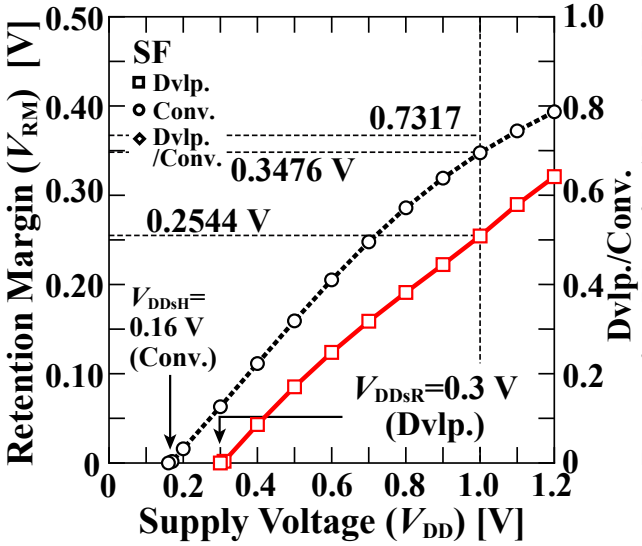
SVL:Self-controllable Voltage Level circuit

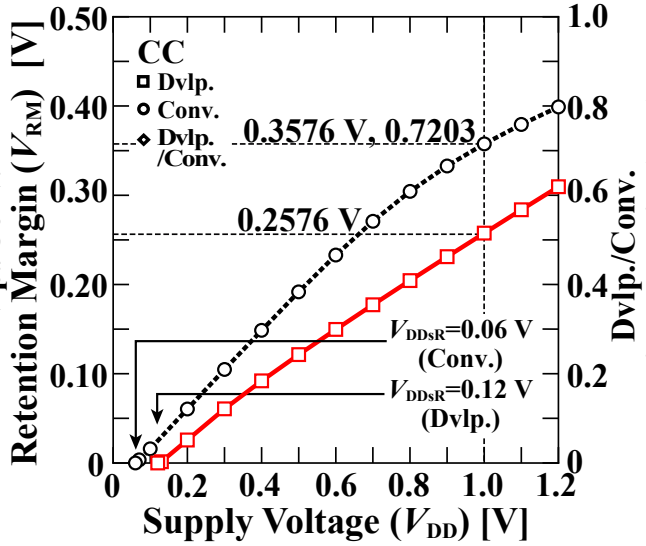
“Retention” Margin of D-FFs

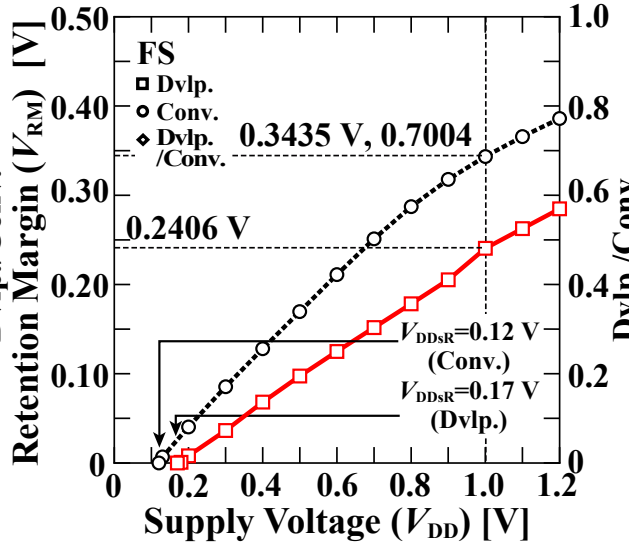
SF (+6σ)
V_{tn}= 0.275 V (+ 53 mV)
V_{tp}= -0.139 V (+103 mV)

CC (Ave.)
V_{tn}= 0.222 V (0)
V_{tp}= -0.242 V (0)

FS (-6σ)
V_{tn}= 0.142 V (-80 mV)
V_{tp}= -0.300 V (-58 mV)







V_{DD} = 1.0 V

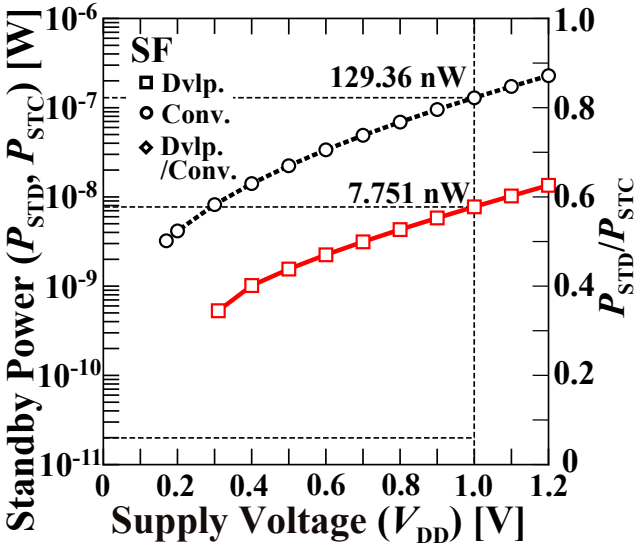
73.17 %	72.03 %	70.04 %

Minimum supply voltage of static “Retention” operation

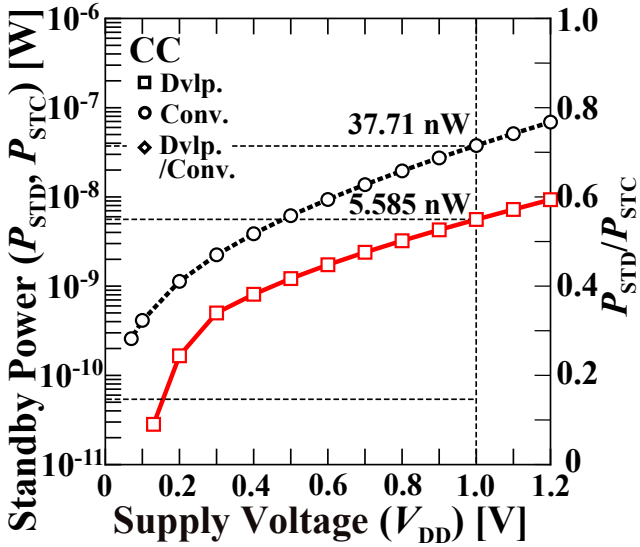
Conv. 0.16 V	Conv. 0.06 V	Conv. 0.12 V
Dvlp. 0.30 V	Dvlp. 0.08 V	Dvlp. 0.17 V

Standby Power of D-FFs

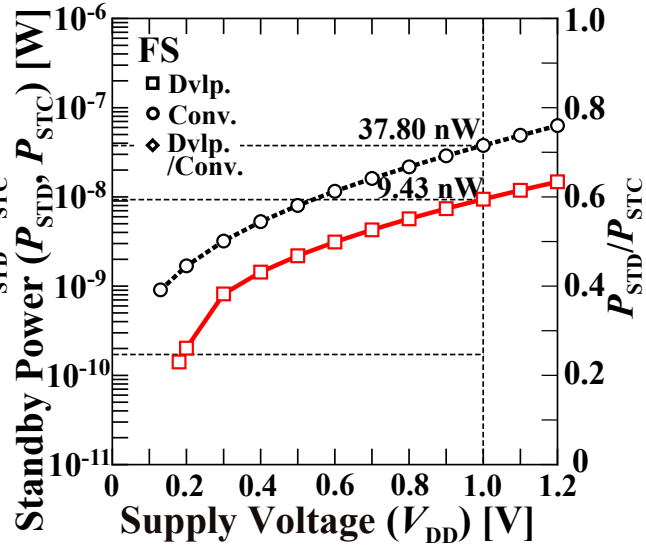
SF (+6σ)
V_{tn}= 0.275 V (+ 53 mV)
V_{tp}= -0.139 V (+103 mV)



CC (Ave.)
V_{tn}= 0.222 V (0)
V_{tp}= -0.242 V (0)



FS (-6σ)
V_{tn}= 0.142 V (-80 mV)
V_{tp}= -0.300 V (-58 mV)



V_{DD} = 1.0 V

5.992 %

14.81 %

24.95 %

Characteristics of D-FFs

	Min. Supply Volt. in "Retention" SF	Standby Power P_{st} V_{DD}=1.0V	Sillicon Area [μm^2]
Conv. D-FF	0.16 V	5.585 μW	858.28
Dvlp. D-FF	0.30 V (39.05%)	37.71 μW (14.81 %)	937.80 (111.62 %)

SVL :

- **Low Leakage while retaining DATA**
- **Small Area Overhead**