

FPGA Laboratory System supporting Power Measurement for Low-Power Digital Design

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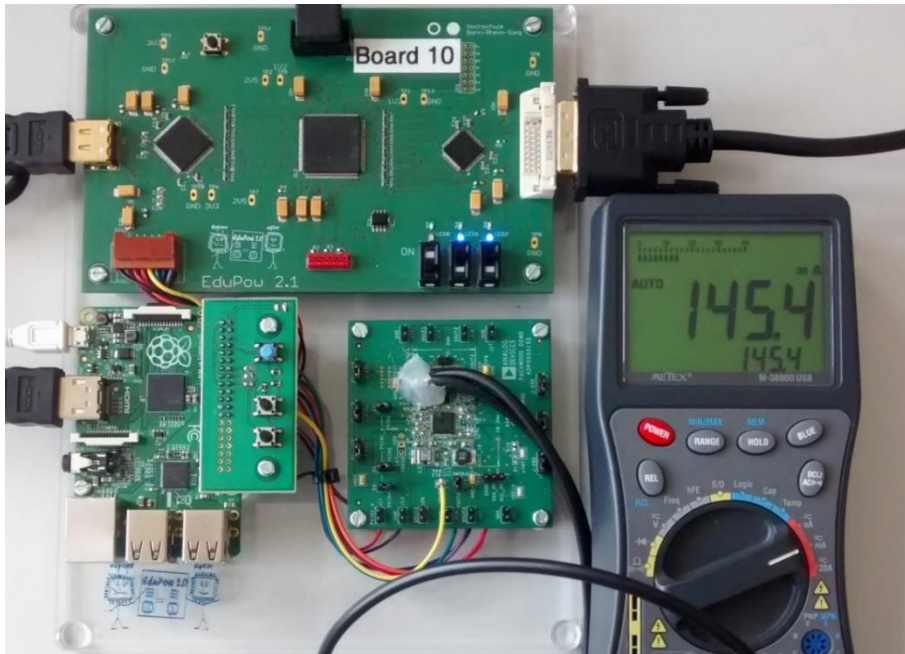
Bonn-Rhein-Sieg University

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FPGA Laboratory System

- The FPGA laboratory systems with Intel Cyclone IV respectively Cyclone V FPGAs are unique in offering:
 - HDMI input and output
 - Power measurement
 - Comparison of two different CMOS technologies
 - Available as a remote lab

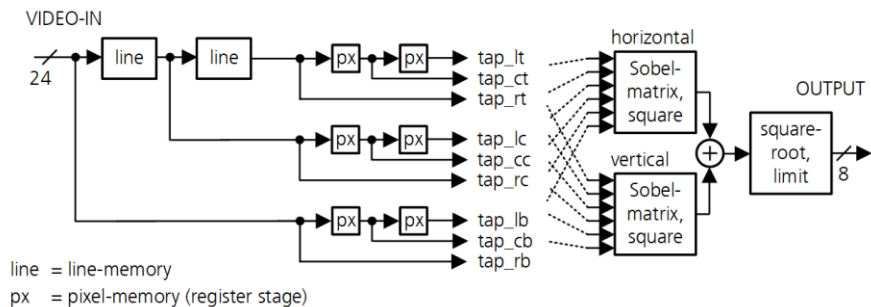


- Various design experiments possible, e.g.
 - CMOS technology
 - Temperature
 - Lane Detection

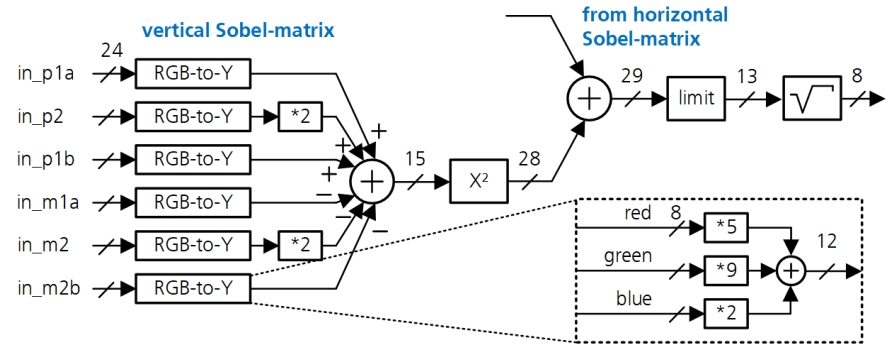
Design Experiment “Lane Detection”

- Original algorithm for lane detection:
 - 24-bit memory
 - 12 x RGB-to-Y

Block Diagram for Lane Detection

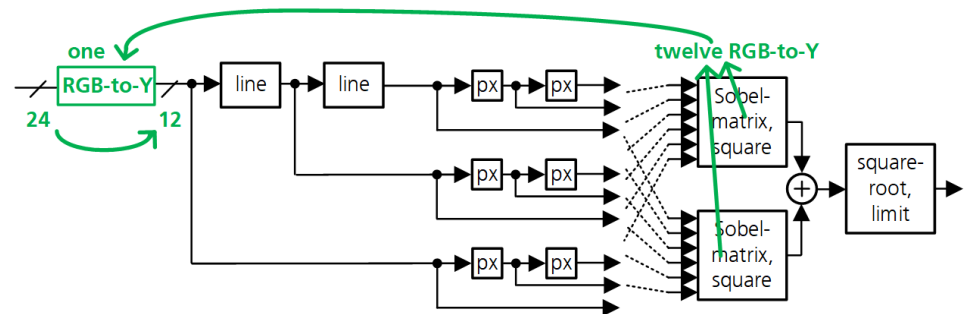


Block Diagram for Sobel Filter



- First optimization of lane detection algorithm:
 - Shifting luminance conversion before line-memory
 - 1 x RGB-to-Y
 - 12-bit memory

Optimize Position of Luminance Conversion



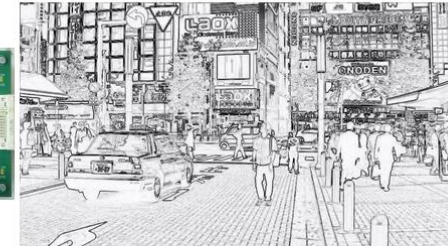
Original Algorithm vs. Optimized Algorithm

- Original algorithm for lane detection
 - 41.30 mA core current
 - 49.56 mW core power

FPGA Core Current:

41.3 mA

(Core Supply Voltage is 1.2 V)



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FPGA Core Current:

30.11 mA

(Core Supply Voltage is 1.2 V)

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- Optimized algorithm for lane detection
 - 30.11 mA core current
 - 36.13 mW core power
 - 27 % power saving
 - Identical output image



Power measurement enables understanding of circuit design