Design of Gate-Leakage-Based Timer Using an Amplifier-Less Replica-Bias Switching Technique in 55-nm DDC CMOS

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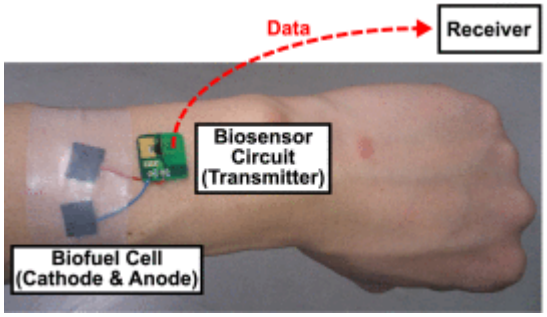
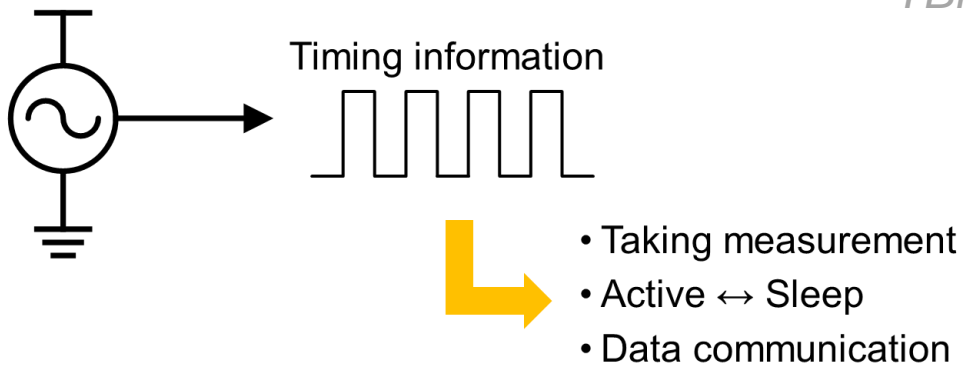
Motivation of This Work

- Sensor systems for biomedical applications
  - Energy harvesting
    - ➢ Solar, thermoelectric, piezoelectric
  - Energy from biological systems
    - ➢ Biofuel Cells



A. Kobayashi, et al., *TBioCAS* 2017.

- Timer circuit

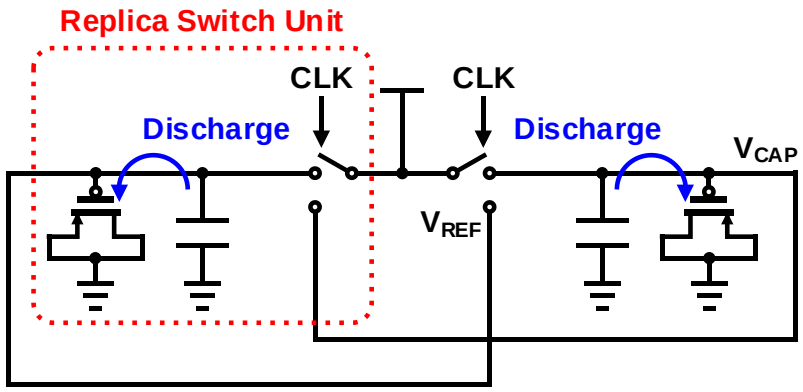


- Technical challenge in timer circuit
  - –Strict frequency stability in the deep subthreshold region

Overview of This Work

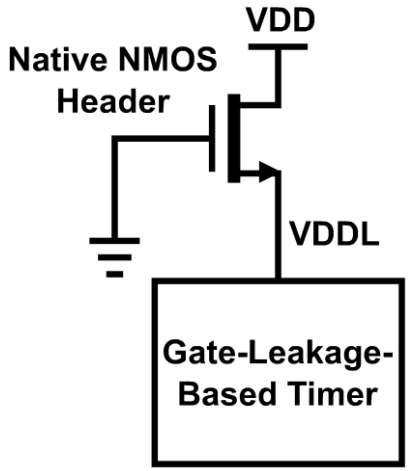
Objective of this work and main techniques

- Gate-leakage-based timer that can achieve efficient operation in the deep subthreshold region



Amplifier-Less Replica-Bias Switching Technique*

- Frequency stability
- Low voltage operation



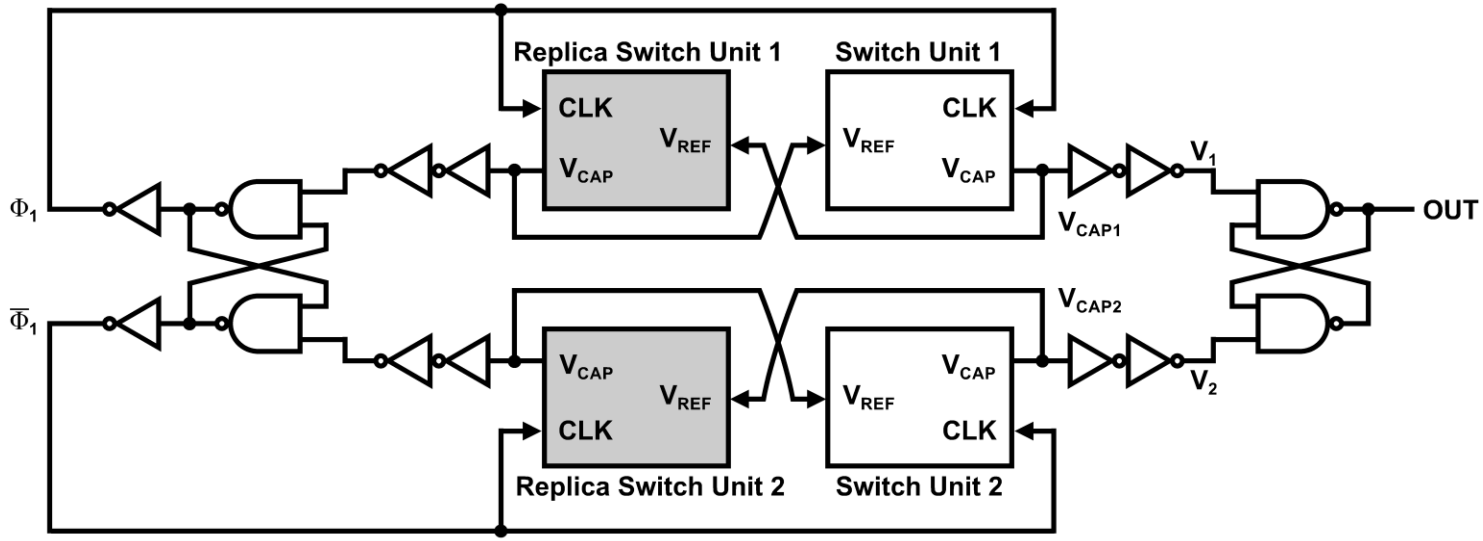
Native NMOS Header*

- Low supply sensitivity

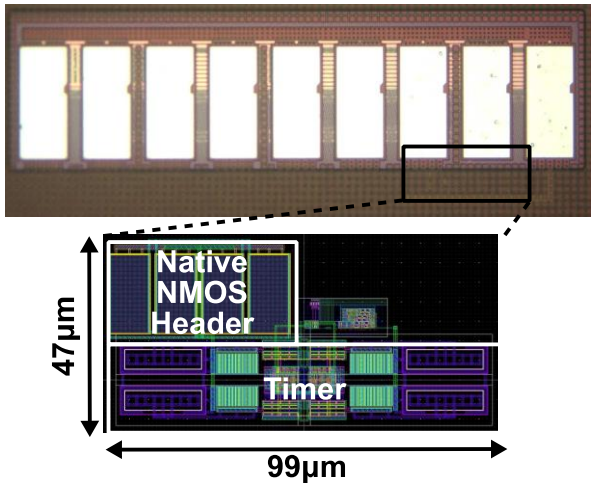
*A. Kobayashi et al., *CICC* 2018

Proposed Gate-Leakage-Based Timer

- Amplifier-less replica-bias switching technique with logic circuits



- Test chip
  - 55-nm DDC CMOS



Performance Summary

- Improvements in the low supply voltage performance

	This Work	[4] CICC 2007	[5] JSSC 2013	[6] JSSC 2016
Technology (nm)	**55 (DDC)**	130	130	65
Architecture	**Amplifier-Less Replica-Bias Switching**	Single-Stage Topology	Multi-Stage Topology	Capacitive Discharging
Supply Voltage (V)	**0.35**	0.45	0.7	0.5
Power (nW)	**10**	0.12	0.66	0.044
Frequency (Hz)	**330 (423[a])**	0.09	5	2.8
Energy Efficiency (pJ/cycle)	**32 (25[a])**	1333	132	15.8
Temp. Sensitivity (ppm/°C)	**1200**	1600	31	1260
Temp. Range (°C)	**-20 to 80**	0 to 80	-20 to 60	-40 to 60
Supply Sensitivity (ppm/mV)	**2310 (340[b])**	1500	N/A	1600
Supply Voltage Range (V)	**0.25 - 0.5 (0.3 - 0.5[b])**	0.3 - 0.5	N/A	0.48 - 0.52
Allan Deviation Floor (ppm)	**200**	N/A	N/A	500
Area (mm^2)	**0.0022 (0.0034[b])**	0.00048	0.015	0.026

A. Kobayashi et al., *CICC* 2018

[a.] VNW = 250 mV
[b.] w/ Native NMOS Header

Acknowledgments

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