A Low-Voltage Low-Power Multi-Channel Neural Interface IC Using Level-Shifted Feedback Technology

ASP-DAC 2019

University Design Contest

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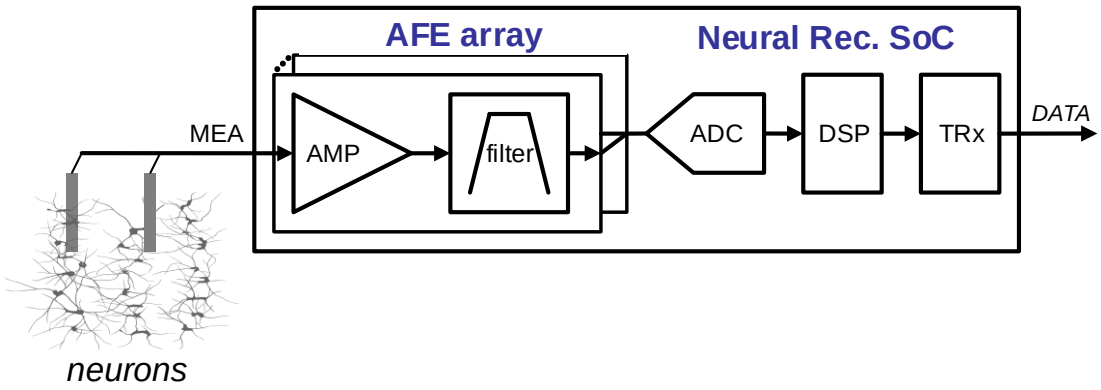
Background

- State-of-the-art neural recording SoCs feature:
  - Analog frontend with low noise and low distortion
  - Thousands of recording channels
  - Usually wireless/battery powered
- **Low voltage design is attractive!!!**



Level Shifted Feedback (LSFB)

- Traditional CCIA

$$V_{ip} \approx \overline{V_{on}} \approx 0.5V_{DD}$$

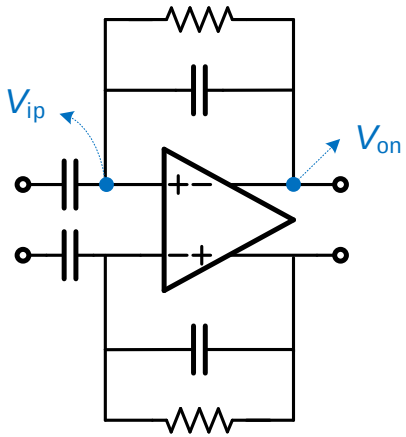
$$V_{DD} > 2\left(V_{\mathrm{gs1}} + V_{ds0}\right)$$

- CCIA with LSFB

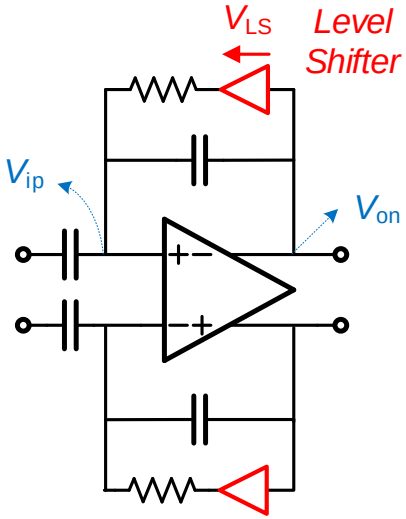
$$V_{ip} \approx \overline{V_{on} - V_{LS}} \approx 0.5V_{DD} - V_{LS}$$

$$V_{DD} > 2\left(V_{gs1} + V_{ds0} - V_{LS}\right)$$

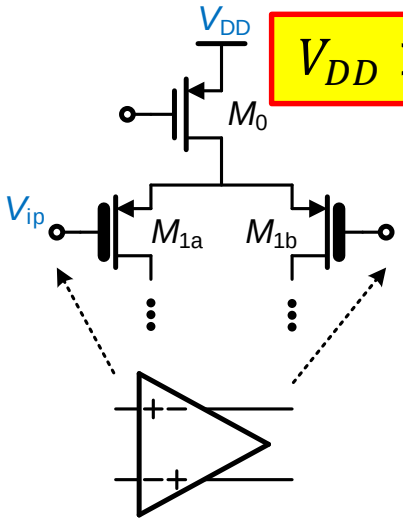
Lower supply voltage!!!



Traditional CCIA



CCIA with LSFB



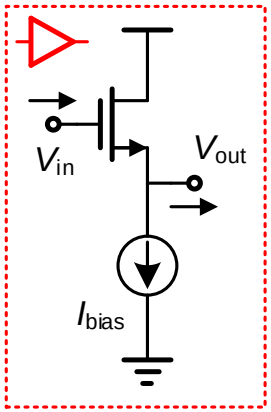
$$V_{DD} > V_{ip} + V_{gs1} + V_{ds0}$$

OTA in CCIA

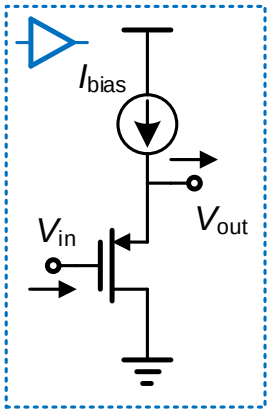
*Assuming output CM voltage is set to $0.5V_{DD}$ to maximize output swing.

Implementation

- LNA
  - Low power, low noise
  - Telescope OTA with current reusing
- PGA
  - Low power, high swing
  - 2-stage OTA

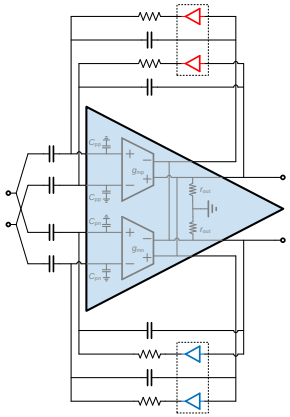


NMOS level shifter

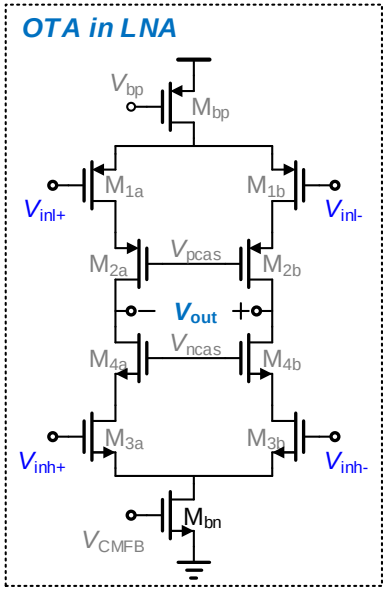


PMOS level shifter

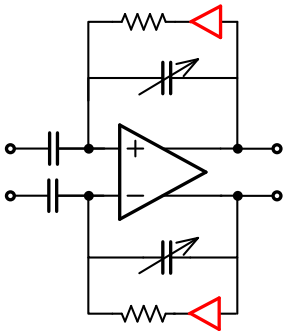
LNA



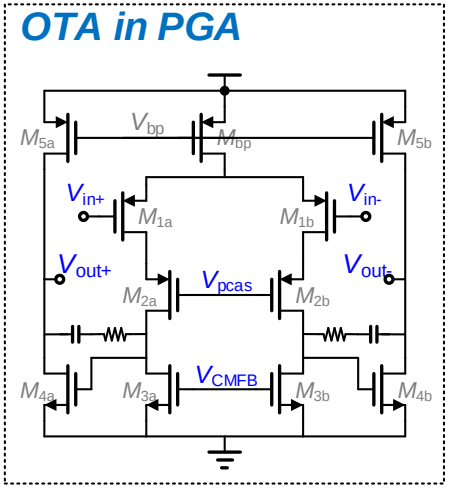
OTA in LNA



PGA



OTA in PGA



Measurement Results

	JSSC'12	TCASI'13	TbioCAS'16	This Work
Technology	65nm	180nm	180nm	65nm
Supply (V)	0.5	1	1.8	0.6
Area/ch(mm^2)	0.013	NA	0.03	0.032
Power/ch (uW)	5	11.6	9.1	1.07
GAIN (dB)	NA	NA	52-66	50.75
BW(Hz)	10k	5.1k	10k	10k
IRN (uV)	4.9	4.0	4.07	5.18
NEF/PEF	5.99/17.96	1.9/3.6	3.51/22.2	2.91/5.19