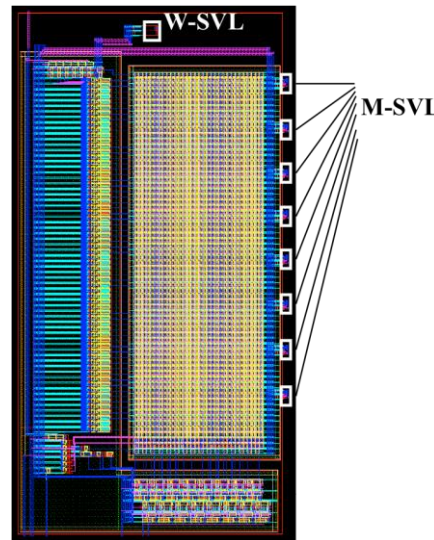
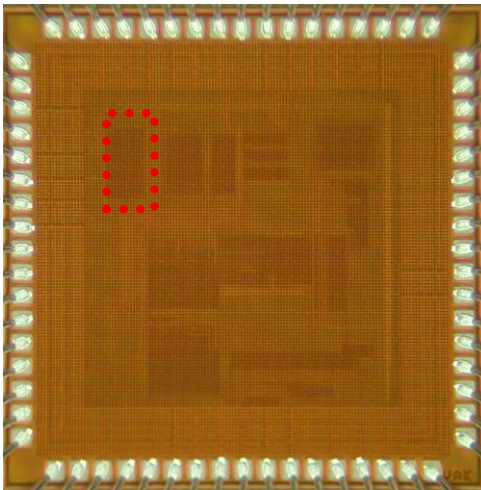
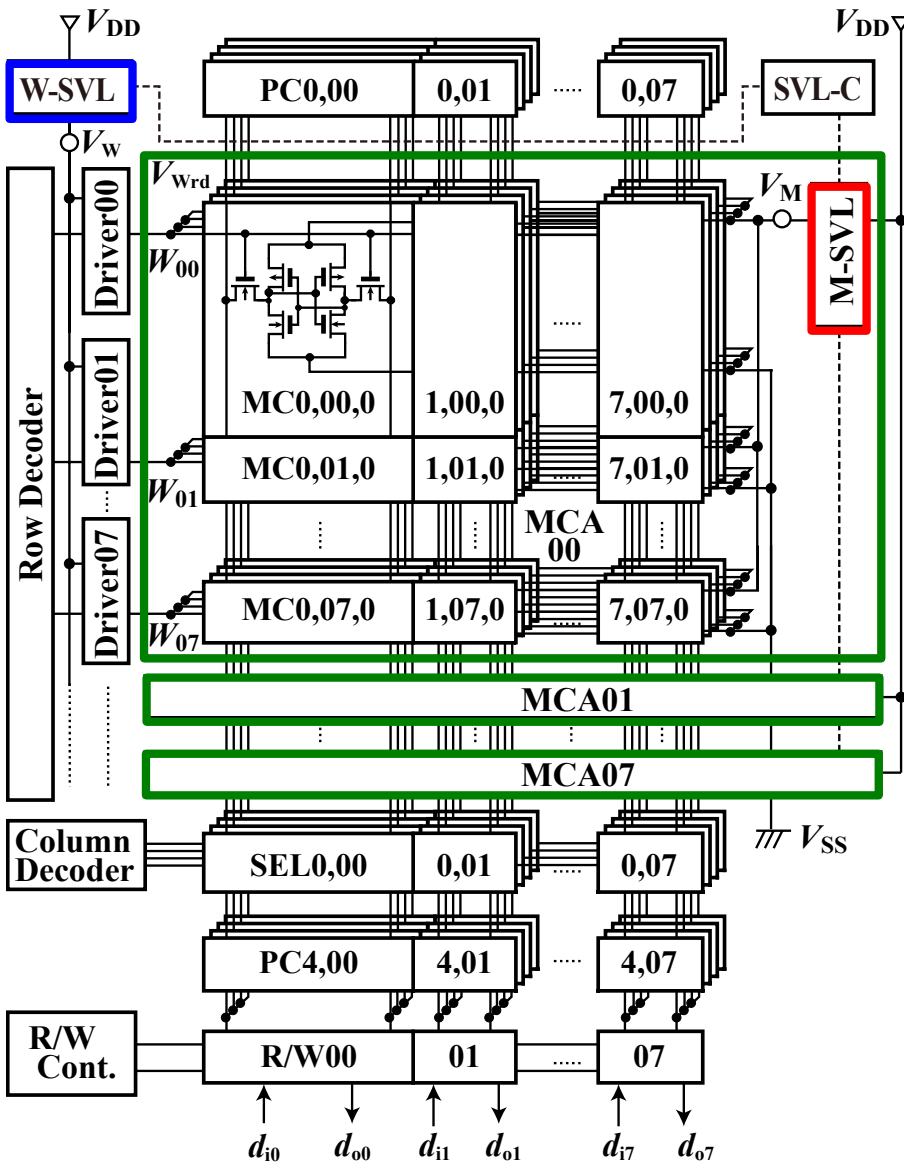
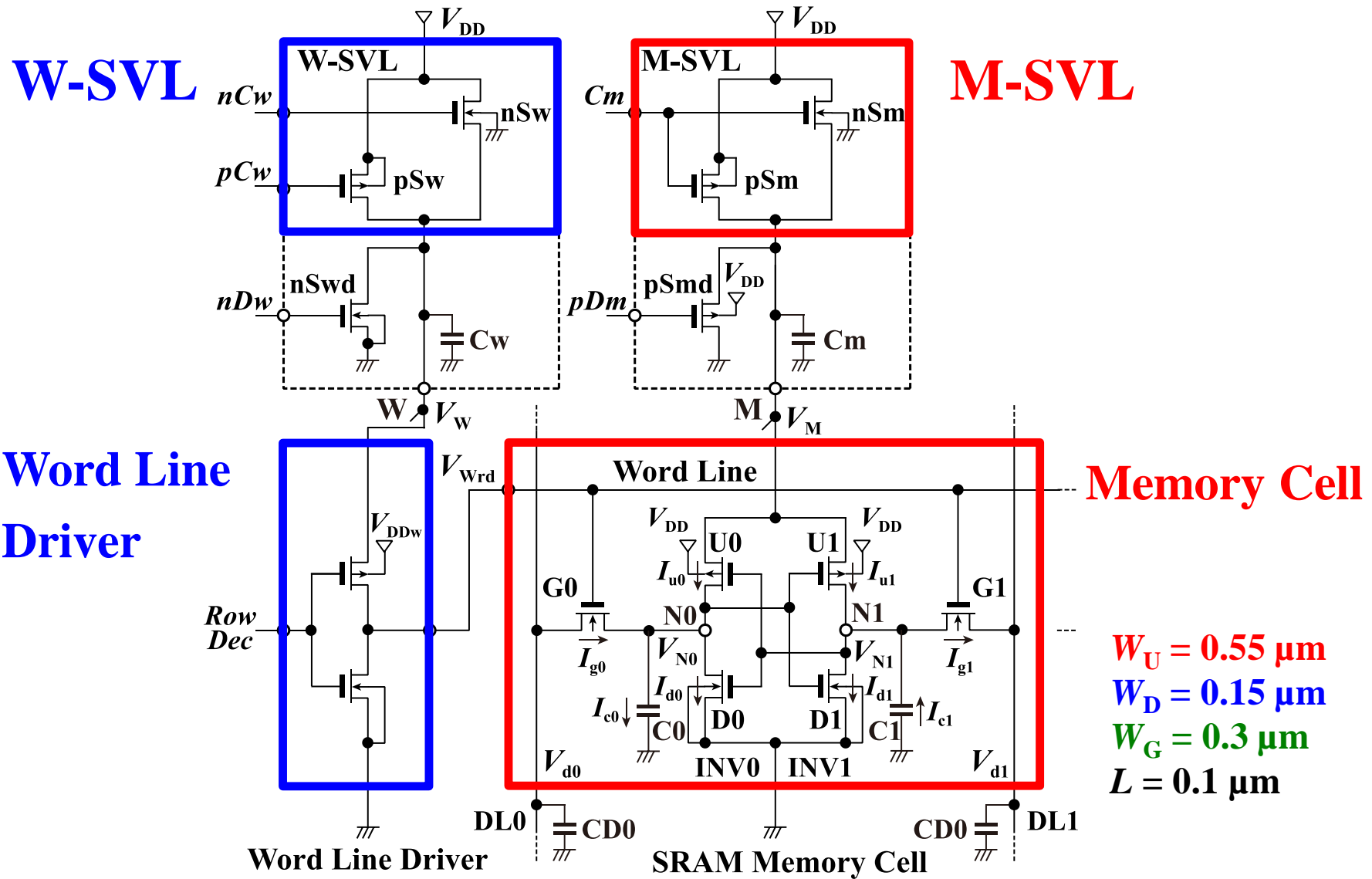


1A-8 Development of a High Stability, Low Standby Power Six-Transistor CMOS SRAM Employing a Single Power Supply



Memory Cell: 8-bit \times 64W \times 4W
W-SVL : 1
(1 SVL/64 Word-line drivers)
M-SVL : 8
(1 SVL/256 Memory Cells)
Silicon Area: 66,269 μm^2
Area Overhead of SVLs: 1.383%

Newly Developed SRAM Memory Cell

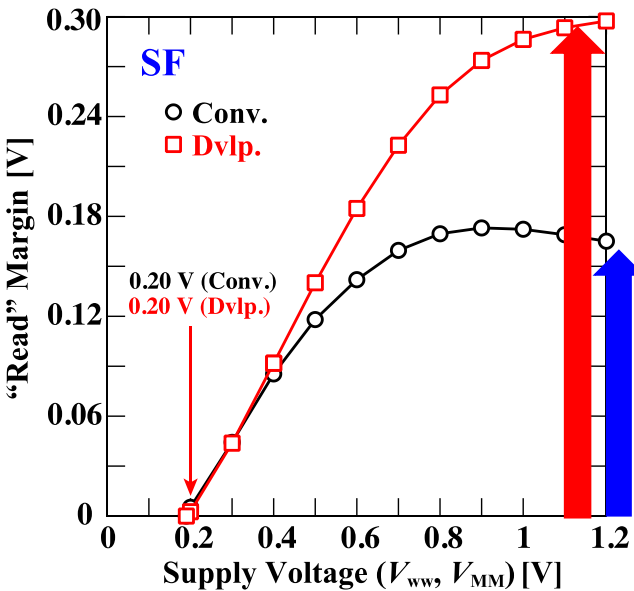


SVL: Self-controllable Voltage Level circuit

“Read” Margin of SRAMs

SF (+6σ)

$V_{tn} = 0.275 \text{ V (+53 mV)}$
 $V_{tp} = -0.139 \text{ V (+103 mV)}$

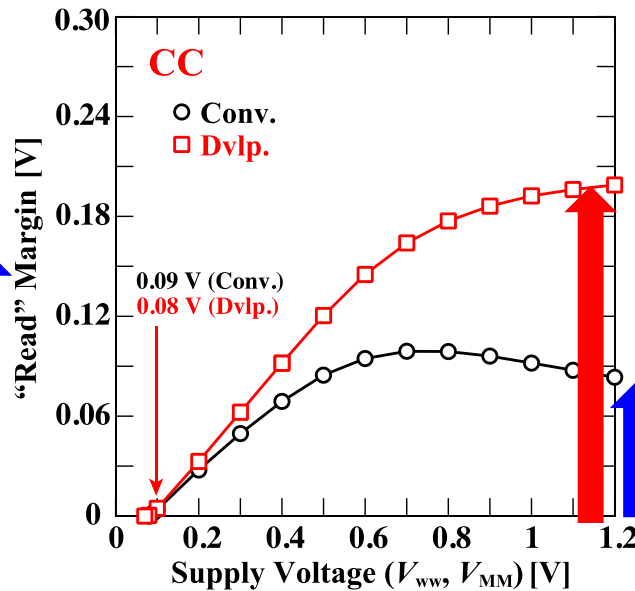


$V_{ww} = 1.2 \text{ V}$

0.1651 V (Conv.) **100.00 %**
 0.2974 V (Dvlp.) **180.13 %**

CC (Ave.)

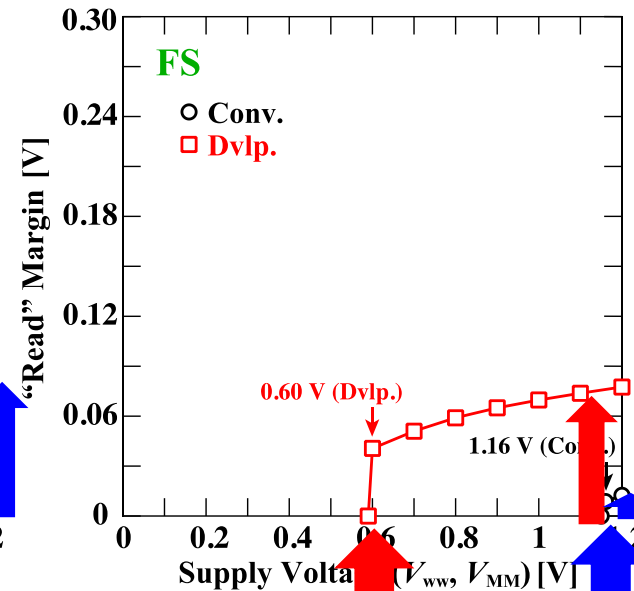
$V_{tn} = 0.222 \text{ V (0)}$
 $V_{tp} = -0.242 \text{ V (0)}$



0.0834 V (Conv.) **100.00 %**
 0.1989 V (Dvlp.) **238.48 %**

FS (-6σ)

$V_{tn} = 0.142 \text{ V (-80 mV)}$
 $V_{tp} = -0.300 \text{ V (-58 mV)}$



0.60 V 1.16V

0.0124 V (Conv.) **100.00 %**
 0.0775 V (Dvlp.) **625.00 %**

Minimum supply voltage of static “Read” operation

Conv. 0.20 V
 Dvlp. 0.20 V

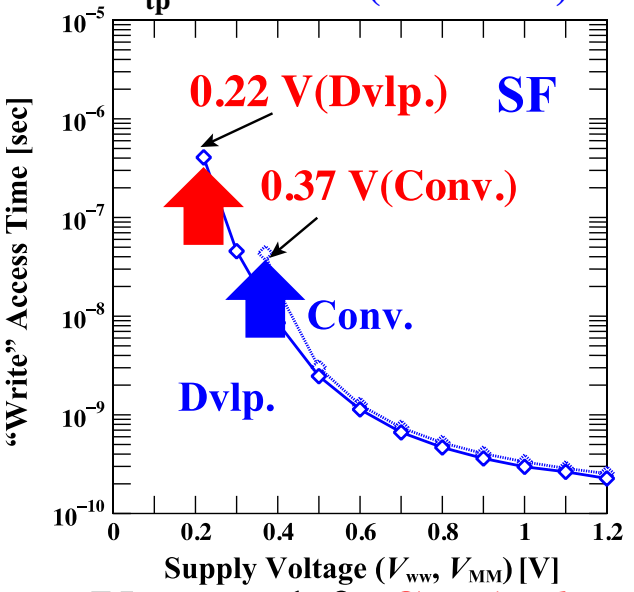
Conv. 0.09 V
 Dvlp. 0.08 V

Conv. 1.16V
 Dvlp. 0.60 V

“Write” Access Time of SRAMs

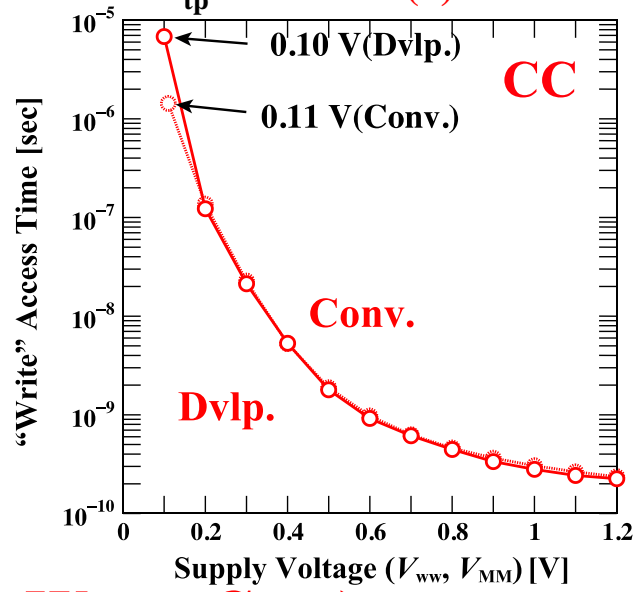
SF (+6σ)

$V_{tn} = 0.275 \text{ V (+53 mV)}$
 $V_{tp} = -0.139 \text{ V (+103 mV)}$



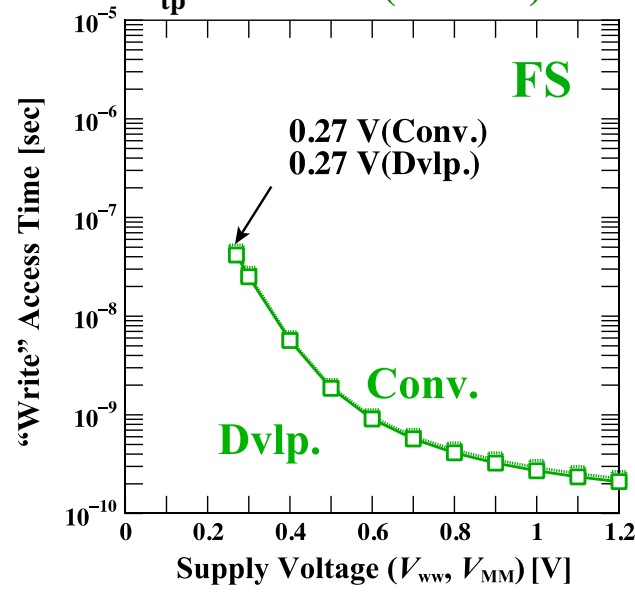
CC (Ave.)

$V_{tn} = 0.222 \text{ V (0)}$
 $V_{tp} = -0.242 \text{ V (0)}$



FS (-6σ)

$V_{tn} = 0.142 \text{ V (-80 mV)}$
 $V_{tp} = -0.300 \text{ V (-58 mV)}$



$V_{WW} = 1.0$ **SF (+6σ : Worst Case)**

“Write” Access Time [psec]

Conv. = 333.49 Dvlp. = 297.22 (89.12 %)

Minimum Supply Voltage for dynamic “Write” operation

Conv. 0.37 V

Dvlp. 0.22 V

Conv. 0.11 V

Dvlp. 0.10 V

Conv. 0.27 V

Dvlp. 0.27 V

Characteristics of 6Tr 2K-bit SRAM

	“Read” Margin FS $V_{DD}=1.2V$	Min. Supply Volt. in “Read” FS	Min. Supply Volt. in “Write” SF	Standby Power P_{st} $V_{DD}=1.0V$	Silicon Area [μm^2]
Conv. SRAM	0.012 V	1.05 V	0.37 V	25.2 μW	65,365
Dvlp. SRAM	0.078 V	0.41 V (39.05%)	0.22 V (59.46%)	1.17 μW (4.64 %)	66,269 (101.383 %)

SVL :

- Small Area Overhead **1.383%**
- **Low Voltage Operation, Expand “Read” and “Write” margins**