



#### GraphSAR: A Sparsity-Aware Processing-in-Memory Architecture for Large-Scale Graph Processing on ReRAMs

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- Background
- Motivation
- Related Work
- GraphSAR design
- Experiment Results
- Conclusion







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- Graphs are widely used!
- Graph: represent **data** and their **relationships**
- Application: social network analysis, neural network modeling, user behavior analysis, brain network modeling ...
- System & Architecture: support for graph-based applications





## **Application I: PageRank**

- Sorting billions of pages according to key words in one second
  - Graph: 2.9 b, 0.36 s

Important

Page A

- PageRank: 0.2 b, 0.30 s
- Google PageRank Algorithm
  - The rank of a page depends on ranks of pages which link to it



 $p_i \in M(p_i)$ 



搜索工具

PageRank让链接来「投票」 - PageRank算法 - 自Google網站管理員工具移除

#### PageRank - Wikipedia, the free encyclopedia

Google+ 搜索 图片 地图 Play YouTube 新闻 Gmail 更多 -

pagerank







• Collaborative filtering based on similar users



Iterate:

- ALS: Alternating Least Squares
  - Minimize Mean Square Error (MSE)
    - Calculating using tags
    - Recommending using non-tags
- Sparse matrix = Graph

$$u_i = \arg\min_{w} \sum_{j \in N[i]} (r_{ij} - m_j \cdot w)^2$$

$$m_j = \arg\min_{w} \sum_{i \in N[j]} (r_{ij} - u_i \cdot w)^2$$

Qiu, Jiantao, et al. "Going deeper with embedded fpga platform for convolutional neural network." Proceedings of the 2016 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays. ACM, 2016.

- Data & relationship = Graph
  - Neuron: vertex
  - Synapse: edge
  - Stimulus intensity: value
- Using graphs to represent different neural networks







## Application III: Deep Learning



## **Generality requirement**

- High-level abstraction model
  - Read-based/Queue-based Model for BFS/APSP
     [Stanford, PACT'10] ×
  - − GAS Model [Google, SIGMOD'10] √
- In GAS (Gather-Apply-Scatter) Model
  - Different algorithms ightarrow Different Apply functions
  - Traverse edges and scatter src to dst





Malewicz, Grzegorz, et al. "Pregel: a system for large-scale graph processing." SIGMOD. ACM, 2010. Hong, Sungpack, Tayo Oguntebi, and Kunle Olukotun. "Efficient parallel graph exploration on multi-core CPU and GPU." PACT, IEEE, 2011.







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**Challenges in graph processing** 

• Key in graph processing: efficient data transferring



Locality

LLC Miss

43.9%

49.7%

access

54.9%

71.0%







- Memristor
  - Resistance can be changed by voltage
- Storage
  - Memristor crossbar
  - Using changeable resistance to store information

#### Computation

 Processing-in-memory, 10x ~ 100x energy efficiency improvement compared with conventional von Neumann architecture













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## **RPBFS** [Hong Kong PolyU, NVMSA 17]

- Designed for Breadth-First Search
  - Using 1 bit to represent status of a vertex
  - Graph Bank: edge storage
    - Parallel processing
  - Master Bank: vertex storage
    - **Centralized processing**
- Performance
  - 33.8x speedup against CPU
  - 16.0x speedup against GPU
- However...

  - د الع الح − Centralization scheme → Scalability problem<sup>II</sup>











- Different patterns  $\rightarrow$  corresponding memories  $\rightarrow$  hybrid memory



- Performance
  - 114x energy efficiency improvement against CPU+DRAM
  - Memory subsystem energy consumption < 50%</li>





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- Matrix-vector representation for graph processing
  - Src vertex vector, adjacency matrix  $\rightarrow$  Dst vertex vector
  - MVM (e.g., PageRank): direct mapping
  - Non-MVM (e.g., BFS): activating each row sequentially
- Divide a large adjacency matrix into small **blocks**



(a) Vertex Program in Graph View

(b) Vertex Program in Matrix View







MVM (e.g., PageRank): direct mapping









- Non-MVM (e.g., BFS): activating each row sequentially







- Compared with CPU
  - Speedup: 16.01x
  - Energy efficiency: 33.82x
- Compared with GPU
  - Speedup: 1.69x ~ 2.19x
  - Energy efficiency: 4.77x ~ 8.91x













• Energy efficiency of graph processing can be improved by using ReRAM



	RPBFS	HyVE	GraphR	
Algorithm	Only BFS	General purposed	General purposed	
Storage	RRAM	Hybrid	RRAM	
Computation	CMOS	CMOS	RRAM/CMOS	







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• GraphR: Writing ReRAM (adjacency list  $\rightarrow$  block)



• Write-and-verify scheme of ReRAM: Heavy writing overheads



Sparsity of graphs: Low parallelism









- Design I: Processing-in-memory
- Design II: Sparsity-aware partitioning



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- Conversion leads to low parallelism/heavy writing overheads
- Directly storing blocks on ReRAM



**Besign II: Sparsity-aware partition** 

• Storing 8\*8 blocks leads to memory space overheads





- For algorithms on unweighted graphs
  - e.g., PageRank, BFS, etc.
  - Scatter the same value to neighbors
  - One bit of an edge to represent connectivity









- Vertex clustering  $\rightarrow$  less blocks to be processed
  - Consecutive vertices in the original adjacency list tend to gather
  - Original indices are not continuous
  - Assign new indices to vertices when reading edges
  - Only O(n) complexity

Original edge list dst src dst src \*\*\*\*\* 3 3 

Edge list	Block edge	$\begin{array}{c} 0 \rightarrow 0 \\ 2 \rightarrow 1 \end{array}$	Edge list	Block edge		
$0 \rightarrow 2$ $1 \rightarrow 8$ $2 \rightarrow 5$ $3 \rightarrow 4$ $4 \rightarrow 7$ $I$ $6 \rightarrow 4$ $I$	• • • • • • • • • • • • • • • • • • • •	$1 \rightarrow 2$ $3 \rightarrow 3$ $4 \rightarrow 6$ $7 \rightarrow 7$ $6 \rightarrow 8$	$0 \rightarrow 1$ $2 \rightarrow 3$ $1 \rightarrow 4$ $5 \rightarrow 6$ $6 \rightarrow 7$ $8 \rightarrow 6$	• •• • •• •• •• •• •• •• •• •• •• •• •• •• ••		







- According to the sparsity-aware partitioning
  - Edges are stored into edge lists and block lists
  - Edge lists and block lists are stored into different banks for the alignment purpose









- Selecting: activate a block for processing
  - GraphR: activate a row
- Processing: process edge list and block list separately
  - GraphR: treat a block with one edge as a block









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#### • Datasets

	WV	HP	GG	YT	РК	СА	WT	TW	FS	YH
# V	7.12k	34.5k	0.88m	1.13m	1.63m	1.97m	2.39m	41.7m	65.6m	1.41b
# E	0.10m	0.42m	5.11m	2.99m	30.6m	2.77m	5.02m	1.47b	1.81b	6.64b
type	social	citation	web	commun ity	social	road	commun ication	social	commun ity	web

• Algorithms

Jure Leskovec et al. SNAP Datasets: Stanford large network dataset collection. Haewoon Kwak et al. What is twitter, a social network or a news media? Yahoo WebScope. Yahoo! altavista web page hyper-link connectivity graph, circa 2002.

- PageRank, Breadth-first Search, Connected Components
- Configuration
  - ReRAM simulator: NVSim
    - read/write energy consumption: 1.08pJ/7.4pJ
    - read/write latency: 29.31ns/50.88ns
    - HRS/LRS resistance: 25MΩ/50KΩ
    - read/write voltage: 0.7V/2V
    - current of LRS/HRS: 40μA/2μA





A LIFO AL LIFO

- Single bit implementation
  - Speedup: 1.15x
  - Energy efficiency improvement: 2.37x
  - Energy-Delay Product reduction: 2.73x







- Lightweight clustering
  - Speedup: 1.30x
  - Energy efficiency improvement: 1.37x
  - Energy-Delay Product reduction: 1.78x





- Compared with GraphR (already used Opt. I & II)
  - Speedup: 1.85x
  - Energy efficiency improvement: 4.43x
  - Energy-Delay Product reduction: 8.19x



Results – Memory space overhead

- Compared with using adjacency list (need to write ReRAM)
  - Only 1.54x storage overheads
  - 46.87x storage overheads when storing 8\*8 blocks









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### Conclusion



- GraphSAR
  - Improving energy efficiency/Accelerating graph processing using ReRAM
  - Design for different graph algorithms
  - Both computation and storage optimization









- 1. Linghao Song et al. GraphE: Accelerating graph processing using reram. In HPCA, pages 531–543. IEEE, 2018.
- Aapo Kyrola et al. Graphchi: Large-scale graph computation on just a pc. In OSDI, pages 31– 46. USENIX, 2012.
- 3. Amitabha Roy et al. X-stream: Edge-centric graph processing using streaming partitions. In SOSP, pages 472–488. ACM, 2013.
- 4. Xiaowei Zhu et al. Gridgraph: Large-scale graph processing on a single machine using 2-level hierarchical partitioning. In ATC, pages 375–386. USENIX, 2015.
- 5. Yuze Chi et al. Nxgraph: An efficient graph processing system on a single machine. In ICDE, pages 409–420. IEEE, 2016.
- 6. Grzegorz Malewicz et al. Pregel: a system for large-scale graph processing. In SIGMOD, pages 135–146. ACM, 2010.
- 7. Yucheng Low et al. Distributed GraphLab: a framework for machine learning and data mining in the cloud. Proceedings of the VLDB Endowment, 5(8):716–727, 2012.
- 8. Tae Jun Ham et al. Graphicionado: A high-performance and energy-efficient accelerator for graph analytics. In MICRO, pages 1–13. IEEE, 2016.
- 9. Fabien Alibart et al. High precision tuning of state for memristive devices by adaptable variation-tolerant algorithm. Nanotechnology, 23(7):075201, 2012.
- Cong Xu et al. Overcoming the challenges of crossbar resistive memory architectures. In HPCA, pages 476–488. IEEE, 2015.







- 11. Lei Han et al. A novel reram-based processing-in-memory architecture for graph computing. In NVMSA, pages 1–6. IEEE, 2017.
- 12. Tianhao Huang et al. Hyve: Hybrid vertex-edge memory hierarchy for energyefficient graph processing. In DATE. EDA Consortium, 2018.
- 13. Cong Xu et al. Understanding the trade-offs in multi-level cell reram memory design. In DAC, pages 1–6. IEEE, 2013.
- 14. Xiaowei Zhu et al. Gemini: A computation-centric distributed graph processing system. In OSDI, pages 301–316. USENIX, 2016.
- 15. Dimin Niu et al. Design of cross-point metal-oxide reram emphasizing reliability and cost. In ICCAD, pages 17–23. IEEE, 2013.
- 16. Jure Leskovec et al. SNAP Datasets: Stanford large network dataset collection. http://snap.stanford.edu/data, June 2014.
- 17. Haewoon Kwak et al. What is twitter, a social network or a news media? In WWW, pages 591–600. ACM, 2010.
- 18. Yahoo WebScope. Yahoo! altavista web page hyper-link connectivity graph, circa 2002. http://webscope.sandbox.yahoo.com/, 2012.
- Xiangyu Dong et al. Nvsim: A circuit-level performance, energy, and area model for emerging non-volatile memory. In Emerging Memory Technologies, pages 15–50. Springer, 2014.







- 20. Shimeng Yu et al. Investigating the switching dynamics and multilevel capability of bipolar metal oxide resistive switching memory. Applied Physics Letters, 98(10):103514, 2011.
- 21. Steven JE Wilton and Norman P Jouppi. Cacti: An enhanced cache access and cycle time model. JSSC, 31(5):677–688, 1996.
- 22. Boris Murmann. ADC performance survey 1997-2017. http://web.stanford.edu/~m urmann/adcsurvey.html, August 2017.





# **Thank you!** Q&A