ASP-DAC 2019

24th Asia and South Pacific Design Automation Conference

FINAL PROGRAM

Date: January 21-24, 2019

Place: Miraikan
National Museum of Emerging Science and Information

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ASIA SOUTH PACIFIC DESIGN AUTOMATION CONFERENCE

http://www.aspdac.com/

ASP-DAC 2019

Contents

Highlights

Opening and Keynote I

Tuesday, January 22, 2019, 9:30-10:30

Tao Zhang **(Tsinghua University, China)**
"Development Trend of Artificial Intelligence Technology and its Application in the Field of Robotics"

Keynote II

Wednesday, January 23, 2019, 9:00-10:00

Satoshi Matsuoka **(RIKEN, Japan)**
"Post-K: A Game-changing Supercomputer with Groundbreaking A64fx High Performance Arm Processor"

Keynote III

Thursday, January 24, 2019, 9:00-10:00

Yasuhisa Shimazaki **(Renesas Electronics, Japan)**
"Hardware and Software Security Technologies to Enable Future Connected Cars"

Special Sessions

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Tuesday, January 22, 2019, 13:30-15:35

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Tuesday, January 22, 2019, 15:55-17:10

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Thursday, January 24, 2019, 13:15-14:30

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Tutorials

ASP-DAC 2019 offers attendees a set of three-hour intense introductions to specific topics. If you register for tutorials, you have the option to select two out of the nine topics. (This year, each tutorial will be presented once.)

Tutorial-1: Integrating Hardware and Algorithm Advances for Cognitive Systems

Monday, January 21, 2019, 9:30-12:30

Organizer:

Hai Li (Duke University)

Speakers:

Kaushik Roy (Purdue University)

Hai Li (Duke University)

Tutorial-2: Enablement of No-Human-in-the-Loop IC Design: Status and Directions

Monday, January 21, 2019, 9:30-12:30

Organizer:

Andrew B. Kahng (University of California, San Diego)

Speakers:

David White, Senior (Cadence Design Systems, Inc.)

Shankar Sadasivam (Qualcomm Inc.)

Andrew B. Kahng (University of California, San Diego)

Tutorial-3: Energy-Efficient Processing and Machine Learning at the Edge: from Sensing to Sensemaking

Monday, January 21, 2019, 9:30-12:30

Organizer/Speaker:

Massimo Alioto (National University of Singapore)

Tutorial-4: Design for Reliability in the Nano-CMOS Era: New Holistic Methodologies for Reliability Modeling and Optimization

Monday, January 21, 2019, 9:30-12:30

Organizers/Speakers:

Sheldon Tan (University of California, Riverside)

Hussam Amrouch (Karlsruhe Institute of Technology)

Tutorial-5: Machine Learning in Test

Monday, January 21, 2019, 9:30-12:30

Organizer/Speaker:

Yu Huang (Mentor, A Siemens Business)

Tutorial-6: Recent Development and Future Perspective of Quantum Annealing

Monday, January 21, 2019, 14:00-17:00

Organizer:

Shu Tanaka (Waseda University)

Speakers:

Shu Tanaka (Waseda University)

Yoshiki Matsuda (Fixstars Corporation)

Kotaro Tanahashi (Recruit Communications Co., Ltd.)

Yuya Seki (National Institute of Advanced Industrial Science and Technology, Japan)

Tutorial-7: Embedded Heterogeneous Computing: Architectural Landscape and Software Challenges

Monday, January 21, 2019, 14:00-17:00

Organizer/Speaker:

Tulika Mitra (National University of Singapore)

Tutorial-8: Smart Image Sensor Systems

Monday, January 21, 2019, 14:00-17:00

Organizers/Speakers:

Marilyn Wolf (Georgia Institute of Technology)

Saibal Mukhopodhyay (Georgia Institute of Technology)

Tutorial-9: Machine Learning for Reliability of ICs and Systems

Monday, January 21, 2019, 14:00-17:00

Organizer:

Mehdi B. Tahoori (Karlsruhe Institute of Technology)

Speakers:

Mehdi B. Tahoori (Karlsruhe Institute of Technology)

Krishnendu Chakrabarty (Duke University)

Welcome to ASP-DAC 2019

On behalf of the Organizing Committee, I would like to invite all of the engineers on the LSI design and design automation areas to the 24th Asia and South Pacific Design Automation Conference (ASP-DAC 2019). ASP-DAC 2019 will be held from January 21st (Mon.) to January 24th (Thu.), 2019 at Miraikan, National Museum of Emerging Science and Innovation, Tokyo, Japan.

ASP-DAC is a high-quality and premium conference on Electronic Design Automation (EDA) area like other sister conferences such as Design Automation Conference (DAC), Design, Automation & Test in Europe (DATE), International Conference on Computer Aided Design (ICCAD), and Embedded Systems Week (ESWEEK). ASP-DAC started in 1995 and has continuously offered opportunity to know the recent advanced technologies on LSI design and design automation areas, and to communicate each other for researchers and designers around Asia and South Pacific regions.

The conference site is Miraikan, which is a national science museum opened in July 2001, and is located at Odaiba district of Tokyo, Japan. Miraikan is close to central Tokyo, about 30 minutes by train. It is easily accessed from Narita (New Tokyo) or Haneda (Tokyo) international airport by train or by bus. Joining the conference and participating in technological discussions, you can also enjoy many attractions in Tokyo area, such as Ginza, Asakusa (Senso-ji temple), Akiharabara, Toyosu (new fish market), Ryogoku Sumo hall, Tokyo Sky Tree, Tokyo Disneyland and Disneysea, etc.

ASP-DAC 2019 received 304 submissions from all over the world. Based on rigorous and thorough reviews and a full-day face-to-face meeting by the Technical Program Committee in August at Korea, 99 papers have been accepted and 29 technical sessions have been organized. Five Special Sessions have also been organized based on invited talks by the Technical Program Committee.

We have arranged three Keynote sessions at the beginning of each day to know the future directions of this area. The first keynote address is 'Development Trend of Artificial Intelligence Technology and its Application in the Field of Robotics' by Prof. Tao Zhang of Tsinghua University of Control Science and Engineering, China. The second one is 'Post-K: A Game-changing Supercomputer with Groundbreaking A64fx High Performance Arm Processor' by Dr. Satoshi Matsuoka of RIKEN Center for Computational Science, Japan. The third keynote address is 'Hardware and Software Security Technologies to Enable Future Connected Cars' by Mr. Yasuhisa Shimazaki of Renesas Electronics Corporation, Japan.

The Designers' Forum is a unique program that will share design experience and solutions of actual product designs of the industries, which will be held in the afternoon of January 23nd and 24th. The topics discussed in this forum include Robotics, advanced image sensing and processing technologies, emerging technologies for Tokyo Olympic 2020, and virtual reality technologies. The University Design Contest is also an important annual event of ASP-DAC where 13 high-quality designs all including actual silicon proof were selected for presentation at Tuesday, January 22nd.

Nine tutorials have been arranged on Monday, January 21st. Each tutorial has 3 hour presentation. Registrants can choose one topics from the morning session including 5 topics and another one from the afternoon session including 4 topics depending on their interests and can obtain wider perspective on the recent hot topics with the reduced tutorial fee.

ASP-DAC 2019 offers you an ideal opportunity to touch the recent technologies and the future directions on the LSI design and design automation areas. You will be able to meet and discuss with a lot of researchers and designers on this area, so please do not miss ASP-DAC 2019. Finally, we would like to express our sincere appreciation to sponsors and supporters.

Toshiyuki Shibuya
General Chair, ASP-DAC 2019

Message from the Technical Program Committee


Taewhan Kim


Tsung-Yi Ho


Masanori Hashimoto

On behalf of the Technical Program Committee of the 24th Asia and South Pacific Design Automation Conference (ASP-DAC) 2019, we would like to welcome all of you to the conference scheduled from January 21 to 24, 2019 in Tokyo, Japan.

This year, ASP-DAC received 304 paper submissions from 25 countries/regions, with the majority of them from Asia, North America, and Europe. The challenge of selecting which papers to accept was significant. We organized the Technical Program Committee (TPC) with 102 professionals who are leading experts on EDA, IC design, system design, hardware security, and emerging technologies/applications. These TPC members are from 12 countries/regions, and organized into 15 subcommittees. The review process ensured fairness through a rigorous double-blind review process to resolve any possible conflict of interest. The full-day TPC meeting was held at the Seoul National University (SNU) on August 27, 2018, with the EDA Workshop afterwards. Almost all TPC members physically attended the TPC meeting, and some joined via teleconferencing due to personal emergency. Out of the 304 submissions, 101 high-quality regular papers were selected, which corresponds to a very competitive acceptance rate of 33%.

The complete conference program consists of regular papers, keynote speeches, as well as special and design contest sessions. They are compiled into a three-day, four parallel-session program. The keynotes are held every morning to kick off the technical sessions. The special and design sessions are allocated on track A. The regular papers are presented in 29 sessions on tracks B, C, and D.

Each Subcommittee was eligible to nominate one best paper candidate. The Best Paper Award (BPA) Committee which consists of 15 members selected 10 best paper candidates, which further went through a rigorous evaluation process. Finally two best paper award winners were selected.

The fruitful technical program of the ASP-DAC 2019 was not possible without hard work of all the authors, reviewers, and TPC members. Special thanks go to TPC Secretaries for their excellent support. Thanks to the generous financial support from ESRC/SNU and ACM SIGDA Korea Chapter, the TPC meeting provided high-quality supplements in both academic and social programs. Finally, we would also like to thank the Organizing Committee for their extraordinary services.

We hope you enjoy the ASP-DAC 2019 technical program.

Taewhan Kim
TPC Chair, ASP-DAC 2019

Tsung-Yi Ho
TPC Vice Chair

Masanori Hashimoto
TPC Vice Chair

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Subcommittees and Subcommittee Chairs (* : Subcommittee Chairs)

[1] System-Level Modeling and Design Methodology

* **Sri Parameswaran** (University of New South Wales, Australia)
Akash Kumar (Technische Universitaet Dresden, Germany)
Jongeun Lee (Ulsan National Institute of Science and Technology, Korea)
Naehyuck Chang (Korea Advanced Institute of Science and Technology, Korea)
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[2] Embedded System Architecture and Design

* **Wujie Wen** (Florida International University, USA)
Xue Lin (Northeastern University, USA)
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Hsiang-Yun Cheng (Academia Sinica, Taiwan)
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Yongpan Liu (Tsinghua University, China)
Lei Jiang (Indiana University Bloomingto, USA)
Xiang Cheng (George Mason University, USA)
Guangyu Sun (Peking University, China)

[3] On-chip Communication and Networks-on-Chip

* **Jiang Xu** (Hong Kong University of Science and Technology, Hong Kong)
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Yaoyao Ye (Shanghai Jiao Tong University, China)
John Kim (KAIST, Korea)
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Lide Duan (University of Texas at San Antonio, USA)

[4] Embedded Software

* **Franco Fummi** (University of Verona, Italy)
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[5,6] Device/Circuit-Level Modeling, Simulation and Verification & Analog, RF and Mixed Signal

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Mark Po-Hung Lin (National Chung Cheng University, Taiwan)
SoYoung Kim (Sungkyunkwan University, Korea)
Jun Tao (Fudan University, China)

[7] Power Analysis, Low Power Design, and Thermal Management

* **Sheldon Tan** (University of California at Riverside, USA)
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Masaaki Kondo (University of Tokyo, Japan)
Yuko Hara-Azumi (Tokyo Institute of Technology, Japan)
Jun Shiomi (Kyoto University, Japan)

[8] Logic/High-Level Synthesis and Optimization

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Mihir Choudhury (IBM Research, USA)
Fabrizio Ferrandi (Politecnico di Milano, Italy)
Weikang Qian (Shanghai Jiao Tong University, China)
John Wickerson (Imperial College London, UK)
Shouyi Yin (Tsinghua University, China)

[9] Physical Design

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Hung-Ming Chen (National Chiao Tung University, Taiwan)
Wenxing Zhu (Fuzhou University, China)

[10,11] Design for Manufacturability and Reliability & Timing and Signal/Power Integrity

* **Charles Chiang** (Synopsys. Inc., USA)
Iris Hui-Ru Jiang (National Taiwan University, Taiwan)
Shigeki Nojima (Toshiba Memory, Japan)
Changhao Yan (Fudan University, China)
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Shao Yun Fang (National Taiwan University of Science and Technology, Taiwan)
Wenjian Yu (Tsing Hua University, China)

[12] Test and Design for Testability

* **Kohei Miyase** (Kyushu Institute of Technology, Japan)
Ying Zhang (Tongji University, China)
Seetal Potluri (Technische Universität Dresden, Germany)
Satoshi Ohtake (Oita University, Japan)
Jin-Fu Li (National Central University, Taiwan)
Michihiro Shintani (Nara Institute of Science and Technology, Japan)

[13] Security and Fault-Tolerant System

* **Jakub Szefer** (Yale University, USA)
Yunheung Paek (Seoul National University, Korea)
Ray C.C. Cheung (City University of Hong Kong, Hong Kong)
Hai Zhou (Northwestern University, USA)
Estelle Wang (Continental Automotive Singapore Pte Ltd., Singapore)
Chengmo Yang (University of Delaware, USA)
Dong Kyue Kim (Hanyang University, Korea)

[14] Emerging Technology

* **Shigeru Yamashita** (Ritsumeikan University, Japan)
Deliang Fan (University of Central Florida, USA)
Xiaoming Chen (Institute of Computing Technology, Chinese Academy of Sciences, China)
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Jianlei Yang (Beihang University, China)
Pingqiang Zhou (ShanghaiTech University, China)

[15] Emerging Application

* **Jiang Hu** (Texas A&M University, USA)
Zhihao Jiang (ShanghaiTech University, China)
Yanzhi Wang (Syracuse University, USA)
Younghyun Kim (University of Wisconsin-Madison, USA)
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University LSI Design Contest

The University LSI Design Contest has been conceived as a unique program at ASP-DAC. The purpose of the contest is to encourage research in LSI design at universities and its realization on a chip by providing opportunities to present and discuss the innovative and state-of-the-art design. The scope of the contest covers circuit techniques for (1) Analog / RF / Mixed-Signal Circuits, (2) Digital Signal Processor, (3) Microprocessors, and (4) Custom Application Specific Circuits / Memories, and methodologies for (a) Full-Custom / Cell-Based LSIs, (b) Gate Arrays, and (c) Field Programmable Devices.

This year, the University LSI Design Contest Committee received 15 designs from five countries/areas, and selected 13 designs out of them. The selected designs will be disclosed in Session 1A at three-minute presentations, followed by interactive discussions in front of their posters with light meals. For three outstanding designs, The Best Design Award and The Special Feature Award will be presented in the opening session. We sincerely acknowledge the other contributions to the contest, too. It is our earnest belief to promote and enhance research and education in LSI design in academic organizations. Please come to the University LSI Design Contest and enjoy the stimulating discussions.

Date: Tuesday, January 22, 2019

Place: Tokyo Odaiba Waterfront, Japan

Oral Presentation: Room Saturn (10:45-12:00)
Poster Presentation: Room Jupiter [Food will be served] (12:00-13:30)

University LSI Design Contest Committee Co-Chairs:

Kousuke Miyaji
(Shinshu University)

Akira Tsuchiya
(The University of Shiga Prefecture)

Designers' Forum

The Designers' Forum is conceived as a unique program that shares the design experience and solutions of real product developments among LSI designers and EDA academia/developers. The topics discussed in this forum includes Robotics, Imaging technologies and applications, Virtual Reality, and Emerging Technologies for Tokyo Olympic 2020.

Oral Sessions: (5A) Robotics: From System Design to Application
(6A) Advanced Imaging Technologies and Applications
(8A) Emerging Technologies for Tokyo Olympic 2020
(9A) Beyond the Virtual Reality World

Session 5A (13:50-15:05, Jan. 23rd)
[Robotics: From System Design to Application]

This session includes three interesting invited talks regarding Robotics that is a key technology for realizing Society 5.0, and it has significant potentials to change our daily life. The first talk focuses on a modeling technique for minimal invasive surgery, and that could be used on remote medicine. The second presentation targets ROS (Robot Operating System) led by Open Robotics that is a state-of-the-art development framework. The third talk discusses rapid development of Robotics technology through contests and open collaborations. The purpose of this session is to share and discuss the state-of-the-art and future Robotics from the viewpoint of various aspects such as vision technologies, design methodologies, and open collaborations.

Session 6A (15:35-17:15, Jan. 23rd)
[Advanced Imaging Technologies and Applications]

The market growth in image sensor is very rapid. Also, image sensors are widely adapted to monitoring, autonomous driving, home-security cameras, and medical fields. This session will visit its trend, hardware implementation, and system design in each application. The first talk presents image sensors for heart rate detection in driver monitoring system, nursing care and security systems. The next presentation shows LiDAR systems for 200m range detection on highway in autonomous driving. The third one shares a low-power event-driven image sensor for detecting moving objects in wireless products. The final talk demonstrates fundus cameras with high frame-rate for physiological monitoring and pathological diagnosis.

Session 8A (13:30-14:45, Jan. 24th)
[Emerging Technologies for Tokyo Olympic 2020]

Tokyo 2020 Olympic and Paralympic Games is a most exciting event in the last few decades in Japan, and is also very good test-field to evaluate emerging technologies for creating Olympic legacy. The first talk presents the wearable robotic device, named eHIMICOf, which assist human movement softly by using Bowden cables to transfer power from motor system. The next presentation shows image processing for object detection and scene recognition based on deep learning technology. The final talk demonstrates emerging devices for accurate spatial sensing and efficient battery management to realize security and safety for autonomous driving and autonomous control.

Session 9A (15:00-16:45, Jan. 24th)
[Beyond the Virtual Reality World]

Virtual reality (VR) technique will take a key role for a human-machine collaboration. This session will talk about the techniques for the next generation VR systems. The first topic presents social impacts from the VR and will discuss about the future of the VR including the latest VR developments and researches. The second topic presents a new wearable display which feature is extremely light weight for easy installation to VR users. The proposed display adopts a new scanning fiber method to improve image qualities. The last presentation discusses new technologies of video presentation techniques to feel super reality for sports experiences. The proposed super-real video expression is effective for both conveying the intention of the producer and a useful scene for viewers. We want to discuss the current technologies trend and also the future impact beyond the VR in this session.

Designers' Forum Co-Chairs:
Masaitsu Nakajima (Socionext, Japan) **Koji Inoue** (Kyushu University, Japan)

ACM SIGDA Student Research Forum at ASP-DAC 2019

The Student Research Forum at the ASP-DAC is renovated from a traditional poster session hosted by ACM SIGDA for Ph.D. students to present and discuss their dissertation research with experts in system design and design automation community. Starting from 2015, the forum includes both Ph.D. and M.S. students, offering great opportunity for the students to establish contacts for their future career. In addition, the forum helps the companies and academic institutes to get an overview of the latest research and discover the extraordinary candidates for their employment. The forum is open to all students of the relevant research community and is free-of-charge.

Date and Time: 18:00-20:00, January 22nd, 2019
Location: Room Jupiter [Food will be served.]

We would like to thank the following committee members for their support and contribution to this forum.

Technical committee:

Hiromitsu Awano (The University of Tokyo, Japan)
Wanli Chang (The University of York, UK)
Yuan-Hao Chang (Academia Sinica, Taiwan)
Sudipta Chattopadhyay (Singapore University of Technology and Design, Singapore)
Xiang Chen (George Mason University, USA)
Xianzhang Chen (Chongqing University, China)
Yi-Jung Chen (National Chi Nan University, Taiwan)
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Shao-Yun Fang (National Taiwan University of Science and Technology, Taiwan)
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Masashi Tawada (Waseda University, Japan)
Chun-Yao Wang (National Tsing Hua University, Taiwan)
Hoeseok Yang (Ajou University, Korea)
Ming-Chang Yang (The Chinese University of Hong Kong, Hong Kong)
Yaoyao Ye (Shanghai Jiao Tong University, China)
Bei Yu (The Chinese University of Hong Kong, Hong Kong)

ASP-DAC liaison:

Yukihide Kohira (University of Aizu, Japan)
Masashi Tawada (Waseda University, Japan)

The sponsors of this forum are ACM SIGDA and Cadence Design Systems, Inc. We would also like to thank ASP-DAC 2019 for supporting this forum.

ACM SIGDA Student Research Forum Chair:

Pi-Cheng Hsiu
(Academic Sinica, Taiwan)

ACM SIGDA Student Research Forum Co-Chair:

Hyung Gyu Lee
(Daegu University, Korea)

Weichen Liu
(Nanyang Technological University, Singapore)

Best Paper Award

Award Winners

2B-1: **"GraphSAR: A Sparsity-Aware Processing-in-Memory Architecture for Large-Scale Graph Processing on ReRAMs"**

Guohao Dai (Tsinghua Univ., China), Tianhao Huang (Massachusetts Inst. of Tech., U.S.A.), Yu Wang, Huazhong Yang (Tsinghua Univ., China), John Wawrzynek (Univ. of California, Berkeley, U.S.A.)

3D-1: **"Energy-Efficient, Low-Latency Realization of Neural Networks through Boolean Logic Minimization"**

Mahdi Nazemi, Ghasem Pasandi, Massoud Pedram (USC, U.S.A.)

Candidates

1D-1: **"Leakage-Aware Thermal Management for Multi-Core Systems Using Piecewise Linear Model Based Predictive Control"**

Xingxing Guo, Hai Wang, Chi Zhang, He Tang, Yuan Yuan (Univ. of Electronic Science and Tech. of China, China)

2B-1: **"GraphSAR: A Sparsity-Aware Processing-in-Memory Architecture for Large-Scale Graph Processing on ReRAMs"**

Guohao Dai (Tsinghua Univ., China), Tianhao Huang (Massachusetts Inst. of Tech., U.S.A.), Yu Wang, Huazhong Yang (Tsinghua Univ., China), John Wawrzynek (Univ. of California, Berkeley, U.S.A.)

3B-1: **"A Staircase Structure for Scalable and Efficient Synthesis of Memristor-Aided Logic"**

Alwin Zulehner (Johannes Kepler Univ. Linz, Austria), Kamalika Datta (National Inst. of Tech. Meghalaya, India), Indranil Sengupta (Indian Inst. of Tech. Kharagpur, India), Robert Wille (Johannes Kepler Univ. Linz, Austria)

3D-1: **"Energy-Efficient, Low-Latency Realization of Neural Networks through Boolean Logic Minimization"**

Mahdi Nazemi, Ghasem Pasandi, Massoud Pedram (USC, U.S.A.)

4D-1: **"Routing in Optical Network-on-Chip: Minimizing Contention with Guaranteed Thermal Reliability"**

Mengquan Li (Chongqing Univ., China), Weichen Liu (Nanyang Technological Univ., Singapore), Lei Yang, Peng Chen, Duo Liu (Chongqing Univ., China), Nan Guan (Hong Kong Polytechnic Univ., Hong Kong)

5C-1: **"SRAF Insertion via Supervised Dictionary Learning"**

Hao Geng, Haoyu Yang, Yuzhe Ma (Chinese Univ. of Hong Kong, Hong Kong), Joydeep Mitra (Cadence, U.S.A.), Bei Yu (Chinese Univ. of Hong Kong, Hong Kong)

5D-3: **"Handling Stuck-at-faults in Memristor Crossbar Arrays using Matrix Transformations"**

Baogang Zhang, Necati Uysal, Deliang Fan, Rickard Ewetz (Univ. of Central Florida, U.S.A.)

7B-3: **"Phone-nomenon: A System-Level Thermal Simulator for Handheld Devices"**

Hong-Wen Chiou, Yu-Min Lee, Shin-Yu Shiau (National Chiao Tung Univ., Taiwan), Chi-Wen Pan, Tai-Yu Chen (Mediatek, Taiwan)

7C-1: **"Diffusion Break-Aware Leakage Power Optimization and Detailed Placement in Sub-10nm VLSI"**

Sun ik Heo (Samsung Electronics, Republic of Korea), Andrew B. Kahng, Minsoo Kim, Lutong Wang (UC San Diego, U.S.A.)

9C-1: **"A Figure of Merit for Assertions in Verification"**

Samuel Hertz, Debjit Pal, Spencer Offenberger, Shobha Vasudevan (Univ. of Illinois, Urbana-Champaign, U.S.A.)

University LSI Design Contest Award

Best Design Award

1A-1: **"A Wide Conversion Ratio, 92.8% Efficiency, 3-Level Buck Converter with Adaptive On/Off-Time Control and Shared Charge Pump Intermediate Voltage Regulator"**
Kousuke Miyaji, Yuki Karasawa, Takanobu Fukuoka (Shinshu Univ., Japan)

Special Feature Award

1A-2: **"A Three-Dimensional Millimeter-Wave Frequency-Shift Based CMOS Biosensor using Vertically Stacked Spiral Inductors in LC Oscillators"**
Maya Matsunaga, Taiki Nakanishi, Atsuki Kobayashi (Nagoya Univ., Japan), Kiichi Niitsu (Nagoya Univ./JST PRESTO, Japan)

1A-3: **"Design of 385 $\times$ 385 μm^2 0.165V 270pW Fully-Integrated Supply-Modulated OOK Transmitter in 65nm CMOS for Glasses-Free, Self-Powered, and Fuel-Cell-Embedded Continuous Glucose Monitoring Contact Lens"**
Kenya Hayashi, Shigeki Arata, Ge Xu, Shunya Murakami, Cong Dang Bui, Takuyoshi Doike, Maya Matsunaga, Atsuki Kobayashi (Nagoya Univ., Japan), Kiichi Niitsu (Nagoya Univ./JST PRESTO, Japan)

10-Year Retrospective Most Influential Paper Award

Award Winner

(ASP-DAC 2009)

3A-1: **"System-Level Cost Analysis and Design Exploration for Three-Dimensional Integrated Circuits (3D ICs)"**
Xiangyu Dong and Yuan Xie (Pennsylvania State Univ., United States)

Candidates

3A-1: **"System-Level Cost Analysis and Design Exploration for Three-Dimensional Integrated Circuits (3D ICs)"**
Xiangyu Dong and Yuan Xie (Pennsylvania State Univ., United States)

4D-1: **"Three-Dimensional Integration Technology and Integrated Systems"**
Mitsumasa Koyanagi, Takafumi Fukushima, Tetsu Tanaka (Tohoku Univ., Japan)

6B-2: **"FastRoute 4.0: Global Router with Efficient Via Minimization"**
Yue Xu, Yanheng Zhang, Chris Chu (Iowa State Univ., United States)

Invitation to ASP-DAC 2020

On behalf of the Organizing Committee, it is my great pleasure and honor to invite you to the 25th ASP-DAC, to be held in Beijing, China on January 13-16, 2020.

Beijing is the capital of China and a metropolis in Northern China. It has a history of more than 3,000 years and was the capital city in five dynasties for about 850 years. The city hosts a collection of amazing cultural sites such as The Great Wall, The Forbidden City, Summer Palace, Tiananmen Square, The Temple of Heaven, etc. Beijing weather features four distinct seasons - short windy spring, long hot summer, cool pleasant autumn, and long chilly winter. Food is a highlight of a visit to Beijing. Specialties include Peking Duck, Mongolian Hotpot, and noodles with meat sauce (zhajiang mian) served up in numerous Beijing restaurants.

The Conference venue is China National Convention Center (CNCC) which is on the North 4th Ring Road of Beijing, adjacent to the National Stadium (Bird Nest), the National Aquatics Center (Water Cube) and the National Indoor Stadium. CNCC is one of China's most versatile international conference venues and has held many important conferences such as APEC 2014, Belt and Road Forum for International Cooperation 2017, IECON 2017, etc.

Beijing is home to a great number of universities and colleges, including several world-class universities and research organizations of international stature, such as Tsinghua University, Peking University, China Academy of Sciences, etc. Many international students from Japan, Korea, North America, Europe, Southeast Asia, and elsewhere come to Beijing to study every year. ASP-DAC 2020 in Beijing will offer great influence to Asian and Global academic circles. Moreover, China has a large population of IC designers, and its government is paying much more attention to the development of its IC industry. ASP-DAC 2020 in Beijing will also further stimulate international collaboration in the IC industry, which is booming in China, and development of cutting edge technologies. ASP-DAC attendees, especially graduating postgraduate students, will be able to find potential jobs and academia opportunities in China, especially in Beijing. We are confident that ASP-DAC 2020 will bring great benefits to both Asian IC industry and ASP-DAC conference.

We warmly welcome participants from all around the world to meet and exchange our visions in the future design automation and embedded system design related technologies. Your active submissions are highly appreciated in order to contribute for an excellent technical program of ASP-DAC 2020.

We hope to see you all in Beijing with ASP-DAC 2020!

K.-T. Tim Cheng
General Co-Chair, ASP-DAC 2020

Huazhong Yang
General Co-Chair, ASP-DAC 2020

Tutorials

ASP-DAC 2019 offers attendees a set of three-hour intense introductions to specific topics. If you register for tutorials, you have the option to select two out of the nine topics. (This year, each tutorial will be presented once.)

	Monday, January 21				
	Room Saturn	Room Uranus	Room Venus	Room Mars	Room Mercury
9:30	**Tutorial-1:** Integrating Hardware and Algorithm Advances for Cognitive Systems	**Tutorial-2:** Enablement of No-Human-in-the-Loop IC Design: Status and Directions	**Tutorial-3:** Energy-Efficient Processing and Machine Learning at the Edge: from Sensing to Sensemaking	**Tutorial-4:** Design for Reliability in the Nano-CMOS Era: New Holistic Methodologies for Reliability Modeling and Optimization	**Tutorial-5:** Machine Learning in Test
12:30	Lunch Break				
14:00	**Tutorial-6:** Recent Development and Future Perspective of Quantum Annealing	**Tutorial-7:** Embedded Heterogeneous Computing: Architectural Landscape and Software Challenges	**Tutorial-8:** Smart Image Sensor Systems	**Tutorial-9:** Machine Learning for Reliability of ICs and Systems	
17:00					

Tutorial-1 Monday, January 21, 9:30-12:30@Room Saturn

Integrating Hardware and Algorithm Advances for Cognitive Systems

Organizer:

Hai Li (Duke University)

Speakers:

Kaushik Roy (Purdue University), **Hai Li** (Duke University)

Tutorial Outline:

As big data processing becomes pervasive and ubiquitous in our lives, the desire for embedded-everywhere and human-centric information processing calls for cognitive computing paradigm that is capable of handling large volume of data dynamically according to environmental conditions, under limited hardware resources. This demand, however, is unlikely to be satisfied through the traditional hardware and software solutions. The performance of existing computer systems is greatly hindered by the increasing performance gap between CPU and memory as well as the fast-growing power consumption, while most practice on deep learning algorithms still heavily relies on large volume of labeled data. The integrated approaches that combine novel circuit/architecture with algorithm advances emerge as one of the most important and active area in computer and computing societies. The objective of the tutorial is to give a comprehensive overview on the status of cognitive computing systems, with a particular focus on the hardware design and system implementation as well as the evolution of neural network algorithms. The research studies on conventional platform as well as the neuromorphic system based on emerging nanotechnologies will be introduced. New applications and challenges will be discussed. The materials particular emphases the technical interactions between circuit design, device characteristics, and computing systems in order to provide a comprehensive overview to the attendees with various backgrounds and interests and maximize the benefits to design and EDA communities.

Tutorial-2 Monday, January 21, 9:30-12:30@Room Uranus

Enablement of No-Human-in-the-Loop IC Design: Status and Directions

Organizer:

Andrew B. Kahng (University of California, San Diego)

Speakers:

David White, Senior (Cadence Design Systems, Inc.), **Shankar Sadasivam** (Qualcomm Inc.), **Andrew B. Kahng** (University of California, San Diego)

Tutorial Outline:

The semiconductor ecosystem faces a design crisis: design at leading nodes faces growing barriers of cost, expertise, and risk. Due to these barriers, system innovation cannot access the latest semiconductor technologies, and this jeopardizes the health of the entire industry ecosystem of design, EDA, and process. To mitigate the design crisis, leading players across the fabless, EDA and foundry sectors - as well as academic researchers - are aggressively exploring big-data / machine learning based approaches that can reduce human effort and schedule requirements of IC design.

Recently, the U.S. Defense Advanced Research Projects Agency (DARPA) has launched a new program, called "IDEA", that attacks cost and schedule barriers in IC design via "no-human-in-the-loop", 24-hour layout automation flows including the RTL-to-GDSII flow that is central to IC implementation. Commercial EDA tools have been driven by leading customers to squeeze as much design quality (PPA) from the foundry enablement as possible. By contrast, the IDEA program proposes to drive EDA tool development in a different direction: "no-human-in-the-loop" returns the focus to "automation", trading away PPA in return for autonomous, "self-driving tools", along with schedule reductions.

This tutorial will summarize key elements in the road toward "no-human-in-the-loop" IC design, including current status and near-term directions.

Machine learning and decision-making: To achieve "no-human-in-the-loop", it is necessary to understand where and why humans are in the loop of IC design today (e.g., in floorplanning, power planning, clock distribution, and timing closure steps). Wherever human expertise and decision-making is critical to design success today, it must be modeled and automated.

Dr. Shankar Sadasivam of Qualcomm (possibly, joined by his colleague Dr. Rajeev Jain) will discuss machine learning theory for decision-making, with subtopics including reinforcement learning, multi-arm and contextual bandits, Bayesian optimization, and online learning. Dr. Sadasivam will also walk through applications of these techniques in the SOC design context.

Characterization and leverage of design intent: One of the keys to fully automating the full design flow is to build technology to characterize design intent and to map it to physical design decisions at the chip, package and board levels. The key technologies to making this work include machine learning, analytics, and visualization algorithms. In this part of the tutorial, Dr. David White of Cadence will review some of the critical algorithms and visualization tools, as well as explore the available synergies between the EDA and design communities regarding use models that facilitate intent-driven design and simulation.

Data for learning: Automation and machine learning must broadly advance in two directions: (1) modeling and prediction of downstream flow outcomes (e.g., routing success, hold buffer insertion, post-timing closure block area) to avoid loops in the flow, and to provide optimization objectives at early flow stages; and (2) modeling of systematic discrepancies between approximate analyses (PEX, STA, etc.) and "signoff-quality" analyses, to reduce analysis errors that must be covered by design guardbands.

Prof. Andrew Kahng of UCSD will present a roadmap along which the EDA and IC design communities can progress in these directions. Crucially, the design, EDA and research communities must share responsibility for overcoming the "small, expensive data" challenge that hampers development of machine learning models for IC design. A standard methodology for "metrics" collection during the design process, as a prerequisite to development of machine learning models, will be described along with recent example experiences and use cases.

As time permits, the three tutorial presenters will add discussion on further topics such as (1) examples of machine learning infrastructure deployed by design organizations; (2) collaborative working models between EDA vendors and customers; and (3) leverage of open-source code and elastic cloud resources.

Tutorial-3 Monday, January 21, 9:30 - 12:30@Room Venus

Energy-Efficient Processing and Machine Learning at the Edge: from Sensing to Sensemaking

Organizer:

Massimo Alioto (National University of Singapore)

Speaker:

Massimo Alioto (National University of Singapore)

Tutorial Outline:

The Internet of Things (IoT) is now taking off as new technology wave in the semiconductor industry. The IoT is currently posing several challenges at its edge, in view of the strict requirements in terms of miniaturization, cost and lifetime of the distributed sensors ("IoT nodes") that constitute its physical interface. Being relatively incompressible, the large wireless power associated with radios is generally mitigated by making IoT nodes smarter, hence reducing communications with the cloud. To retain the advantages of pushing significant processing into the IoT nodes, ultra-low energy processing needs to be achieved by leveraging multiple design dimensions, ranging from energy-performance scaling (e.g., wide voltage scaling), to energy-quality scaling (e.g., adjustable accuracy), and application specific accelerators for data sensemaking (e.g., machine learning engines).

In this tutorial, a survey of fresh ideas and recent techniques to design ultra-low energy circuits for in-node processing in IoT applications is presented. A preliminary analysis of the current status of the IoT and trends in the foreseeable future are introduced to understand the system constraints, and translate them into design specifications. Then, minimum-energy operation is discussed by introducing near-threshold CMOS logic circuits along with their unique properties and challenges, while debunking several wrong assumptions stemming from traditional above-threshold low-power common wisdom. Practical design guidelines are also provided for near-threshold standard cell libraries, clock networks, memories, and other aspects related to automated design. For the first time, a novel variation-aware design framework is presented to quickly estimate the typically large design margin imposed by process/voltage/temperature variations, and guide the design to reduce the design margin.

As crucial building block of IoT nodes with on-chip sensor data sensemaking, energy-efficient accelerators for machine learning are introduced, building on the above circuit-level techniques. As particularly important case, low-energy deep learning accelerators are discussed by highlighting the "big ideas" that are enabling the recent and very rapid improvements in energy efficiency. Concepts are exemplified by integrated prototypes from industry and academia.

Tutorial-4 Monday, January 21, 9:30 - 12:30@Room Mars

Design for Reliability in the Nano-CMOS Era: New Holistic Methodologies for Reliability Modeling and Optimization

Organizer:

Sheldon Tan (University of California, Riverside), **Hussam Amrouch** (Karlsruhe Institute of Technology)

Speakers:

Sheldon Tan (University of California, Riverside), **Hussam Amrouch** (Karlsruhe Institute of Technology)

Tutorial Outline:

Reliability has become a significant challenge for design of current nanometer integrated circuits (ICs). Long-term reliability degradation caused by aging effects are becoming limiting constraints in emerging computing and communication platforms due to increased failure rates from the continuous transistor scaling, increasing process variations and aggressive power reductions. Reliability problems will get worse as future chips will show signs of aging much faster than the previous generations. Despite aging occurs at the physical level, workloads at the system level play a major role in stimulating the underlying mechanisms of aging. Therefore, holistic solutions in which the physical effects are linked with and abstracted all the way up to the system level become necessary for mitigating the looming reliability crisis.

The motivation of this tutorial is to understand the newest research results in reliability from ground up in which both Bias Temperature Instability (BTI) and Electromigration (EM), which are the key aging mechanisms in transistors and interconnect wires, are jointly covered. Intended audiences are circuit- and system- level designers who investigate reliability aspects in embedded systems.

Talk 1: EM-Aware Design: from Physics to System Level
Speaker: Sheldon Tan

In this talk, we will present some of recent research works in my research lab (VSCLAB) at UC Riverside. First, we will review a recently proposed physics-based three-phase EM models for multi-segment interconnect wires, which consists of nucleation, incubation and growth phases to completely model the EM failure processes in typical copper damascene interconnects. The new EM model can predict more accurate EM failure behaviors for multi-segment wires such as interconnects with reservoir and sink segments. Second, we will present newly proposed fast aging acceleration techniques for efficient EM failure detections and validation of practical VLSI chips. We will present the novel configurable reservoir/sink-structured interconnect designs in which the current in the sink segment can be activated/deactivated dynamically during operation. In this way, the stress conditions of the interconnect wires can be increased and the lifetime of the wires can be reduced significantly. Afterwards, we will present the compact dynamic EM models for general multi-segment interconnect wires and voltage-based EM immortality check algorithm for general interconnect trees. Then we will present a fast 2D stress numerical analysis technique based on the Krylov subspace and finite difference time domain methods (FDTD) for general interconnect wires structure. The proposed numerical analysis method can lead to 100X speedup over the simple FDTD method and can be applied to any interconnect structures for all the EM wear-out phases. Last, not least, we will focus on the system level dynamic reliability management (DRM) techniques based on the newly proposed physics-based EM models. We will show several recent works of the EM-aware DRM for lifetime optimizations for dark-silicon, embedder/real-time systems and 3D ICs to improve the TSV reliability.

Talk2: Estimating and Optimizing BTI Effects: from Physics to System Level
Speaker: Hussam Amrouch

In this presentation, we will first demonstrate how we can bring aging awareness to existing EDA tool flows based on so-called degradation-aware cell libraries. We will show why these libraries are necessary not only to accurately estimate guardbands but to efficiently containing them. Then, we will show how these libraries can be used within the standard tool flows to quantify the impact of aging at the system level in the context of image processing. Afterwards, we will demonstrate how aging-induced timing errors can be converted into deterministic and controlled approximations instead. This enables designers to narrow or even remove guardbands through exploring application of approximate computing principles in the context of aging. Finally, we will demonstrate how the existing view of BTI needs to be updated. State of the art used to assume BTI as a long-term reliability degradation that needs months and years to appear. However, in the deep nano technology, BTI has shifted to a short-term reliability challenge. We will explain why embedded system designers need to take that into account when designing guardbands. Otherwise, reliability cannot be sustained at runtime. At the end of our presentation, we will distribute to attendees USB sticks, which contain our degradation-aware libraries. This will enable them to study BTI effects using existing commercial EDA tool flows.

Tutorial-5 Monday, January 21, 9:30 - 12:30@Room Mercury

Machine Learning in Test

Organizer:

Yu Huang (Mentor, A Siemens Business)

Speakers:

Yu Huang (Mentor, A Siemens Business)

Tutorial Outline:

Machine learning has become a very hot topic in recent years due to its successful application in diverse areas such as computer vision, natural language processing, and intelligent gaming. Exciting new applications, such as autonomous driving, robotics, and AI assisted medical diagnosis, continue to emerge on a regular basis. However, machine learning has still not made much headway in the area of IC testing, since most researchers are unfamiliar with the underlying theory and algorithms, and are unsure of how to apply these techniques in the test domain. We believe machine learning is a powerful and innovative new technology, and can make a significant difference in the area of testing in the near future. This tutorial will review the basics of machine learning, its applications in testing, and forecast future applications of machine learning in testing. It will include the following two parts that are presented in an interleaving manner around each topic:

In the first part, we will provide the background necessary to understand the applications of machine learning in testing. We will start by covering the basics of machine learning. We will also give a brief overview of deep learning. We will end by showing how easy it is to try using machine learning and deep learning models, thanks to powerful, free libraries. We will start by characterizing what machine learning is: its definition, supervised vs unsupervised learning, classification vs regression problems. We will then introduce the notion of an objective or loss function. Using examples, we will show how our intuition about probability naturally leads to maximum likelihood estimation. We will proceed to take a deeper dive into regression. We will start by looking at simple linear regression. We will describe polynomial regression and show how even a simple linear model can be used to obtain a non-linear prediction by leveraging higher level features - a theme which we will keep revisiting throughout the tutorial. This will lead us to one of the pitfalls of machine learning - overfitting. We will discuss two easy and practical ways to avoid overfitting: regularization and cross validation. Our next focus will be classification. We will talk about a popular classifier: Support Vector Machines (SVMs). We will introduce the kernel trick which transforms an SVM into a powerful classifier. We will discuss how the concept of maximum margin separation, which is the key concept underlying an SVM, can be extended to regression to obtain the Support Vector Regression algorithm. We will motivate Bayes Theorem using examples and make a brief foray into the world of conditional probability and Bayesian Inference. We will describe the extremely powerful framework of Probabilistic Graphical Models and show how Bayes Theorem is at its foundation. Next, we will spend some time on the hottest sub-field in machine learning: deep learning. We will start by describing neural networks. We will discuss the reasons why they were not popular or in much use till a few years ago. We will introduce deep learning and talk about the theoretical and practical breakthroughs that happened a decade earlier which led to its meteoric rise. We will look at examples where deep learning has been used effectively, and the challenges it Submitted to TTTC TTEP 2018 currently faces. We will also discuss how deep learning researchers are trying to overcome these challenges. To conclude this part, we will mention freely downloadable Python libraries and show some actual python code. We hope to drive home how easy it is to try traditional as well as state-of-the-art machine learning / deep learning models and algorithms.

In the second part of the tutorial, we will start by reviewing published work in testing, where machine learning algorithms are used to solve hard problems. These problems will encompass the following areas of testing:

1. Yield learning / root cause analysis

With decreasing feature sizes and increasing complexity of fabrication processes for manufacturing VLSI semiconductor devices, more systematic defects occur at the advanced technology nodes. Product yield ramp up is mostly determined by how fast systematic defects are identified and fixed. Given the large amount of time and resources needed for doing physical failure analysis (PFA), it is becoming infeasible to find systematic defects by doing PFA on a large number of failing devices. For this reason, volume diagnosis data mining, where we apply statistical and machine learning models to a collection of diagnosis reports, is being increasingly used for root cause identification. This greatly reduces the turnaround time and cost of systematic defect identification. The root cause information can be used to do yield analysis and provide guidance on how to improve yield. In addition, it can be used to reduce PFA cost by focusing on failing devices with systematic defects.

2. Diagnosis

If a defect can be modeled as a permanent fault, simulating the fault can help us identify the suspects. However, real defects on Silicon are very complicated, and might not be permanent. We will use scan chain failure diagnosis as an example, and focus on handling hard-to-model defect behaviors. We will explain a machine learning based diagnosis algorithm that was implemented in a commercial tool.

3. DFT planning

Various configuration choices are available for decompression and compaction hardware. Finding an optimal configuration is very tedious and time consuming if we use a brute force approach. Using machine learning, this problem can be solved efficiently and effectively. Next, we will discuss which characteristics of test, diagnosis, and DFT applications are deep-learning friendly, and which are not. We will also provide advice on how to select applications that might be solved effectively using deep learning. Finally, we will propose future research directions in the area of testing, where we think machine learning (especially deep learning) can make a big impact.

Tutorial-6 Monday, January 21, 14:00 - 17:00@Room Saturn

Recent Development and Future Perspective of Quantum Annealing

Organizer:

Shu Tanaka (Waseda University)

Speakers:

Shu Tanaka (Waseda University), **Yoshiki Matsuda** (Fixstars Corporation), **Kotaro Tanahashi** (Recruit Communications Co., Ltd.), **Yuya Seki** (National Institute of Advanced Industrial Science and Technology, Japan)

Tutorial Outline:

Quantum annealing is expected to be a promising calculation method to perform the combinatorial optimization efficiently, which is a kind of natural computing technology using quantum phenomena. Quantum annealing was proposed as an alternative heuristic algorithm of simulated annealing in the background of statistical physics. In the simulated annealing, we introduce the temperature and decrease it gradually, whereas in the quantum annealing we introduce a quantum effect and decrease it gradually. Based on the theoretical proposition of quantum annealing, the first commercial quantum annealing machine was released in 2011. After that, D-Wave has been developed step by step, that is, the number of qubits in D-Wave is doubling every two years. In addition, hardware development, middleware/software development, application search of quantum annealing and its cousin technologies have been done by quite a few research groups. In this tutorial, the theoretical background of quantum annealing will be shown. In addition, very recent development of hardware, middleware/software, and application search of quantum annealing will be explained.

(1) Recent Development and Future Perspective of Quantum Annealing

In this tutorial, historical review and theoretical background of quantum annealing will be given. In addition, the procedure of quantum annealing will be explained. When we perform combinatorial optimizations by using quantum annealing machines, we have to prepare the Ising model which is a theoretical model in statistical physics. The structure of Ising model corresponds to the cost function of combinatorial optimization. In the first part of this tutorial, I will show some examples of the mapping from typical combinatorial optimization problems to the Ising model.

In the second part of this tutorial, I will explain the details of quantum annealing hardware. In existing quantum annealing hardware, superconducting qubits are arranged, and we embed the Ising model which corresponds to the combinatorial optimization problem we want to solve.

In the third of this tutorial, I will show some remaining problems in quantum annealing and its related technologies.

(2) Tutorial of Ising computations for combinatorial optimization problems

There exists a significant difference between the architectures of logic and Ising calculations, especially for the programming styles. The architecture of the Ising machine is suitable for describing the problem's "goals" directly, while the instruction and operands are constructed by "solutions" for the conventional procedural programming style. The problem's "goals" mean the relationships and preferable states among the Boolean variables.

The preferable state is expressed as the function which is called the energy (or cost/target) function for combinatorial optimization problems. For example, when we want to obtain the state "two variables are the same value" as a goal, we build the function with two variables inputs which takes the lowest (or highest) value when the goal, variables are the same value, is satisfied. The building of the energy function itself is the programming of the Ising machines.

In this tutorial, firstly we will show basic formulations of the energy function and the solving processes on the real Ising machines. Then, we will demonstrate our middleware between Ising machines and conventional programming languages, and we will explain some techniques to implement concrete examples of typical combinatorial optimizations to Ising machines. Finally, we will discuss further developments of Ising machines and software.

(3) Quantum Annealing for Machine Learning: Feature Selection and Sampling Applications

Optimizations play an essential role in many machine learning algorithms. However, some combinatorial optimization problems which belong to the NP-hard class cannot be solved efficiently by conventional optimization methods. Recently, quantum annealing (QA) has been shown to be effective for optimization problems in machine learning, such as feature selection or sampling problems.

In the first part of this tutorial, we will introduce a couple of feature selection algorithms optimized by quantum annealing machines. Feature selection, to find a subset of relevant features, is an important problem in machine learning both to speed up the training and to improve the generalization ability of the model. However, the number of combinations of the feature subset increases exponentially with the dimension size of the data. We introduce methods to formulate feature selection problem as Ising model to be solved by QA machines.

Next, we will discuss the applications of QA as a sampler. Some generative models in machine learning such as Boltzmann machines require samplings from the Boltzmann distributions. Since exact sampling from the distribution is intractable, we usually use heuristics such as Markov chain Monte Carlo methods (MCMC). Recent studies showed QA machines can accelerate the training of Boltzmann machines. We will introduce some potential applications of QA as a sampler.

(4) Beyond Transverse-Field Quantum Annealing

Performance improvement of quantum annealing (QA) is an important but unsolved issue. Although current implementations of QA use a uniform transverse field as driver Hamiltonian inducing quantum fluctuations, the transverse-field QA requires exponentially long time to solve certain problems. In this tutorial, recent approaches to improve the performance of QA are introduced.

Firstly, we explain how to estimate the performance of QA. In order to clarify discussion, we focus on quantum adiabatic computation (QAC) that is a procedure of quantum annealing satisfying the quantum adiabatic condition. From the statistical-mechanical point of view, quantum phase transition phenomenon is closely related to the performance of QA. In particular, quantum first order phase transition is symptom of the failure of QA.

Secondly, we introduce intractable problems for the transverse-field QA. Failure of QA is shown from both aspects of phase transition phenomenon and the quantum adiabatic condition.

Finally, we introduce successful attempts to improve the performance of QA. Except for special cases, QA requires exponentially long time to solve problems in which quantum first order phase transitions occur. Some methods to avoid the first order transitions are introduced. In addition, we explain a keyword "non-stoquasticity" related to the attempts.

Tutorial-7 Monday, January 21, 14:00 - 17:00@Room Uranus

Embedded Heterogeneous Computing: Architectural Landscape and Software Challenges

Organizer:

Tulika Mitra (National University of Singapore)

Speaker:

Tulika Mitra (National University of Singapore)

Tutorial Outline:

Heterogeneous computing, materialized in the form of multiprocessor system-on-chips (MPSoC) comprising of various processing elements such as general-purpose cores with differing characteristics, GPUs, DSPs, non-programmable accelerators (e.g., AI accelerators), and reconfigurable computing, are expected to dominate the current and the future embedded and mobile platform landscape. The heterogeneity enables a computational kernel with specific requirements to be paired with the processing element(s) ideally suited to perform that computation, leading to substantially improved performance and energy-efficiency. While heterogeneous computing is an attractive proposition in theory, considerable software support at all levels is essential to fully realize its promises. The system software needs to orchestrate the different on-chip compute resources in a synergistic manner with minimal engagement from the application developers. This tutorial will put the spotlight on the architectural and software perspective of embedded heterogeneous computing, especially in the context of popular emerging applications, such as artificial intelligence, 3D gaming, multimedia processing and analytics. The tutorial will introduce the technology trends driving heterogeneous computing, provide an overview of computationally divergent and performance heterogeneous multi-cores, and present recent research in architecture, compiler, and runtime support to fully realize the potential of heterogeneity towards high-performance, energy-efficient computing. The topics covered by the tutorial include:

- Technology trends behind heterogeneous computing
- Architectural landscape: performance heterogeneous CPU (e.g., ARM big.LITTLE), GPU, DSP, accelerators (e.g., Neural Processing Units), reconfigurable computing fabric
- Memory hierarchy for heterogeneous computing
- Software programmability challenges
- Application scheduling on heterogeneous computing systems
- Power and thermal Management for heterogeneous computing systems

Tutorial-8 Monday, January 21, 14:00 - 17:00@Room Venus

Smart Image Sensor Systems

Organizers:

Marilyn Wolf (Georgia Institute of Technology), **Saibal Mukhopodhyay** (Georgia Institute of Technology)

Speakers:

Marilyn Wolf (Georgia Institute of Technology), **Saibal Mukhopodhyay** (Georgia Institute of Technology)

Tutorial Outline:

The tutorial will cover:

- Fundamentals of computer vision applications: detection, recognition, tracking.
- Computer vision methods: feature extraction algorithms, neural networks and machine learning.
- Algorithm/architecture co-design.
- Analog mixed-signal smart sensors.
- 3D smart sensor technology.

The tutorial will be organized into two sections. The first section on computer vision methods and design. Computer vision algorithms operate at several levels of abstraction from pixels through objects and motion. Feature extraction, clustering, classification, optical flow, and prediction are all important tools of computer vision. A variety of algorithms including convolutional neural networks (CNNs), Bayesian models, and numerical methods are used. Algorithm/architecture co-design is critical to the design of real-time embedded computer vision systems to take into account requirements on image resolution and frame rate, classification accuracy, and platform architectures.

The second section will focus on on smart sensor architectures and systems. After reviewing the basics of CMOS APS image sensor design, the talk will discuss several approaches to integrated smart sensors. 3D smart sensors use back-side illuminated (BSI) sensors with front side connections to analog/digital conversion, memory, and processing. 3D architectures provide very high bandwidth to both the sensor and to memory. Computational architectures are fine-grained and support MIMD computation. These architectures support both high bandwidth to processors and memory as well as low latency. Thermal behavior must be carefully managed to avoid degrading both computational performance and image noise. Analog and digital techniques can be combined to provide low latency and low power.

Tutorial-9 Monday, January 21, 14:00 - 17:00@Room Mars

Machine Learning for Reliability of ICs and Systems

Organizer:

Mehdi B. Tahoori (Karlsruhe Institute of Technology)

Speakers:

Mehdi B. Tahoori (Karlsruhe Institute of Technology), **Krishnendu Chakrabarty** (Duke University)

Tutorial Outline:

With increasing the complexity of digital systems and the use of advanced nanoscale technology nodes, various process and runtime variabilities threaten the correct operation of these systems. The interdependence of these reliability detractors and their dependencies to circuit structure as well as running workloads makes it very hard to derive simple deterministic models to analyze and target them. As a result, machine learning techniques can be used to extract useful information which can be used to effectively monitor and improve the reliability of digital systems. These learning schemes are typically performed offline on large data sets in order to obtain various regression models which then are used during runtime operation to predict the health of the system and guide appropriate adaptation and countermeasure schemes. The purpose of this tutorial is to discuss and evaluate various learning schemes in order to analyze the reliability of the ICs and systems due to various runtime failure mechanisms which originate from process and runtime variabilities such as thermal and voltage fluctuations, device and interconnect aging mechanisms, as well as radiation-induced soft errors. The tutorial will also describe how time-series data analytics based on key performance indicators can be used to detect anomalies and predict failure in complex electronic systems. A comprehensive set of experimental results will be presented for data collected during 30 days of field operation from over 20 core routers. The tutorial will present a feature-categorization-based hybrid method to detect anomalies in features with different statistical characteristics. Changepoint detection based on maximum-likelihood analysis and health-status analysis will be described to distinguish changed normal scenarios from anomalous behavior.
Syllabus:

- Overview of important unreliability sources in advanced nano-scale technology nodes (10min)
- Modeling of unreliability sources (10 min). The dependency of unreliability sources on different parameters such as, temperature, supply voltage and running workload. Why modeling is not enough for reliability prediction?
- Machine-learning based monitoring of ICs (45 min)
  - Monitoring Aging effect: Employing machine learning to find a small set of so called Representative Critical Gates (RCG) or Representative Timing-critical flip-flops (RTFF) the workload of which is correlated with the degradation of the entire circuit.
  - Monitoring Soft error: Employing machine learning to predict the soft-error vulnerability of circuit/memory based on monitoring the signal probabilities (SPs) of a small set of flip-flops.
  - Monitoring Voltage droop: Employing machine learning to predict voltage droop and its effect on circuit timing based on monitoring a sequence of circuit inputs.
- Learning-based adaptation and mitigation techniques of ICs (45 min). Using proactive monitoring and approaches the reliability can be predicted before an error happens. This means that mitigation and adaptation actions can be applied in a timely manner. In this part, the adaptation and mitigation techniques are overviewed.
- Break, Q&A, and discussion (10 minutes)
- Architecture of core routers and sources of data (10 minutes)
  - Core routers as the internet backbone
  - Key performance indicators and type of data
  - Data collection and analysis framework
- Anomaly detection and time-series analysis (30 minutes)
  - Basic concepts in anomaly detection
  - Feature-categorization-based hybrid method to detect anomalies in features with different statistical characteristics.
- Changepoint detection to deal with data with time-varying statistical features (40 minutes)
  - Identification of changepoint windows
  - Goodness of fit: Negative log-likelihood, least-squares residuals, average scatter
- Health-status analysis (30 minutes)
  - Time-series symbolization
  - Identification of local patterns and global patterns
  - Hierarchical agglomerative clustering
- Q&A, discussion, and wrap-up (10 minutes)

At a glance

Tuesday, January 22

	A (Room Saturn)	B (Room Uranus)	C (Room Venus)	D (Room Mars+Mercury)
9:00	**1K Opening & Keynote I** (Miraikan Hall)			
10:30	Coffee Break			
10:45	1A: University Design Contest	1B: Real-time Embedded Software	1C: Hardware and System Security	1D: Thermal- and Power-Aware Design and Optimization
12:00	Lunch Break / **University Design Contest Poster Discussion** (Room Jupiter)			
13:30	2A: **(Special Session)** Reverse Engineering: growing more mature - and facing powerful countermeasures	2B: All about PIM	2C: Design for Reliability	2D: New Advances in Emerging Computing Paradigms
15:35	Coffee Break			
15:55	3A: **(Special Session)** Design, testing, and fault tolerance of Neuromorphic systems	3B: Memory-Centric Design and Synthesis	3C: Efficient Modeling of Analog, Mixed Signal and Arithmetic Circuits	3D: Logic and Precision Optimization for Neural Network Designs
18:00				
20:00	ACM SIGDA Student Research Forum at ASP-DAC 2019 (Room Jupiter)			

Wednesday, January 23

	A (Room Saturn)	B (Room Uranus)	C (Room Venus)	D (Room Mars+Mercury)
9:00	**2K Keynote II** (Miraikan Hall)			
10:00	Coffee Break			
10:20	4A: **(Special Session)** Modern Mask Optimization: From Shallow To Deep Learning	4B: System Level Modelling Methods I	4C: Testing and Design for Security	4D: Network-Centric Design and System
12:00	Lunch Break / **Supporters' Session** (Miraikan Hall)			
13:50	5A: **(Designers' Forum)** Robotics: From System Design to Application	5B: Advanced Memory Systems	5C: Learning: Make Patterning Light and Right	5D: Design and CAD for Emerging Memories
15:05	Coffee Break			
15:25	6A: **(Designers' Forum)** Advanced Imaging Technologies and Applications	6B: Optimized Training for Neural Networks	6C: New Trends in Biochips	6D: Power-efficient Machine Learning Hardware Design
18:30				
20:30	**Banquet** (Hilton Tokyo Odaiba, "Orion")			

Thursday, January 24

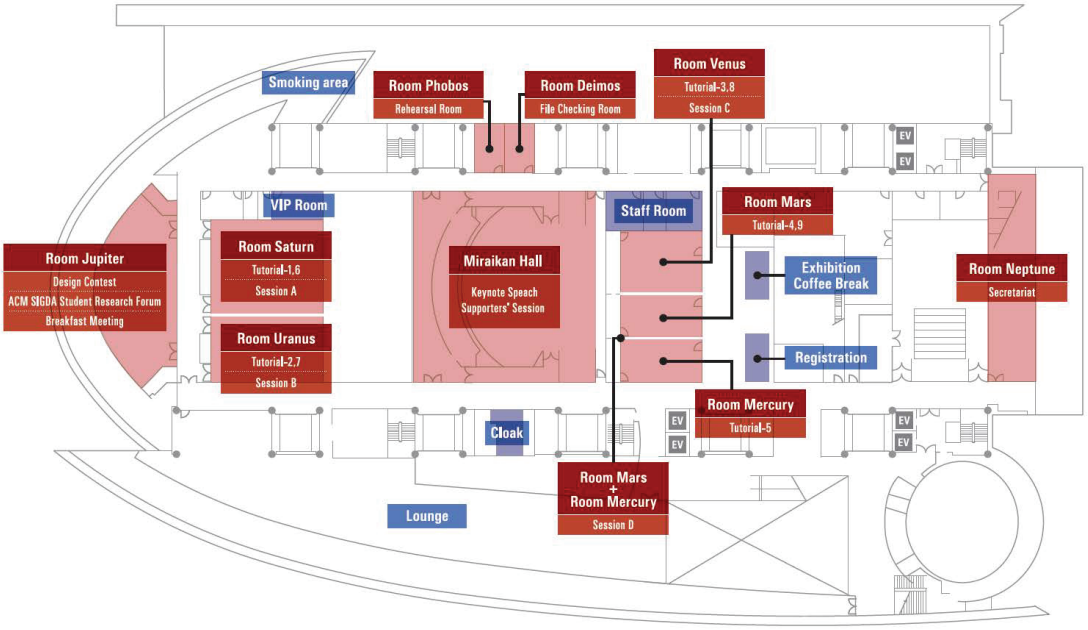
	A (Room Saturn)	B (Room Uranus)	C (Room Venus)	D (Room Mars+Mercury)
9:00	**3K Keynote III** (Miraikan Hall)			
10:00	Coffee Break			
10:20	7A: **(Special Session)** Security of Machine Learning and Machine Learning for Security: Progress and Challenges for Secure, Machine Intelligent Mobile Systems	7B: System Level Modelling Methods II	7C: Placement	7D: Algorithms and Architectures for Emerging Applications
12:00	Lunch Break			
13:15	8A: **(Designers' Forum)** Emerging Technologies for Tokyo Olympic 2020	8B: Embedded Software for Parallel Architecture	8C: Machine Learning and Hardware Security	8D: Memory Architecture for Efficient Neural Network Computing
14:30	Coffee Break			
14:50	9A: **(Designers' Forum)** Beyond the Virtual Reality World	9B: Logic-Level Security and Synthesis	9C: Analysis and Algorithms for Digital Design Verification	9D: FPGA and Optics-Based Neural Network Designs
16:05	Coffee Break			
16:25	10A: **(Special Session)** The Resurgence of Reconfigurable Computing in the Post Moore Era	10B: Hardware Acceleration	10C: Routing	
17:40				

Room Assignment

Room Assignment

Location	Event
Lobby	Registration, Information Desk, Supporter's Exhibition, and Coffee Break
Cloak	Cloak
Miraikan Hall	Opening, Keynotes I,II,III, and Supporter's Session
Room Saturn	Session A, Tutorials 1,6, and University Design Contest
Room Uranus	Session B and Tutorials 2,7
Room Venus	Session C and Tutorials 3,8
Room Mars	Session D and Tutorials 4,9
Room Mercury	Session D and Tutorial 5
Room Jupiter	Speaker's Breakfast, Poster Discussion, and ACM SIGDA Student Research Forum
Room Phobos	Rehearsal Room
Room Deimos	File Checking Room
Hilton Tokyo Odaiba, Room Orion (1F)	Banquet

Floor Map of Miraikan 7F:



Area Map for Miraikan:

Keynote Addresses

Keynote I

Tuesday, January 22, 9:00-10:30

"Development Trend of Artificial Intelligence Technology and its Application in the Field of Robotics"

Prof. Tao Zhang
Tsinghua University

In recent years, artificial intelligence has advanced remarkably, and this has brought various robot systems to a more highly advanced level as well. Meanwhile, the development of robot technology can significantly promote innovations in artificial intelligence technologies. This talk will introduce the development trends of artificial intelligence technologies by summarizing the main achievements in each technological field. Furthermore, it will enumerate the applications of artificial intelligent technologies in various robot systems, such as unmanned vehicles, unmanned aerial vehicles, service robots, space robots, marine robots, et al. We hope our viewpoints and predictions will be actually realized in the near future and we also believe that the world will be changed for the better and human life will be improved by means of artificial intelligent technology and its application in the field of robotics.

Keynote II

Wednesday, January 23, 9:00-10:00

"Post-K: A Game-changing Supercomputer with Groundbreaking A64fx High Performance Arm Processor"

Dr. Satoshi Matsuoka
RIKEN

The first would be exascale supercomputer in the world, the "Post-K", is being co-designed by Riken-CCS and Fujitsu in collaboration with the entire HPC community in Japan. The heart of Post-K is the groundbreaking Fujitsu A64fx processor which will sit at the pinnacle of billions of ARM processors manufactured every year, and will likely best competing CPUs by significant margins for HPC and other related workloads such as Big Data and AI, as well as CAE/EDA. Not only high in FLOPS with worldfs first implementation of wide-vector ARM SVE standard, but also the chip will likely to be the first general-purpose CPU to accommodate high bandwidth on-package HBM2 memory, coupled with streaming-friendly memory controllers and cache hierarchy for nearly a Terabyte of memory bandwidth. Such features will accelerate CAE workloads to unprecedented performance levels in platforms from supercomputers to workstations while being fully compliant to broad and open software ecosystem.

Keynote III

Thursday, January 24, 9:00-10:00

“Hardware and Software Security Technologies to Enable Future Connected Cars”

Dr. Yasuhisa Shimazaki
Renesas Electronics

In coming autonomous-driving era, automobiles and many kinds of facilities will be connected each other to provide safe, comfortable and efficient driving environment for drivers. Communication between a vehicle and cloud, for example, is used to obtain traffic information, to deliver driver-centric applications, to maintain automotive condition by monitoring and analyzing various sensing data obtained around the vehicle and so on and so forth. This means, however, we need to pay much attention to cyber security in automotive system. Actually, a remote attack on a running car through cellular network was demonstrated in 2015, resulting in 1.4 million recalls. In order to address this issue, MCUs used in an automobile need to have some sort of security measures which protect themselves and their communication channels effectively and efficiently. In this presentation, basic security technology will firstly be introduced, and then actual implementation of hardware and software security technique will be shown. The presentation will also cover standardization trend in automotive security.

Remark: The presenter of each paper is marked with "*".

1K Opening & Keynote I

Time: 9:00 - 10:30, Tuesday, January 22, 2019
Location: Miraikan Hall
Chair: Toshiyuki Shibuya (Fujitsu Labs., Japan)

1K-1 (Time: 9:30 - 10:30)
(Keynote Address) Development trend of artificial intelligence technology and its application in the field of robotics
Tao Zhang (Tsinghua Univ., China)

1A University Design Contest

Time: 10:45 - 12:00, Tuesday, January 22, 2019
Location: Room Saturn
Chairs: Kousuke Miyaji (Shinshu Univ., Japan), Akira Tsuchiya (Univ. of Shiga Prefecture, Japan)

1A-1 (Time: 10:45 - 10:48)
A Wide Conversion Ratio, 92.8% Efficiency, 3-Level Buck Converter with Adaptive On/Off-Time Control and Shared Charge Pump Intermediate Voltage Regulator
*Kousuke Miyaji, Yuki Karasawa, Takanobu Fukuoka (Shinshu Univ., Japan)

1A-2 (Time: 10:48 - 10:51)
A Three-Dimensional Millimeter-Wave Frequency-Shift Based CMOS Biosensor using Vertically Stacked Spiral Inductors in LC Oscillators
*Maya Matsunaga, Taiki Nakanishi, Atsuki Kobayashi (Nagoya Univ., Japan), Kiichi Niitsu (Nagoya Univ./JST PRESTO, Japan)

1A-3 (Time: 10:51 - 10:54)
Design of 385 x 385 μm^2 0.165V 270pW Fully-Integrated Supply-Modulated OOK Transmitter in 65nm CMOS for Glasses-Free, Self-Powered, and Fuel-Cell-Embedded Continuous Glucose Monitoring Contact Lens
*Kenya Hayashi, Shigeki Arata, Ge Xu, Shunya Murakami, Cong Dang Bui, Takuyoshi Doike, Maya Matsunaga, Atsuki Kobayashi (Nagoya Univ., Japan), Kiichi Niitsu (Nagoya Univ./JST PRESTO, Japan)

1A-4 (Time: 10:54 - 10:57)
2D Optical Imaging Using Photosystem I Photosensor Platform with 32×32 CMOS Biosensor Array
*Kiichi Niitsu (Nagoya Univ./JST PRESTO, Japan), Taichi Sakabe (Nagoya Univ., Japan), Mariko Miyachi, Yoshinori Yamanoi, Hiroshi Nishihara (Univ. of Tokyo, Japan), Tatsuya Tomo (Tokyo Univ. of Science, Japan), Kazuo Nakazato (Nagoya Univ., Japan)

1A-5 (Time: 10:57 - 11:00)
Design of Gate-Leakage-Based Timer Using an Amplifier-Less Replica-Bias Switching Technique in 55-nm DDC CMOS
*Atsuki Kobayashi, Yuya Nishio, Kenya Hayashi, Shigeki Arata (Nagoya Univ., Japan), Kiichi Niitsu (Nagoya Univ./JST PRESTO, Japan)

1A-6 (Time: 11:00 - 11:03)
A Low-Voltage CMOS Electrophoresis IC Using Electroless Gold Plating for Small-Form-Factor Biomolecule Manipulation
*Kiichi Niitsu (Nagoya Univ./JST PRESTO, Japan), Yuuki Yamaji, Atsuki Kobayashi, Kazuo Nakazato (Nagoya Univ., Japan)

1A-7 (Time: 11:03 - 11:06)
A Low-Voltage Low-Power Multi-Channel Neural Interface IC Using Level-Shifted Feedback Technology
*Liangjian Lyu, Yu Wang (Fudan Univ., China), Chixiao Chen, C. -J. Richard Shi (Univ. of Washington, U.S.A.)

1A-8 (Time: 11:06 - 11:09)
Development of a High Stability, Low Standby Power Six-Transistor CMOS SRAM Employing a Single Power Supply
*Nobuaki Kobayashi (Nihon Univ., Japan), Tadayoshi Enomoto (Chuo Univ., Japan)

1A-9 (Time: 11:09 - 11:12)
Design of Heterogeneously-integrated Memory System with Storage Class Memories and NAND Flash Memories
*Chihiro Matsui, Ken Takeuchi (Chuo Univ., Japan)

1A-10 (Time: 11:12 - 11:15)
A 65-nm CMOS Fully-Integrated Circulating Tumor Cell and Exosome Analyzer Using an On-Chip Vector Network Analyzer and a Transmission-Line-Based Detection Window
Taiki Nakanishi, Maya Matsunaga, Shunya Murakami, Atsuki Kobayashi (Nagoya Univ., Japan), *Kiichi Niitsu (Nagoya Univ./JST PRESTO, Japan)

1A-11 (Time: 11:15 - 11:18)
Low Standby Power CMOS Delay Flip-Flop with Data Retention Capability
*Nobuaki Kobayashi (Nihon Univ., Japan), Tadayoshi Enomoto (Chuo Univ., Japan)

1A-12 (Time: 11:18 - 11:21)
Accelerate Pattern Recognition for Cyber Security Analysis
*Mohammad Tahghighi, Wei Zhang (Hong Kong Univ. of Science and Tech., Hong Kong)

1A-13 (Time: 11:21 - 11:24)
FPGA Laboratory System supporting Power Measurement for Low-Power Digital Design
Marco Winzker, *Andrea Schwandt (Bonn-Rhein-Sieg Univ., Germany)

1B Real-time Embedded Software
Time: 10:45 - 12:00, Tuesday, January 22, 2019
Location: Room Uranus
Chairs: Zhaoyan Shen (Shandong Univ.), Zebo Peng (Linköping Univ., Sweden)

1B-1 (Time: 10:45 - 11:10)
Towards Limiting the Impact of Timing Anomalies in Complex Real-Time Processors
*Pedro Benedicte (Barcelona Supercomputing Center and Univ. Politècnica de Catalunya, Spain), Jaume Abella, Carles Hernandez, Enrico Mezzetti (Barcelona Supercomputing Center, Spain), Francisco J. Cazorla (Barcelona Supercomputing Center and IIIA-CSIC, Spain)

1B-2 (Time: 11:10 - 11:35)
SeRoHAL: Generation of Selectively Robust Hardware Abstraction Layers for Efficient Protection of Mixed-criticality Systems
*Petra R. Kleeberger, Juana Rivera, Daniel Mueller-Gritschneder, Ulf Schlichtmann (Tech. Univ. München, Germany)

1B-3 (Time: 11:35 - 12:00)
Partitioned and Overhead-Aware Scheduling of Mixed-Criticality Real-Time Systems
*Yuanbin Zhou, Soheil Samii, Petru Eles, Zebo Peng (Linköping Univ., Sweden)

1C Hardware and System Security
Time: 10:45 - 12:00, Tuesday, January 22, 2019
Location: Room Venus
Chairs: Ray C.C. Cheung (City Univ. of Hong Kong, Hong Kong), Hai Zhou (Northwestern Univ., U.S.A.)

1C-1 (Time: 10:45 - 11:10)
Layout Recognition Attacks on Split Manufacturing
*Wenbin Xu, Lang Feng, Jeyavijayan Rajendran, Jiang Hu (Texas A&M Univ., U.S.A.)

1C-2 (Time: 11:10 - 11:35)
Execution of Provably Secure Assays on MEDA Biochips to Thwart Attacks
*Tung-Che Liang (Duke Univ., U.S.A.), Mohammed Shayan (New York Univ., U.S.A.), Krishnendu Chakrabarty (Duke Univ., U.S.A.), Ramesh Karri (New York Univ., U.S.A.)

1C-3 (Time: 11:35 - 12:00)
TAD: Time Side-Channel Attack Defense of Obfuscated Source Code
*Alexander Fell, Hung Thinh Pham, Siew Kei Lam (Nanyang Technological Univ., Singapore)

1D Thermal- and Power-Aware Design and Optimization
Time: 10:45 - 12:00, Tuesday, January 22, 2019
Location: Room Mars+Room Mercury
Chairs: Hussam Amrouch (Karlsruhe Inst. of Tech. (KIT), Germany), Jiang Hu (Texas A&M)

1D-1 (Time: 10:45 - 11:10)
Leakage-Aware Thermal Management for Multi-Core Systems Using Piecewise Linear Model Based Predictive Control
Xingxing Guo, *Hai Wang, Chi Zhang, He Tang, Yuan Yuan (Univ. of Electronic Science and Tech. of China, China)

1D-2 (Time: 11:10 - 11:35)
Multi-Angle Bended Heat Pipe Design Using X-Architecture Routing with Dynamic Thermal Weight on Mobile Devices
Hsuan-Hsuan Hsiao, *Hong-Wen Chiou, Yu-Min Lee (National Chiao Tung Univ., Taiwan)

1D-3 (Time: 11:35 - 12:00)
Fully-automated Synthesis of Power Management Controllers from UPF
*Dustin Peterson, Oliver Bringmann (Univ. of Tuebingen, Germany)

2A (SS-1) Reverse Engineering: growing more mature - and facing powerful countermeasures

Time: 13:30 - 15:35, Tuesday, January 22, 2019
Location: Room Saturn
Chair: Naehyuck Chang (KAIST, Republic of Korea)

2A-1 (Time: 13:30 - 13:55)
(Invited Paper) Integrated Flow for Reverse Engineering of Nanoscale Technologies
*Bernhard Lippmann, Aayush Singla, Niklas Unverricht, Peter Egger, Anja Dübotzky, Michael Werner (Infineon Technologies AG, Germany), Horst Gieser (Fraunhofer EMFT, Germany), Martin Rasche, Oliver Kellermann (Raith GmbH, Germany), Helmut Gräb (TUM, Germany)

2A-2 (Time: 13:55 - 14:20)
(Invited Paper) NETA: When IP Fails, Secrets Leak
Travis Meade, Jason Portillo, Shaojie Zhang (Univ. of Central Florida, U.S.A.), *Yier Jin (Univ. of Florida, U.S.A.)

2A-3 (Time: 14:20 - 14:45)
(Invited Paper) Machine Learning and Structural Characteristics for Reverse Engineering
Johanna Baehr, Alessandro Bernardini, Georg Sigl, *Ulf Schlichtmann (Tech. Univ. of Munich, Germany)

2A-4 (Time: 14:45 - 15:10)
(Invited Paper) Towards Cognitive Obfuscation: Impeding Hardware Reverse Engineering Based on Psychological Insights
*Carina Wiesen, Steffen Becker, Nils Albartus, Max Hoffmann, Sebastian Wallat, Marc Fyrbiak, Nikol Rummel, Christof Paar (Ruhr Univ. Bochum, Germany)

2A-5 (Time: 15:10 - 15:35)
(Invited Paper) Insights to the Mind of a Trojan Designer: The Challenge to Integrate a Trojan in the Bitstream
*Maik Ender, Paul Martin Knopp, Christof Paar, Pawel Swierczynski, Sebastian Wallert, Matthias Wilhelm (Ruhr Univ. Bochum, Germany)

2B All about PIM

Time: 13:30 - 15:35, Tuesday, January 22, 2019
Location: Room Uranus
Chairs: Guangyu Sun (Peking Univ., China), Wanli Chang (Univ. of York, U.K.)

2B-1 (Time: 13:30 - 13:55)
GraphSAR: A Sparsity-Aware Processing-in-Memory Architecture for Large-Scale Graph Processing on ReRAMs
*Guohao Dai (Tsinghua Univ., China), Tianhao Huang (Massachusetts Inst. of Tech., U.S.A.), Yu Wang, Huazhong Yang (Tsinghua Univ., China), John Wawrzynek (Univ. of California, Berkeley, U.S.A.)

2B-2 (Time: 13:55 - 14:20)
ParaPIM: A Parallel Processing-in-Memory Accelerator for Binary-Weight Deep Neural Networks
Shaahin Angizi, Zhezhi He, *Deliang Fan (Univ. of Central Florida, U.S.A.)

2B-3 (Time: 14:20 - 14:45)
CompRRAE: RRAM-based Convolutional Neural Network Accelerator with Reduced Computations through a Runtime Activation Estimation
*Xizi Chen, Jingyang Zhu, Jingbo Jiang, Chi-Ying Tsui (Hong Kong Univ. of Science and Tech., Hong Kong)

2B-4 (Time: 14:45 - 15:10)
CuckooPIM: An Efficient and Less-blocking Coherence Mechanism for Processing-in-Memory Systems
*Sheng Xu, Xiaoming Chen, Ying Wang, Yinhe Han, Xiaowei Li (Chinese Academy of Sciences, China)

2B-5 (Time: 15:10 - 15:35)
AERIS: Area/Energy-Efficient 1T2R ReRAM Based Processing-in-Memory Neural Network System-on-a-Chip
*Jinshan Yue, Yongpan Liu, Fang Su (Tsinghua Univ., China), Shuangchen Li (Univ. of California, Santa Barbara, U.S.A.), Zhe Yuan, Zhibo Wang, Wenyu Sun, Xueqing Li, Huazhong Yang (Tsinghua Univ., China)

2C Design for Reliability

Time: 13:30 - 15:35, Tuesday, January 22, 2019
Location: Room Venus
Chairs: Shigeki Nojima (Toshiba Memory, Japan), Bei Yu (Chinese Univ. of Hong Kong, Hong Kong)

2C-1 (Time: 13:30 - 13:55)
IR-ATA: IR Annotated Timing Analysis, A Flow for Closing the LoopBetween PDN design, IR Analysis & Timing Closure
Ashkan Vakil, Houman Homayoun, *Avesta Sasan (George Mason Univ., U.S.A.)

2C-2 (Time: 13:55 - 14:20)
Learning-Based Prediction of Package Power Delivery Network Quality
Yi Cao (Qualcomm Technologies, U.S.A.), *Andrew B. Kahng (UC San Diego, U.S.A.), Joseph Li, Abinash Roy, Vaishnav Srinivas (Qualcomm Technologies, U.S.A.), Bangqi Xu (UC San Diego, U.S.A.)

2C-3 (Time: 14:20 - 14:45)
Tackling Signal Electromigration with Learning-Based Detection and Multistage Mitigation
*Wei Ye, Mohamed Baker Alawieh, Yibo Lin, David Z. Pan (Univ. of Texas, Austin, U.S.A.)

2C-4 (Time: 14:45 - 15:10)
ROBIN: Incremental Oblique Interleaved ECC for Reliability Improvement in STT-MRAM Caches
*Elham Cheshmikhani (Sharif Univ. of Tech., Iran), Hamed Farbeh (Amirkabir Univ. of Tech., Iran), Hossein Asadi (Sharif Univ. of Tech., Iran)

2C-5 (Time: 15:10 - 15:35)
Aging-aware Chip Health Prediction Adopting an Innovative Monitoring Strategy
Yun-Ting Wang (National Tsing Hua Univ., Taiwan), Kai-Chiang Wu (National Chiao Tung Univ., Taiwan), *Chung-Han Chou (Feng Chia Univ., Taiwan), Shih-Chieh Chang (National Tsing Hua Univ., Taiwan)

2D New Advances in Emerging Computing Paradigms
Time: 13:30 - 15:35, Tuesday, January 22, 2019
Location: Room Mars+Room Mercury
Chairs: Shigeru Yamashita (Ritsumeikan Univ., Japan), Xiaoming Chen (Chinese Academy of Sciences, China)

2D-1 (Time: 13:30 - 13:55)
Compiling SU(4) Quantum Circuits to IBM QX Architectures
*Alwin Zulehner, Robert Wille (Johannes Kepler Univ. Linz, Austria)

2D-2 (Time: 13:55 - 14:20)
Quantum Circuit Compilers Using Gate Commutation Rules
*Toshinari Itoko, Rudy Raymond, Takashi Imamichi, Atsushi Matsuo (IBM Research, Japan), Andrew W. Cross (IBM Research, U.S.A.)

2D-3 (Time: 14:20 - 14:45)
Scalable Design for Field-coupled Nanocomputing Circuits
*Marcel Walter (Univ. of Bremen, Germany), Robert Wille (Johannes Kepler Univ. Linz, Austria), Frank Sill Torres (DFKI GmbH, Germany), Daniel Groβe, Rolf Drechsler (Univ. of Bremen, Germany)

2D-4 (Time: 14:45 - 15:10)
BDD-based Synthesis of Optical Logic Circuits Exploiting Wavelenngth Division Multiplexing
*Ryosuke Matsuo, Jun Shiomi, Tohru Ishihara, Hidetoshi Onodera (Kyoto Univ., Japan), Akihiko Shinya, Masaya Notomi (NTT, Japan)

2D-5 (Time: 15:10 - 15:35)
Hybrid Binary-Unary Hardware Accelerator
S. Rasoul Faraji, *Kia Bazargan (Univ. of Minnesota, U.S.A.)

3A (SS-2) Design, testing, and fault tolerance of Neuromorphic systems
Time: 15:55 - 17:10, Tuesday, January 22, 2019
Location: Room Saturn
Chair: Chenchen Liu (Clarkson Univ., U.S.A.)

3A-1 (Time: 15:55 - 16:20)
(Invited Paper) Fault Tolerance in Neuromorphic Computing Systems
*Yu Wang (Tsinghua Univ., China), Mengyun Liu, Krishnendu Chakrabarty (Duke Univ., U.S.A.), Lixue Xia (Tsinghua Univ., China)

3A-2 (Time: 16:20 - 16:45)
(Invited Paper) Build Reliable and Efficient Neuromorphic Design with Memristor Technology
Bing Li, Bonan Yan (Duke Univ., U.S.A.), Chenchen Liu (Clarkson Univ., U.S.A.), *Hai Li (Duke Univ., U.S.A.)

3A-3 (Time: 16:45 - 17:10)
(Invited Paper) Reliable In-Memory Neuromorphic Computing Using Spintronics
Christopher Muench, Rajendra Bishnoi, *Mehdi Tahoori (KIT, Germany)

3B Memory-Centric Design and Synthesis

Time: 15:55 - 17:10, Tuesday, January 22, 2019
Location: Room Uranus
Chairs: Shouyi Yin (Tsinghua Univ., China), Matthew Ziegler (IBM)

3B-1 (Time: 15:55 - 16:20)
A Staircase Structure for Scalable and Efficient Synthesis of Memristor-Aided Logic
*Alwin Zulehner (Johannes Kepler Univ. Linz, Austria), Kamalika Datta (National Inst. of Tech. Meghalaya, India), Indranil Sengupta (Indian Inst. of Tech. Kharagpur, India), Robert Wille (Johannes Kepler Univ. Linz, Austria)

3B-2 (Time: 16:20 - 16:45)
On-chip Memory Optimization for High-level Synthesis of Multi-dimensional Data on FPGA
Daewoo Kim, Sugil Lee, *Jongeun Lee (Ulsan National Inst. of Science and Tech., Republic of Korea)

3B-3 (Time: 16:45 - 17:10)
HUBPA: High Utilization Bidirectional Pipeline Architecture for Neuromorphic Computing
Houxiang Ji, *Li Jiang, Tianjian Li, Naifeng Jing, Jing Ke, Xiaoyao Liang (Shanghai Jiao Tong Univ., China)

3C Efficient Modeling of Analog, Mixed Signal and Arithmetic Circuits

Time: 15:55 - 17:10, Tuesday, January 22, 2019
Location: Room Venus
Chairs: Jun Tao (Fudan Univ., China), Shobha Vasudevan (Univ. of Illinois, Urbana-Champaign, U.S.A.)

3C-1 (Time: 15:55 - 16:20)
Efficient Sparsification of Dense Circuit Matrices in Model Order Reduction
*Charalampos Antoniadis, Nestor Evmorfopoulos, Georgios Stamoulis (Univ. of Thessaly, Greece)

3C-2 (Time: 16:20 - 16:45)
Spectral Approach to Verifying Non-linear Arithmetic Circuits
Cunxi Yu (EPFL, Switzerland), Tiankai Su, Atif Yasin, *Maciej Ciesielski (UMass Amherst, U.S.A.)

3C-3 (Time: 16:45 - 17:10)
S^2-PM: Semi-Supervised Learning for Efficient Performance Modeling of Analog and Mixed Signal Circuits
Mohamed Baker Alawieh, Xiyuan Tang, *David Z. Pan (Univ. of Texas, Austin, U.S.A.)

3D Logic and Precision Optimization for Neural Network Designs

Time: 15:55 - 17:10, Tuesday, January 22, 2019
Location: Room Mars+Room Mercury
Chairs: Massanori Muroyama (Tohoku Univ., Japan), Younghyun Kim (Univ. of Wisconsin, U.S.A.)

3D-1 (Time: 15:55 - 16:20)
Energy-Efficient, Low-Latency Realization of Neural Networks through Boolean Logic Minimization
Mahdi Nazemi, Ghasem Pasandi, *Massoud Pedram (USC, U.S.A.)

3D-2 (Time: 16:20 - 16:45)
Log-Quantized Stochastic Computing for Memory and Computation Efficient DNNs
*Hyeonuk Sim, Jongeun Lee (Ulsan National Inst. of Science and Tech., Republic of Korea)

3D-3 (Time: 16:45 - 17:10)
Cell Division: Weight Bit-Width Reduction Technique for Convolutional Neural Network Hardware Accelerators
*Hanmin Park, Kiyoung Choi (Seoul National Univ., Republic of Korea)

SRF ACM SIGDA Student Research Forum at ASP-DAC2019

Time: 18:00 - 20:00, Tuesday, January 22, 2019
Location: Room Jupiter
Chairs: Pi-Cheng Hsiu (Academic Sinica, Taiwan)
Hyung Gyu Lee (Daegu Univ., Korea)
Weichen Liu (Nangyang Technological Univ., Singapore)

SRF-1: New Views for Stochastic Computing: From Time-Encoding to Deterministic Processing
M. Hassan Najafi (University of Minnesota-Twin Cities)

SRF-2: A Multi-Phase Intellectual Property Core Watermarking Approach during Architectural Synthesis
Dipanjan Roy (Indian Institute of Technology Indore)

SRF-3: Automatic Design Environment using High-level Synthesis for Reconfigurable 3D Sound Processor
Saya Ohira (Nihon University)

SRF-4: VLSI Design for Manufacturability based on Dictionary Learning Framework
Hao Geng (The Chinese University of Hong Kong)

SRF-5: Computer-Aided Design for Quantum Computing
Alwin Zulehner (Johannes Kepler University Linz)

SRF-6: Enhancing VLSI Design for Manufacturability with Machine Learning Techniques
Haoyu Yang (The Chinese University of Hong Kong)

SRF-7: A Model-driven Framework with Assertion Based Verification (ABV) Support for Embedded Systems Design Automation
Muhammad Waseem Anwar (National University of Sciences and Technology)

SRF-8: Optimization of Multi-Target Sample Preparation On-Demand with Digital Microfluidic Biochips
Sudip Poddar (Indian Statistical Institute)

SRF-9: Clustering for Reduction of Power Consumption and Area on Post-Silicon Delay Tuning
Kota Muroi (The University of Aizu)

SRF-10: Task and Data Co-Allocation for MPSoCs with 3D-stacked Memories to Optimize Performance under Thermal Constraints
Chia-Yin Liu (National Chi Nan University)

SRF-11: The Accurate Power Consumption Model For Rotary UAVs
Dooyoung Hong (Korea Advanced Institute of Science and Technology)

SRF-12: Modulo 2^n+1 arithmetic based on signed-digit and binary number addition algorithm
Yuuki Suzuki (Gunma University)

SRF-13: A Data Transfer Optimization in Non-Binary to Binary Conversion Circuit in Non-Binary Cyclic ADC
Yuji Shindo (Tokyo City University)

SRF-14: A Decision Network Design for Efficient Semantic Segmentation Computation in Edge Computing
Xin-Yu Kuo (National Tsing Hua University)

2K Keynote II

Time: 9:00 - 10:00, Wednesday, January 23, 2019
Location: Miraikan Hall
Chair: Hidetoshi Onodera (Kyoto Univ., Japan)

2K-1 (Time: 9:00 - 10:00)

(Keynote Address) Post-K: A Game-changing Supercomputer with Groundbreaking A64fx High Performance Arm Processor

Satoshi Matsuoka (RIKEN, Japan)

4A (SS-3) Modern Mask Optimization: From Shallow To Deep Learning

Time: 10:20 - 12:00, Wednesday, January 23, 2019
Location: Room Saturn
Chairs: Evangeline F. Y. Young (Chinese Univ. of Hong Kong, Hong Kong), Atsushi Takahashi (Tokyo Inst. of Tech., Japan)

4A-1 (Time: 10:20 - 10:45)

(Invited Paper) LithoROC: Lithography Hotspot Detection with Explicit ROC Optimization

*Wei Ye, Yibo Lin, Meng Li, Qiang Liu, David Z. Pan (Univ. of Texas, Austin, U.S.A.)

4A-2 (Time: 10:45 - 11:10)

(Invited Paper) Detecting Multi-Layer Layout Hotspots with Adaptive Squish Patterns

*Haoyu Yang (Chinese Univ. of Hong Kong, Hong Kong), Piyush Pathak, Frank Gennari, Ya-Chieh Lai (Cadence Design Systems, U.S.A.), Bei Yu (Chinese Univ. of Hong Kong, Hong Kong)

4A-3 (Time: 11:10 - 11:35)

(Invited Paper) A Local Optimal Method on DSA Guiding Template Assignment with Redundant/Dummy Via Insertion

*Xingquan Li (Fuzhou Univ., China), Bei Yu (Chinese Univ. of Hong Kong, Hong Kong), Jianli Chen, Wenxing Zhu (Fuzhou Univ., China)

4A-4 (Time: 11:35 - 12:00)

(Invited Paper) Deep Learning-Based Framework for Comprehensive Mask Optimization

Bo-Yi Yu, *Yong Zhong, Shao-Yun Fang, Hung-Fei Kuo (National Taiwan Univ. of Science and Tech., Taiwan)

4B System Level Modelling Methods I

Time: 10:20 - 12:00, Wednesday, January 23, 2019
Location: Room Uranus
Chair: Sri Parameswaran (Univ. of New South Wales, Australia)

4B-1 (Time: 10:20 - 10:45)

AxDNN:Towards the Cross-layer Design of Approximate DNNs

*Yinghui Fan, Xiaoxi Wu, Jiying Dong, Zhi Qi (Southeast Univ., China)

4B-2 (Time: 10:45 - 11:10)

Simulate-the-hardware: Training Accurate Binarized Neural Networks for Low-Precision Neural Accelerators

*Jiajun Li (Univ. of Chinese Academy of Sciences/Chinese Academy of Sciences, China), Ying Wang (Chinese Academy of Sciences, China), Bosheng Liu (Univ. of Chinese Academy of Sciences/Chinese Academy of Sciences, China), Yinhe Han, Xiaowei Li (Chinese Academy of Sciences, China)

4B-3 (Time: 11:10 - 11:35)

An N-Way Group Association Architecture and Sparse Data Group Association Load Balancing Algorithm for Sparse CNN Accelerators

*Jingyu Wang, Zhe Yuan, Ruoyang Liu, Huazhong Yang, Yongpan Liu (Tsinghua Univ., China)

4B-4 (Time: 11:35 - 12:00)

Maximizing Power State Cross Coverage in Firmware-based Power Management

*Vladimir Herdt, Hoang M. Le (Univ. of Bremen, Germany), Daniel Groβe, Rolf Drechsler (Univ. of Bremen, DFKI GmbH, Germany)

4C Testing and Design for Security

Time: 10:20 - 12:00, Wednesday, January 23, 2019
Location: Room Venus
Chairs: Michihiro Shintani (NAIST, Japan), Kohei Miyase (Kyushu Inst. of Tech., Japan)

4C-1 (Time: 10:20 - 10:45)

Improving Scan Chain Diagnostic Accuracy Using Multi-Stage Artificial Neural Networks

Mason Chern, Shih-Wei Lee, *Shi-Yu Huang (National Tsing Hua Univ., Taiwan), Yu Huang, Gaurav Veda, Kun-Han Tsia, Wu-Tung Cheng (Mentor, A Siemens Business, U.S.A.)

4C-2 (Time: 10:45 - 11:10)
Testing Stuck-Open Faults of Priority Address Encoder in Content Addressable Memories
*Tsai-Ling Tsai, Jin-Fu Li (National Central Univ., Taiwan), Chun-Lung Hsu, Chi-Tien Sun (ITRI, Taiwan)

4C-3 (Time: 11:10 - 11:35)
ScanSAT: Unlocking Obfuscated Scan Chains
*Lilas Alrahis (Khalifa Univ., United Arab Emirates), Muhammad Yasin (Tandon school of engineering, New York university, U.S.A.), Hani Saleh, Baker Mohammad, Mahmoud Al-Qutayri (Khalifa Univ., United Arab Emirates), Ozgur Sinanoglu (New York Univ. Abu Dhabi, United Arab Emirates)

4C-4 (Time: 11:35 - 12:00)
CycSAT-Unresolvable Cyclic Logic Encryption Using Unreachable States
Amin Rezaei, You Li, Yuanqi Shen, Shuyu Kong, *Hai Zhou (Northwestern Univ., U.S.A.)

4D Network-Centric Design and System
Time: 10:20 - 12:00, Wednesday, January 23, 2019
Location: Room Mars+Room Mercury
Chairs: Keiji Kimura (Waseda Univ., Japan), Yaoyao Ye (Shanghai Jiao Tong Univ., China)

4D-1 (Time: 10:20 - 10:45)
Routing in Optical Network-on-Chip: Minimizing Contention with Guaranteed Thermal Reliability
*Mengquan Li (Chongqing Univ., China), Weichen Liu (Nanyang Technological Univ., Singapore), Lei Yang, Peng Chen, Duo Liu (Chongqing Univ., China), Nan Guan (Hong Kong Polytechnic Univ., Hong Kong)

4D-2 (Time: 10:45 - 11:10)
Bidirectional Tuning of Microring-Based Silicon Photonic Transceivers for Optimal Energy Efficiency
*Yuyang Wang (Univ. of California, Santa Barbara, U.S.A.), M. Ashkan Seyedi, Jared Hulme, Marco Fiorentino, Raymond G. Beausoleil (Hewlett Packard Labs, U.S.A.), Kwang-Ting Cheng (Hong Kong Univ. of Science and Tech., Hong Kong)

4D-3 (Time: 11:10 - 11:35)
Redeeming Chip-level Power Efficiency by Collaborative Management of the Computation and Communication
*Ning Lin, Hang Lu, Xin Wei, Xiaowei Li (Chinese Academy of Sciences/Univ. of Chinese Academy of Sciences, China)

4D-4 (Time: 11:35 - 12:00)
A High-Level Modeling and Simulation Approach Using Test-Driven Cellular Automata for Fast Performance Analysis of RTL NoC Designs
*Moon Gi Seok (Arizona State Univ., U.S.A.), Daejin Park (Kyungpook National Univ., Republic of Korea), Hessam S. Sarjoughian (Arizona State Univ., U.S.A.)

5A (DF-1) Robotics: From System Design to Application
Time: 13:50 - 15:05, Wednesday, January 23, 2019
Location: Room Saturn
Organizer: Koji Inoue (Kyushu Univ., Japan), Organizer/Chair: Yuji Ishikawa (Toshiba Device & Storage, Japan)

5A-1 (Time: 13:50 - 14:15)
(Designers' Forum) Computer-Aided Support System for Minimally Invasive Surgery Using 3D Organ Shape Models
Ken'ichi Morooka (Kyusyu Univ., Japan)

5A-2 (Time: 14:15 - 14:40)
(Designers' Forum) ROS and mROS: How to accelerate the development of robot systems and integrate embedded devices
Hideki Takase (Kyoto Univ./JST PRESTO, Japan)

5A-3 (Time: 14:40 - 15:05)
(Designers' Forum) Rapid Development of Robotics technology using Robot Contest and Open Collaboration
Masaki Yamamoto (AI Solution Center, Panasonic, Japan)

5B Advanced Memory Systems
Time: 13:50 - 15:05, Wednesday, January 23, 2019
Location: Room Uranus
Chairs: Jaehyun Park (Univ. of Ulsan, Republic of Korea), Chenchen Liu (Clarkson Univ.)

5B-1 (Time: 13:50 - 14:15)
A Sharing-Aware L1.5D Cache for Data Reuse in GPGPUs
*Jianfei Wang, Li Jiang, Jing Ke, Xiaoyao Liang, Naifeng Jing (Shanghai Jiao Tong Univ., China)

5B-2 (Time: 14:15 - 14:40)
NeuralHMC: An Efficient HMC-Based Accelerator for Deep Neural Networks
Chuhan Min (Univ. of Pittsburgh, U.S.A.), Jiachen Mao, Hai Li, *Yiran Chen (Duke Univ., U.S.A.)

5B-3 (Time: 14:40 - 15:05)
Boosting Chipkill Capability under Retention-Error Induced Reliability Emergency
Xianwei Zhang (AMD, U.S.A.), Rujia Wang, *Youtao Zhang, Jun Yang (Univ. of Pittsburgh, U.S.A.)

5C Learning: Make Patterning Light and Right

Time: 13:50 - 15:05, Wednesday, January 23, 2019
Location: Room Venus
Chairs: Tetsuaki Matsunawa (Toshiba Memory), Hidetoshi Matsuoka (Fujitsu Labs.)

5C-1 (Time: 13:50 - 14:15)
SRAF Insertion via Supervised Dictionary Learning
*Hao Geng, Haoyu Yang, Yuzhe Ma (Chinese Univ. of Hong Kong, Hong Kong), Joydeep Mitra (Cadence, U.S.A.), Bei Yu (Chinese Univ. of Hong Kong, Hong Kong)

5C-2 (Time: 14:15 - 14:40)
A Fast Machine Learning-based Mask Printability Predictor for OPC Acceleration
*Bentian Jiang (Chinese Univ. of Hong Kong, Hong Kong), Hang Zhang (Cornell Univ., U.S.A.), Jinglei Yang (Univ. of California, Santa Barbara, U.S.A.), Evangeline F. Y. Young (Chinese Univ. of Hong Kong, Hong Kong)

5C-3 (Time: 14:40 - 15:05)
Semi-Supervised Hotspot Detection with Self-Paced Multi-Task Learning
Ying Chen (Chinese Academy of Sciences/Univ. of Chinese Academy of Sciences, China), Yibo Lin (Univ. of Texas, Austin, U.S.A.), Tianyang Gai (Chinese Academy of Sciences/Univ. of Chinese Academy of Sciences, China), Yajuan Su (Chinese Academy of Sciences, China), Yayi Wei (Chinese Academy of Sciences/Univ. of Chinese Academy of Sciences, China), *David Z. Pan (Univ. of Texas, Austin, U.S.A.)

5D Design and CAD for Emerging Memories

Time: 13:50 - 15:05, Wednesday, January 23, 2019
Location: Room Mars+Room Mercury
Chairs: Li Jiang (Shanghai Jiao Tong Univ., China), Takao Marukame (Toshiba Corporate Research & Development Center, Japan)

5D-1 (Time: 13:50 - 14:15)
Exploring emerging CNFET for Efficient Last Level Cache Design
Dawen Xu, *Li Li (Hefei Univ. of Tech., China), Ying Wang, Cheng Liu, Huawei Li (Chinese Academy of Sciences, China)

5D-2 (Time: 14:15 - 14:40)
Mosaic: An Automated Synthesis Flow for Boolean Logic Based on Memristor Crossbar
*Lei Xie (Southeast Univ., China)

5D-3 (Time: 14:40 - 15:05)
Handling Stuck-at-faults in Memristor Crossbar Arrays using Matrix Transformations
Baogang Zhang, Necati Uysal, Deliang Fan, *Rickard Ewetz (Univ. of Central Florida, U.S.A.)

6A (DF-2) Advanced Imaging Technologies and Applications

Time: 15:35 - 17:15, Wednesday, January 23, 2019
Location: Room Saturn
Organizer: Masaki Sakakibara (Sony Semiconductor Solutions, Japan), Organizer/Chair: Shinichi Shibahara (Renesas Electronics, Japan)

6A-1 (Time: 15:35 - 16:00)
(Designers' Forum) NIR Lock-in Pixel Image Sensors for Remote Heart Rate Detection
Shoji Kawahito, Cao Chen, Leyi Tan, Keiichiro Kagawa, Keita Yasutomi (Shizuoka Univ., Japan), Norimichi Tsumura (Chiba Univ., Japan)

6A-2 (Time: 16:00 - 16:25)
(Designers' Forum) A TDC/ADC Hybrid LiDAR SoC for 200m Range Detection with High Image Resolution under 100klux Sunlight
Kentaro Yoshioka (Toshiba, Japan)

6A-3 (Time: 16:25 - 16:50)
(Designers' Forum) A 1/4-inch 3.9Mpixel Low Power Event-driven Back-illuminated Stacked CMOS Image sensor
Oichi Kumagai (Sony Semiconductor Solutions, Japan)

6A-4 (Time: 16:50 - 17:15)
(Designers' Forum) Next-Generation Fundus Camera with Full-Color Image Acquisition in 0-lx Visible Light using BSI CMOS Image Sensor with Advanced NIR Multi-Spectral Imaging System -Application Field Development of Dynamic Intelligent Systems Using High-Speed Vision-
Hirofumi Sumi, Hironari Takehara (NAIST, Japan), Norimasa Kishi (Univ. of Tokyo, Japan), Jun Ohta (NAIST, Japan), Masatoshi Ishikawa (Univ. of Tokyo, Japan)

6B Optimized Training for Neural Networks
Time: 15:35 - 16:50, Wednesday, January 23, 2019
Location: Room Uranus
Chairs: Deliang Fan (Univ. of Central Florida, U.S.A.), Raymond (Ruirui) Huang (Alibaba Cloud, U.S.A.)

6B-1 (Time: 15:35 - 16:00)
CAPTOR: A Class Adaptive Filter Pruning Framework for Convolutional Neural Networks in Mobile Applications
*Zhuwei Qin, Fuxun Yu (George Mason Univ., U.S.A.), ChenChen Liu (Clarkson Univ., U.S.A.), Xiang Chen (George Mason Univ., U.S.A.)

6B-2 (Time: 16:00 - 16:25)
TNPU: An Efficient Accelerator Architecture for Training Convolutional Neural Networks
*Jiajun Li, Guihai Yan, Wenyan Lu, Shuhao Jiang, Shijun Gong, Jingya Wu, Junchao Yan, Xiaowei Li (Chinese Academy of Sciences, China)

6B-3 (Time: 16:25 - 16:50)
REIN: A Robust Training Method for Enhancing Generalization Ability of Neural Networks in Autonomous Driving Systems
*Fuxun Yu (George Mason Univ., U.S.A.), Chenchen Liu (Clarkson Univ., U.S.A.), Xiang Chen (George Mason Univ., U.S.A.)

6C New Trends in Biochips
Time: 15:35 - 16:50, Wednesday, January 23, 2019
Location: Room Venus
Chair: Tsun-Ming Tseng (Tech. Univ. of Munich, Germany)

6C-1 (Time: 15:35 - 16:00)
Factorization Based Dilution of Biochemical Fluids with Micro-Electrode-Dot-Array Biochips
Sohini Saha (IIEST, Shibpur, India), Debraj Kundu, *Sudip Roy (IIT Roorkee, India), Sukanta Bhattacharjee (New York Univ., United Arab Emirates), Krishnendu Chakrabarty (Duke Univ., U.S.A.), Partha P. Chakrabarti (IIT Kharagpur, India), Bhargab B. Bhattacharya (ISI Kolkata, India)

6C-2 (Time: 16:00 - 16:25)
Sample Preparation for Multiple-Reactant Bioassays on Micro-Electrode-Dot-Array Biochips
*Tung-Che Liang (Duke Univ., U.S.A.), Yun-Sheng Chan (National Chiao Tung Univ., Taiwan), Tsung-Yi Ho (National Tsing Hua Univ., Taiwan), Krishnendu Chakrabarty (Duke Univ., U.S.A.), Chen-Yi Lee (National Chiao Tung Univ., Taiwan)

6C-3 (Time: 16:25 - 16:50)
Robust Sample Preparation on Low-Cost Digital Microfluidic Biochips
*Zhanwei Zhong (Duke Univ., U.S.A.), Robert Wille (Johannes Kepler Univ. Linz, Austria), Krishnendu Chakrabarty (Duke Univ., U.S.A.)

6D Power-efficient Machine Learning Hardware Design
Time: 15:35 - 16:50, Wednesday, January 23, 2019
Location: Room Mars+Room Mercury
Chairs: Hai Wang (UESTC, China), Sheldon Tan (Univ. of California, Riverside, U.S.A.)

6D-1 (Time: 15:35 - 16:00)
SAADI: A Scalable Accuracy Approximate Divider for Dynamic Energy-Quality Scaling
Setareh Behroozi, Jingjie Li, Jackson Melchert, *Younghyun Kim (Univ. of Wisconsin-Madison, U.S.A.)

6D-2 (Time: 16:00 - 16:25)
SeFAct: Selective Feature Activation and Early Classification for CNNs
*Farhana Sharmin Snigdha, Ibrahim Ahmed, Susmita Dey Manasi, Meghna G. Mankalale (Univ. of Minnesota, U.S.A.), Jiang Hu (Texas A&M Univ., U.S.A.), Sachin S. Sapatnekar (Univ. of Minnesota, U.S.A.)

6D-3 (Time: 16:25 - 16:50)
FACH: FPGA-based Acceleration of Hyperdimensional Computing by Reducing Computational Complexity
Mohsen Imani, Sahand Salamat, Saransh Gupta, *Jiani Huang, Tajana Rosing (UC San Diego, U.S.A.)

3K Keynote III

Time: 9:00 - 10:00, Thursday, January 24, 2019
Location: Miraikan Hall
Chair: Shinji Kimura (Waseda Univ., Japan)

3K-1 (Time: 9:00 - 10:00)
(Keynote Address) Hardware and Software Security Technologies to Enable Future Connected Cars
Yasuhisa Shimazaki (Renesas Electronics, Japan)

7A (SS-4) Security of Machine Learning and Machine Learning for Security: Progress and Challenges for Secure, Machine Intelligent Mobile Systems

Time: 10:20 - 12:00, Thursday, January 24, 2019
Location: Room Saturn
Chairs: Xiang Chen (George Mason Univ., U.S.A.), Yanzhi Wang (Northeastern Univ., U.S.A.)

7A-1 (Time: 10:20 - 10:45)
(Invited Paper) ADMM Attack: An Enhanced Adversarial Attack for Deep Neural Networks with Undetectable Distortions
Pu Zhao, *Kaidi Xu (Northeastern Univ., U.S.A.), Sijia Liu (IBM Research, U.S.A.), Yanzhi Wang, Xue Lin (Northeastern Univ., U.S.A.)

7A-2 (Time: 10:45 - 11:10)
(Invited Paper) A System-level Perspective to Understand the Vulnerability of Deep Learning Systems
Tao Liu, Nuo Xu, Qi Liu (Florida International Univ., U.S.A.), *Yanzhi Wang (Northeastern Univ., U.S.A.), Wujie Wen (Florida International Univ., U.S.A.)

7A-3 (Time: 11:10 - 11:35)
(Invited Paper) High-Performance Adaptive Mobile Security Enhancement against Malicious Speech and Image Recognition
*Zirui Xu, Fuxun Yu (George Mason Univ., U.S.A.), Chenchen Liu (Clarkson Univ., U.S.A.), Xiang Chen (George Mason Univ., U.S.A.)

7A-4 (Time: 11:35 - 12:00)
(Invited Paper) AdverQuil: an Efficient Adversarial Detection and Alleviation Technique for Black-Box Neuromorphic Computing Systems
Hsin-Pai Cheng, Juncheng Shen, Huanrui Yang (Duke Univ., U.S.A.), Qing Wu (Air Force Research Laboratory, U.S.A.), Hai Li, *Yiran Chen (Duke Univ., U.S.A.)

7B System Level Modelling Methods II

Time: 10:20 - 12:00, Thursday, January 24, 2019
Location: Room Uranus
Chair: Naehyuck Chang (KAIST, Republic of Korea)

7B-1 (Time: 10:20 - 10:45)
SIMULTime: Context-Sensitive Timing Simulation on Intermediate Code Representation for Rapid Platform Explorations
*Alessandro Cornaglia, Alexander Viehl (FZI Research Center for Information Technology, Germany), Oliver Bringmann, Wolfgang Rosenstiel (Univ. of Tübingen, Germany)

7B-2 (Time: 10:45 - 11:10)
Modeling Processor Idle Times in MPSoC Platforms to Enable Integrated DPM, DVFS, and Task Scheduling Subject to a Hard Deadline
Amirhossein Esmaili, Mahdi Nazemi, *Massoud Pedram (Univ. of Southern California, U.S.A.)

7B-3 (Time: 11:10 - 11:35)
Phone-nomenon: A System-Level Thermal Simulator for Handheld Devices
*Hong-Wen Chiou, Yu-Min Lee, Shin-Yu Shiau (National Chiao Tung Univ., Taiwan), Chi-Wen Pan, Tai-Yu Chen (Mediatek, Taiwan)

7B-4 (Time: 11:35 - 12:00)
Virtual Prototyping of Heterogeneous Automotive Applications: Matlab, SystemC, or both?
Xiao Pan, *Carna Zivkovic, Christoph Grimm (Univ. of Kaiserslautern, Germany)

7C Placement

Time: 10:20 - 12:00, Thursday, January 24, 2019
Location: Room Venus
Chairs: Ting-Chi Wang (National Tsing Hua Univ.), Yasuhiro Takashima (Univ. of Kitakyushu, Japan)

7C-1 (Time: 10:20 - 10:45)
Diffusion Break-Aware Leakage Power Optimization and Detailed Placement in Sub-10nm VLSI
Sun ik Heo (Samsung Electronics, Republic of Korea), *Andrew B. Kahng, Minsoo Kim, Lutong Wang (UC San Diego, U.S.A.)

7C-2 (Time: 10:45 - 11:10)
MDP-trees: Multi-Domain Macro Placement for Ultra Large-Scale Mixed-Size Designs
*Yen-Chun Liu (National Taiwan Univ., Taiwan), Tung-Chieh Chen (Maxeda Technology, Taiwan), Yao Wen Chang, Sy-Yen Kuo (National Taiwan Univ., Taiwan)

7C-3 (Time: 11:10 - 11:35)
A Shape-Driven Spreading Algorithm Using Linear Programming for Global Placement
*Shounak Dhar (Univ. of Texas, Austin, U.S.A.), Love Singhal, Mahesh A. Iyer (Intel, U.S.A.), David Z. Pan (Univ. of Texas, Austin, U.S.A.)

7C-4 (Time: 11:35 - 12:00)
Finding Placement-Relevant Clusters With Fast Modularity-Based Clustering
*Mateus Fogaça (Univ. Federal do Rio Grande do Sul, Brazil), Andrew B. Kahng (Univ. of California, San Diego, U.S.A.), Ricardo Augusto da Luz Reis (Univ. Federal do Rio Grande do Sul, Brazil), Lutong Wang (Univ. of California, San Diego, U.S.A.)

7D Algorithms and Architectures for Emerging Applications

Time: 10:20 - 12:00, Thursday, January 24, 2019
Location: Room Mars+Room Mercury
Chair: Taewhan Kim (Seoul National Univ., Republic of Korea)

7D-1 (Time: 10:20 - 10:45)
An Approximation Algorithm to the Optimal Switch Control of Reconfigurable Battery Packs
Shih-Yu Chen, *Jie-Hong Jiang (National Taiwan Univ., Taiwan), Shou-Hung Ling, Shih-Hao Liang, Mao-Cheng Huang (ITRI, Taiwan)

7D-2 (Time: 10:45 - 11:10)
Autonomous Vehicle Routing In Multiple Intersections
*Sheng-Hao Lin, Tsung-Yi Ho (National Tsing Hua Univ., Taiwan)

7D-3 (Time: 11:10 - 11:35)
GRAM: Graph Processing in a ReRAM-based Computational Memory
*Minxuan Zhou, Mohsen Imani, Saransh Gupta, Yeseong Kim, Tajana Rosing (Univ. of California, San Diego, U.S.A.)

7D-4 (Time: 11:35 - 12:00)
ADEPOS: Anomaly Detection based Power Saving for Predictive Maintenance using Edge Computing
*Sumon Kumar Bose, Bapi Kar, Mohendra Roy, Pradeep Kumar Gopalakrishnan, Arindam Basu (Nanyang Technological Univ., Singapore)

8A (DF-3) Emerging Technologies for Tokyo Olympic 2020

Time: 13:15 - 14:30, Thursday, January 24, 2019
Location: Room Saturn
Organizer/Chair: Koichiro Yamashita (Fujitsu, Japan), Organizer: Akihiko Inoue (Panasonic, Japan)

8A-1 (Time: 13:15 - 13:40)
(Designers' Forum) Walking assistive powered-wear 'HIMICO' with wire-driven assist
Kenta Murakami (Panasonic, Japan)

8A-2 (Time: 13:40 - 14:05)
(Designers' Forum) Deep Scene Recognition with Object Detection
Zhiming Tan (Fujitsu R&D Center, China)

8A-3 (Time: 14:05 - 14:30)
(Designers' Forum) Spatial and battery sensing solutions for smart cities leading to 2020 Olympics
Hiroyuki Tsujikawa (Panasonic, Japan)

8B Embedded Software for Parallel Architecture

Time: 13:15 - 14:30, Thursday, January 24, 2019
Location: Room Uranus
Chairs: Mengying Zhao (Shandong Univ., China), Weichen Liu (Nanyang Technological Univ.)

8B-1 (Time: 13:15 - 13:40)
Efficient Sporadic Task Handling in Parallel AUTOSAR Applications Using Runnable Migration
*Milan Copic, Rainer Leupers, Gerd Ascheid (RWTH Aachen Univ., Germany)

8B-2 (Time: 13:40 - 14:05)
A Heuristic for Multi Objective Software Application Mappings on Heterogeneous MPSoCs
*Gereon Onnebrink, Ahmed Hallawa, Rainer Leupers, Gerd Ascheid (RWTH Aachen Univ., Germany), Awaid-Ud-Din Shaheen (Silexica GmbH, Germany)

8B-3 (Time: 14:05 - 14:30)
ReRAM-based Processing-in-Memory Architecture for Blockchain Platforms
*Fang Wang (Hong Kong Polytechnic Univ., Hong Kong), Zhaoyan Shen (Shandong Univ., China), Lei Han (Hong Kong Polytechnic Univ., Hong Kong), Zili Shao (Chinese Univ. of Hong Kong, Hong Kong)

8C Machine Learning and Hardware Security

Time: 13:15 - 14:30, Thursday, January 24, 2019
Location: Room Venus
Chairs: Dong Kyue Kim (Hanyang Univ., Republic of Korea), Ray C.C. Cheung (City Univ. of Hong Kong, Hong Kong)

8C-1 (Time: 13:15 - 13:40)
Towards Practical Homomorphic Email Filtering: A Hardware-Accelerated Secure Naive Bayesian Filter
*Song Bian, Masayuki Hiromoto, Takashi Sato (Kyoto Univ., Japan)

8C-2 (Time: 13:40 - 14:05)
A 0.16pJ/bit Recurrent Neural Network Based PUF for Enhanced Machine Learning Attack Resistance
*Nimesh Kirit Shah (Nanyang Technological Univ., Singapore), Manaar Alam (Indian Inst. of Tech. Kharagpur, India), Durga Prasad Sahoo (Robert Bosch Engineering and Business Solutions Private, India), Debdeep Mukhopadhyay (Indian Inst. of Tech. Kharagpur, India), Arindam Basu (Nanyang Technological Univ., Singapore)

8C-3 (Time: 14:05 - 14:30)
P^3M: A PIM-based Neural Network Model Protection Scheme for Deep Learning Accelerator
*Wen Li, Ying Wang, Huawei Li, Xiaowei Li (Chinese Academy of Sciences, China)

8D Memory Architecture for Efficient Neural Network Computing

Time: 13:15 - 14:30, Thursday, January 24, 2019
Location: Room Mars+Room Mercury
Chairs: Jongeun Lee (UNIST, Republic of Korea), Bei Yu (Chinese Univ. of Hong Kong, Hong Kong)

8D-1 (Time: 13:15 - 13:40)
Learning the Sparsity for ReRAM: Mapping and Pruning Sparse Neural Network for ReRAM based Accelerator
*Jilan Lin (UCSB/Tsinghua Univ., China), Zhenhua Zhu, Yu Wang (Tsinghua Univ., China), Yuan Xie (UCSB, U.S.A.)

8D-2 (Time: 13:40 - 14:05)
In-Memory Batch-Normalization for Resistive Memory based Binary Neural Network Hardware
*Hyungjun Kim, Yulhwa Kim, Jae-Joon Kim (POSTECH, Republic of Korea)

8D-3 (Time: 14:05 - 14:30)
Exclusive On-Chip Memory Architecture for Energy-Efficient Deep Learning Acceleration
*Hyeonuk Sim (UNIST, Republic of Korea), Jason Anderson (Univ. of Toronto, Canada), Jongeun Lee (UNIST, Republic of Korea)

9A (DF-4) Beyond the Virtual Reality World

Time: 14:50 - 16:05, Thursday, January 24, 2019
Location: Room Saturn
Organizer: Hiroe Iwasaki (NTT, Japan), Organizer/Chair: Masaru Kokubo (Hitachi, Japan)

9A-1 (Time: 14:50 - 15:15)
(Designers' Forum) The World of VR2.0
Michitaka Hirose (Univ. of Tokyo, Japan)

9A-2 (Time: 15:15 - 15:40)
(Designers' Forum) Optical fiber scanning system for ultra-lightweight wearable display
Yoshio Seo (Hitachi, Japan)

9A-3 (Time: 15:40 - 16:05)
(Designers' Forum) Superreal Video Representation for Enhanced Sports Experiences - R&D on VR x AI technologies -
Hideaki Kimata (NTT, Japan)

9B Logic-Level Security and Synthesis

Time: 14:50 - 16:05, Thursday, January 24, 2019
Location: Room Uranus
Chairs: Akash Kumar (TU Dresden), Tsutomu Sasao (Meiji Univ.)

9B-1 (Time: 14:50 - 15:15)
BeSAT: Behavioral SAT-based Attack on Cyclic Logic Encryption
Yuanqi Shen, You Li, Amin Rezaei, Shuyu Kong, David Dlott, *Hai Zhou (Northwestern Univ., U.S.A.)

9B-2 (Time: 15:15 - 15:40)
Structural Rewriting in XOR-Majority Graphs
*Zhufei Chu (Ningbo Univ., China), Mathias Soeken (EPFL, Switzerland), Yinshui Xia, Lunyao Wang (Ningbo Univ., China), Giovanni De Micheli (EPFL, Switzerland)

9B-3 (Time: 15:40 - 16:05)
Design Automation for Adiabatic Circuits
*Alwin Zulehner (Johannes Kepler Univ. Linz, Austria), Micheal Frank (Sandia National Labs, U.S.A.), Robert Wille (Johannes Kepler Univ. Linz, Austria)

9C Analysis and Algorithms for Digital Design Verification

Time: 14:50 - 16:05, Thursday, January 24, 2019
Location: Room Venus
Chairs: Mark Po-Hung Lin (National Chung Cheng Univ., Taiwan), Andreas G. Veneris (Univ. of Toronto, Canada)

9C-1 (Time: 14:50 - 15:15)
A Figure of Merit for Assertions in Verification
Samuel Hertz, *Debjit Pal, Spencer Offenberger, Shobha Vasudevan (Univ. of Illinois, Urbana-Champaign, U.S.A.)

9C-2 (Time: 15:15 - 15:40)
Suspect2vec: A Suspect Prediction Model for Directed RTL Debugging
*Neil Veira, Zissis Poulos, Andreas Veneris (Univ. of Toronto, Canada)

9C-3 (Time: 15:40 - 16:05)
Path Controllability Analysis for High Quality Designs
*Li-Jie Chen (National Taiwan Univ., Taiwan), Hong-Zu Chou, Kai-Hui Chang (Avery Design Systems, U.S.A.), Sy-Yen Kuo (National Taiwan Univ., Taiwan), Chilai Huang (Avery Design Systems, U.S.A.)

9D FPGA and Optics-Based Neural Network Designs

Time: 14:50 - 16:05, Thursday, January 24, 2019
Location: Room Mars+Room Mercury
Chair: Taewhan Kim (Seoul National Univ., Republic of Korea)

9D-1 (Time: 14:50 - 15:15)
Implementing Neural Machine Translation with Bi-Directional GRU and Attention Mechanism on FPGAs Using HLS
*Qin Li, Xiaofan Zhang (Univ. of Illinois, Urbana-Champaign, U.S.A.), Jinjun Xiong (IBM, U.S.A.), Wen-mei Hwu, Deming Chen (Univ. of Illinois, Urbana-Champaign, U.S.A.)

9D-2 (Time: 15:15 - 15:40)
Efficient FPGA Implementation of Local Binary Convolutional Neural Network
Aidyn Zhakatayev, *Jongeun Lee (Ulsan National Inst. of Science and Tech., Republic of Korea)

9D-3 (Time: 15:40 - 16:05)
Hardware-software Co-design of Slimmed Optical Neural Networks
*Zheng Zhao, Derong Liu, Meng Li, Zhoufeng Ying, Biying Xu (Univ. of Texas, Austin, U.S.A.), Lu Zhang, Bei Yu (Chinese Univ. of Hong Kong, Hong Kong), Ray T. Chen, David Z. Pan (Univ. of Texas, Austin, U.S.A.)

10A (SS-5) The Resurgence of Reconfigurable Computing in the Post Moore Era

Time: 16:25 - 17:40, Thursday, January 24, 2019
Location: Room Saturn
Chair: Antonino Tumeo (Pacific Northwest National Laboratory, U.S.A.)

10A-1 (Time: 16:25 - 16:50)
(Invited Paper) Software Defined Architectures for Data Analytics
*Vito Giovanni Castellana, Marco Minutoli, Antonino Tumeo (Pacific Northwest National Laboratory, U.S.A.), Pietro Fezzardi, Marco Lattuada, Fabrizio Ferrandi (Politecnico di Milano, Italy)

10A-2 (Time: 16:50 - 17:15)
(Invited Paper) Runtime Reconfigurable Memory Hierarchy in Embedded Scalable Platforms
Davide Giri, Paolo Mantovani, *Luca P. Carloni (Columbia Univ., U.S.A.)

10A-3 (Time: 17:15 - 17:40)
(Invited Paper) XPPE: Cross-Platform Performance Estimation of Hardware Accelerators Using Machine Learning
*Hosein Mohamamdi Makrani, Hossein Sayadi, Tinoosh Mohsenin, Avesta Sasan, Houman Homayoun, Setareh Rafatirad (George Mason Univ., U.S.A.)

10B Hardware Acceleration

Time: 16:25 - 17:40, Thursday, January 24, 2019
Location: Room Uranus
Chairs: Yongpan Liu (Tsinghua Univ., China), Xiang Chen (George Mason Univ., U.S.A.)

10B-1 (Time: 16:25 - 16:50)
Addressing the Issue of Processing Element Under-Utilization in General-Purpose Systolic Deep Learning Accelerators
Bosheng Liu (Univ. of Chinese Academy of Sciences/Chinese Academy of Sciences, China), *Xiaoming Chen, Ying Wang, Yinhe Han (Chinese Academy of Sciences, China), Jiajun Li, Haobo Xu (Univ. of Chinese Academy of Sciences, China), Xiaowei Li (Chinese Academy of Sciences, China)

10B-2 (Time: 16:50 - 17:15)
ALook: Adaptive Lookup for GPGPU Acceleration
*Daniel Peroni, Mohsen Imani, Tajana Rosing (Univ. of California, San Diego, U.S.A.)

10B-3 (Time: 17:15 - 17:40)
Collaborative Accelerators for In-Memory MapReduce on Scale-up Machines
*Abraham Addisie, Valeria Bertacco (Univ. of Michigan, U.S.A.)

10C Routing

Time: 16:25 - 17:40, Thursday, January 24, 2019
Location: Room Venus
Chairs: Hunng-Ming Chen (NCTU), Kohira Yukihide (Univ. of Aizu)

10C-1 (Time: 16:25 - 16:50)
Detailed Routing by Sparse Grid Graph and Minimum-Area-Captured Path Search
*Gengjie Chen, Chak-Wa Pui, Haocheng Li, Jingsong Chen, Bentian Jiang, Evangeline F. Y. Young (Chinese Univ. of Hong Kong, Hong Kong)

10C-2 (Time: 16:50 - 17:15)
Thermal-aware 3D Symmetrical Buffered Clock Tree Synthesis
Deok Keun Oh, Mu Jun Choi, Ju Ho Kim (Sogang Univ., Republic of Korea)

10C-3 (Time: 17:15 - 17:40)
Latency Constraint Guided Buffer Sizing and Layer Assignment for Clock Trees with Useful Skew
*Necati Uysal (Univ. of Central Florida, U.S.A.), Wen-Hao Liu (Cadence Design Systems, U.S.A.), Rickard Ewetz (Univ. of Central Florida, U.S.A.)

Supporter's Exhibition

Supporter's exhibition is held by three companies which support ASP-DAC 2019 and have exhibition booths. The supporter's exhibition is presented at Miraikan 7F Lobby from January 22 through January 24.

Exhibit Hours: **10:00 – 17:30, January 22 / 10:00 – 17:30, January 23 / 10:00 – 16:00, January 24**
Location: **Miraikan 7F Lobby**

MunEDA GmbH https://www.muneda.com/	MunEDA provides withing it's WiCkeD EDA suite tools for migration, sizing and verification of Custom IC circuits such as Highspeed I/O, Memory, RF Circuits, Analog, Standard Cells, and many others. Designers can improve and optimize the circuit regarding constraints & feasibility, performances & specifications, robustness, yield, area, stability, timing, power, realiability, aging, degradation, stress, self heating and many others.
TOSHIBA MEMORY Toshiba Memory Corporation https://business.toshiba-memory.com/en-apac/top.html	Toshiba Memory Corporation, a world leader in memory solutions, is dedicated to the development, production and sales of flash memory and SSDs. In June 2018, Toshiba Memory was acquired by an industry consortium led by Bain Capital. Toshiba Memory pioneers cutting-edge memory solutions and services that enrich people's lives and expand society's horizons. The company's innovative 3D flash memory technology, BiCS FLASH™, is shaping the future of storage in high density applications including advanced smartphones, PCs, SSDs, automotive and data centers. For more information on Toshiba Memory, please visit https://business.toshiba-memory.com/en-apac/top.html
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Information

Proceedings:
ASP-DAC 2019 will be producing an authority to access the download site for the conference proceedings. The site will be open on Jan. 21, 2019. Please note that neither CD-ROM nor USB memory are provided.

Banquet:
Conference registrants are invited to attend a banquet to be held on January 23, 2019. The banquet will be held from 18:30 to 20:30 at the Hilton Tokyo Odaiba 1F "Room Orion". Regular Member and Non-member Conference registrants receive a ticket to the banquet when they register at the conference. Full-time students, Designers' Forum-only registrants, and Tutorial-only registrants wishing to attend the banquet will be required to pay 5,000 yen for a ticket when they register on site.

Duty free import:
Personal effects and professional equipment can be brought into Japan duty free as long as their contents and quantities are deemed reasonable by the customs officer. You can also bring in 400 cigarettes, 500 grams of tobacco or 100 cigars; 3 bottles of alcoholic beverages; 2 ounces of perfume; and gifts and souvenirs whose total market price is less than 200,000 yen or its equivalent. There is no allowance for tobacco or alcoholic beverages for persons aged 19 years or younger. Firearms and other types of weapons, and narcotics are strictly prohibited.

Currency Exchange:
Only Japanese yen (JPY, ¥) is acceptable at regular stores and restaurants. Certain foreign currencies may be accepted at a limited number of hotels, restaurants and souvenir shops. You can buy yen at foreign exchange banks and other authorized money exchangers on presentation of your passport.

Travelers checks and credit cards:
Travelers checks are accepted only by leading banks and major hotels in principal cities, and the use of travelers checks in Japan is not as popular as in some other countries. VISA, MasterCard, Diners Club, and American Express are widely accepted at hotels, department stores, shops, restaurants and nightclubs.

Tipping:
In Japan, tips are not necessary anywhere, even at hotels and restaurants.

Electricity:
Electric voltage is uniformly 100 volts, AC, throughout Japan, but with two different cycles: 50 in Eastern Japan*, and 60 in Western Japan**. Leading hotels in major cities have two outlets of 100 and 220 volts but their sockets usually accept a two-leg plug only.
*Eastern Japan :**Tokyo**, Yokohama, Tohoku, Hokkaido
**Western Japan :Nagoya, Osaka, Kyoto, Hiroshima, Shikoku, Kyushu

Shopping:
Shops and other sales outlets in Japan are generally open on Saturdays, Sundays and national holidays as well as weekdays from 10:00 to 20:00. Department stores, however, are closed on one weekday, differing by store, and certain specialty shops may not open on Sundays and national holidays.

Other Information:
Participants can get sightseeing information at the JTB Travel desk in the Conference site during the Conference period.

GO TOKYO
http://www.gotokyo.org/en/
TRAVEL DIRECTORY Odaiba
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JAPAN NATIONAL TOURISM ORGANIZATION
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MEMO

MEMO

ASIA SOUTH PACIFIC DESIGN AUTOMATION CONFERENCE

Call for Papers
ASP-DAC 2020

http://www.aspdac.com/
January 13-16, 2020
China National Convention Center (CNCC)
Beijing, China

Aims of the Conference:
ASP-DAC 2020 is the 25th annual international conference on VLSI design automation in Asia and South Pacific regions, one of the most active regions of design and fabrication of silicon chips in the world. The conference aims at providing the Asian and South Pacific CAD/DA and Design community with opportunities of presenting recent advances and with forums for future directions in technologies related to Electronic Design Automation (EDA). The format of the meeting intends to cultivate and promote an instructive and productive interchange of ideas among EDA researchers/developers and system/circuit/device designers. All scientists, engineers, and students who are interested in theoretical and practical aspects of VLSI design and design automation are welcomed to ASP-DAC.

Areas of Interest:
Original papers in, but not limited to, the following areas are invited.

[1] System-Level Modeling and Design Methodology:
1.1. HW/SW co-design, co-simulation and co-verification
1.2. System-level design exploration, synthesis and optimization
1.3. Model- and component-based embedded system/software design
1.4. System-level formal verification
1.5. System-level modeling, simulation and validation tools/methodology

[2] Embedded System Architecture and Design:
2.1. Many- and multi-core SoC architecture
2.2. Reconfigurable and self-adaptive SoC architecture
2.3. IP/platform-based SoC design
2.4. Domain-specific architecture
2.5. Dependable architecture
2.6. Machine learning architecture
2.7. Cyber physical system
2.8. Storage system and memory architecture
2.9. Internet of things

[3] On-chip Communication and Networks-on-Chip:
3.1. Communication-centric system design, application, and simulation
3.2. Networks-on-chip and NoC-based system design
3.3. Inter/intra-chip interconnect and network, and interface and I/O
3.4. Emerging interconnect technology and application

[4] Embedded Software:
4.1. Kernel, middleware and virtual machine
4.2. Compiler and toolchain
4.3. Real-time system
4.4. Resource allocation for heterogeneous computing platform
4.5. Storage software and application
4.6. Human-computer interface
4.7. System verification and analysis

[5] Device/Circuit-Level Modeling, Simulation and Verification:
5.1. Device/circuit/interconnect modeling and analysis
5.2. Device/circuit-level simulation tool and methodology
5.3. RTL and gate-leveling modeling, simulation and verification
5.4. Circuit-level formal verification

[6] Analog, RF and Mixed Signal:
6.1. Analog/mixed-signal/RF synthesis
6.2. Analog layout, verification and simulation techniques
6.3. Noise analysis
6.4. High-frequency electromagnetic simulation of circuit
6.5. Mixed-signal design consideration
6.6. Power-aware analog circuit/system design
6.7. Analog/mixed-signal modeling and simulation techniques

[7] Power Analysis, Low Power Design, and Thermal Management:
7.1. Power modeling, analysis and simulation
7.2. Low-power design and methodology
7.3. Thermal aware design
7.4. Energy harvesting and battery management

[8] Logic/High-Level Synthesis and Optimization:
8.1. High-level synthesis tool and methodology
8.2. Combinational, sequential and asynchronous logic synthesis
8.3. Logic synthesis and physical design technique for FPGA
8.4. Technology mapping

[9] Physical Design:
9.1. Floorplanning, partitioning and placement
9.2. Interconnect planning and synthesis
9.3. Placement and routing optimization
9.4. Clock network synthesis
9.5. Post layout and post-silicon optimization
9.6. Package/PCB/3D-IC routing

[10] Design for Manufacturability and Reliability:
10.1. Reticle enhancement, lithography-related design and optimization
10.2. Resilience under manufacturing variation
10.3. Design for manufacturability, yield, and defect tolerance
10.4. Reliability, aging and soft error analysis
10.5. Design for reliability, aging, and robustness

[11] Timing and Signal/Power Integrity:
11.1. Deterministic/statistical timing and performance analysis and optimization
11.2. Power/ground and package modeling, analysis and optimization
11.3. Signal/power integrity, EM modeling and analysis
11.4. Extraction, TSV and package modeling
11.5. 2D/3D on-chip power delivery network analysis and optimization

[12] Test and Design for Testability:
12.1. ATPG, BIST and DFT
12.2. Fault modeling and simulation
12.3. System test and 3D IC test
12.4. Online test and fault tolerance
12.5. Memory test and repair
12.6. Analog and mixed-signal/RF test

[13] Security and Fault-Tolerant System:
13.1. Security modeling and analysis
13.2. Architecture, tool and methodology for secure hardware
13.3. Design for security and security primitive
13.4. Cross-layer security
13.5. Fault analysis, detect and tolerance

[14] Emerging Technology:
14.1. New transistor/device and process technology: spintronic, phase-change, single-electron etc.
14.2. CAD for nanotechnology, MEMS, quantum computing etc.
14.3. Neuromorphic and brain-inspired computing

[15] Emerging Application:
15.1. Biomedical, biochip, and biodata processing.
15.2. Big/thick data, datacenter
15.3. Advanced multimedia application
15.4. Energy-storage/smart-grid/smart-building design and optimization
15.5. Automotive system design and optimization
15.6. Electromobility

Please note that each paper shall be accompanied by at least one different conference registration at the speaker's registration rate (e.g., two speaker registrations are needed for presenting two accepted papers). But any registered co-author can present the work at the conference. ACM and IEEE reserve the right to exclude a paper from distribution after the conference (e.g., removal from ACM Digital Library and IEEE Xplore) if the paper is not presented at the conference by the author of the paper. ASP-DAC does not allow double and/or parallel submissions of similar work to any other conferences, symposia, and journals.

Submission of Papers:

Deadline for submission:	**5 PM AOE (Anywhere on earth)**	**July 5 (Fri), 2019**
Notification of acceptance:		**Sep. 9 (Mon), 2019**
Deadline for final version:	**5 PM AOE (Anywhere on earth)**	**Nov. 4 (Mon), 2019**

For detailed instructions for submission, please refer to the "Authors' Guide" at: **http://www.aspdac.com/**

ASP-DAC 2019 Chairs

General Co-Chairs:	**Tim Cheng (Hong Kong University of Science and Technology)**
	Huazhong Yang (Tsinghua University)
Technical Program Chair:	**Tsung-Yi Ho (National Tsing Hua University)**
Technical Program Vice Chairs:	**Sheldon Tan (University of California, Riverside)**
	Yiran Chen (Duke University)

Panels, Special Sessions, and Tutorials: Suggestions and proposals are welcome and have to be addressed to the Conference Secretariat (aspdac2020@aspdac.com) no later than August 2 (Fri), 2020.
Contact: Conference Secretariat: aspdac2020@aspdac.com TPC Secretariat: tpc@aspdac20.com

Call for Designs

University LSI Design Contest

ASP-DAC 2020

http://www.aspdac.com/aspdac/
January 13-16, 2020
China National Convention Center (CNCC), Beijing, China

Aims of the Contest:

The University LSI Design Contest will be held as an interesting feature of ASP-DAC 2020. The aim of the Contest is to encourage education and research on IC design at universities or other academic organizations. We solicit designs that fit in some of the following categories:

- Designed, and actually Silicon proven on chips in universities or other academic organizations during the last two years;
- Designs that report actual measurements from implementations;
- Innovative design prototypes.

Excellent designs selected will be honored with the opportunities for oral presentation in a special session at the conference. And awards will be given to a few numbers of outstanding designs, selected from those presented at the conference.

Areas of Design:

Application areas or types of circuits of original LSI circuit designs include, but are not limited to:
(1) Analog, RF and Mixed-Signal Circuits, (2) Digital Signal Processing, (3) Microprocessors, (4) System-on-Chip, and (5) Custom ASIC.
Methods or technology used for implementation include:
(1) Custom ASIC and Cell-Based LSIs, (2) Gate Arrays, and (3) FPGA/PLDs

Submission of Design Descriptions:

A camera-ready summary is requested to be prepared within 2 pages including figures, tables, and references. It is strongly recommended that measured experimental results and a chip micrograph are included in the summary. Please do not submit the same paper as a regular paper.
Specification of the submission format will be available at http://www.aspdac.com/aspdac/

- Deadline for summary: July 5 (Friday), 2019
- Notification of acceptance: Sept. 9 (Monday), 2019
- Deadline for camera-ready: Nov. 4 (Monday), 2019

Review:

The proposed designs will be reviewed by the Design Contest Committee using a process similar to the review process for the technical papers. The following criteria will be applied in the selection of designs: (1) Reliability of design and implementation, (2) Quality of implementation, (3) Performance of the design, (4) Novelty of application, algorithm, architecture, (5) Others.
Interesting or excellent designs selected will be presented at a special session of the conference.

Presentation:

An author of each selected design will be required to make oral presentation at a special session of ASP-DAC 2020. And the digest of each design to be presented will be included in the conference proceedings.

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