	ASP-DAC 2020 Accepted Paper List
Paper ID	Paper Title
1004	Audio Adversarial Examples Generation with Recurrent Neural Networks
1011	MindReading: An Ultra Low-Power Nanophotonic Accelerator for EEG-based Intention Recognition
1014	A Generic FPGA Accelerator for Minimum Storage Regenerating Codes
1015	Contention Minimized Bypassing in SMART NoC
1016	JIT-Based Context-Sensitive Timing Simulation for Efficient Platform Exploration
1017	Enhancing Generalization of Wafer Defect Detection by Data Discrepancy-aware Preprocessing and Contrast-varied Augmentation
1018	Unified Redistribution Layer Routing for 2.5D IC Packages
1022	HL-Pow: A Learning-Based Power Modeling Framework for High-Level Synthesis
1023	Machine Learning Based Online Full-Chip Heatmap Estimation
1025	Event Delivery using Prediction for Faster Parallel SystemC Simulation
1027	Representable Matrices: Enabling High Accuracy Analog Computation for Inference of DNNs using Memristors
1032	FTT-NAS: Discovering Fault-Tolerant Neural Architecture
1033	Establishing Reachset Conformance for the Formal Analysis of Analog Circuits
1034	Black Box Search Space Profiling for Accelerator-Aware Neural Architecture Search
1038	Towards Design Methodology of Efficient Fast Algorithms for Accelerating Generative Adversarial Networks on FPGAs
1039	Search-free Accelerator for Sparse Convolutional Neural Networks
1040	"An Energy-Efficient Quantized and Regularized Training Framework For Processing-In-Memory Accelerators"
1053	When Single Event Upset Meets Deep Neural Networks: Observations, Explorations, and Remedies
1056	EFFORT: Enhancing Energy Efficiency and Error Resilience of a Near-Threshold Tensor Processing Unit
1060	Nonvolatile and Energy-efficient FeFET-Based Multiplier for Energy-Harvesting Devices
1061	A Reconfigurable Approximate Multiplier for Quantized CNN Applications
1067	Insights and Optimizations on IR-drop Induced Sneak-Path for RRAM Crossbar-based Convolutions
1075	Exploring Graphical Models with Bayesian Learning and MCMC for Failure Diagnosis
1076	Programmable Neuromorphic Circuit based on Printed Electrolyte-Gated Transistors
1082	Standard-compliant Parallel SystemC simulation of Loosely-Timed Transaction Level Models
1084	Integrated Airgap Insertion and Layer Reassignment for Circuit Timing Optimization
1085	iGPU Leak: An Information Leakage Vulnerability on Intel Integrated GPU
1088	Towards Automatic Hardware Synthesis from Formal Specification to Implementation
1090	Reutilization of Trace Buffers for Performance Enhancement of NoC based MPSoCs
1096	AIR: A Fast but Lazy Timing-Driven FPGA Router

1097	Optimal Fluid Loading on Programmable Microfluidic Devices for Bio-protocol Execution
1105	Modulo Scheduling with Rational Initiation Intervals in Custom Hardware Design
1110	Advanced Equivalence Checking of Quantum Circuits
1112	Mitigating Adversarial Attacks for Deep Neural Networks by Input Deformation and Augmentation
1114	An FPGA based Network Interface Card with Query Filter for Storage nodes of Big Data Systems
1117	"EA-HRT: An Energy-Aware scheduler for Heterogeneous Real-Time systems"
1118	Concurrency in DD-based Quantum Circuit Simulation
1120	Automated Trigger Activation by Repeated Maximal Clique Sampling
1122	Automated Test Generation for Activation of Assertions in RTL Models
1123	Approximation of Quantum States Using Decision Diagrams
1126	Template-based PDN Synthesis in Floorplan and Placement Using Classifier and CNN Techniques
1130	Thanos: High-Performance CPU-GPU Based Graph Partitioning Using Cross-Decomposition
1132	"PARC: A Processing-in-CAM Architecture for Genomic Long Read Pairwise Alignment using ReRAM"
1134	Formal Semantics of Predictable Pipelines: a Comparative Study
1135	High-Definition Routing Congestion Prediction for Large-Scale FPGAs
1137	S3DET: Detecting System Symmetry Constraints for Analog Circuits with Graph Similarity
1143	Towards Area-Efficient Optical Neural Networks: An FFT-based Architecture
1144	"A Flexible Processing-in-Memory Accelerator for Dynamic Channel-Adaptive Deep Neural Networks"
1147	PowerNet: Transferable Dynamic IR Drop Estimation via Maximum Convolutional Neural Network
1149	FIST: A Feature-Importance Sampling and Tree-Based Method for Automatic Design Flow Parameter Tuning
1152	LanCe: A Comprehensive and Lightweight CNN Defense Methodology against Physical Adversarial Attacks on Embedded Multimedia Applications
1154	CP-CNN: Cluster-Based Partitioning of Convolutional Neural Networks, A Solution for Computational Energy and Complexity Reduction
1163	The Notion of Cross Coverage in AMS Design Verification
1166	Concurrent Monitoring of Operational Health in Neural Networks Through Balanced Output Partitions
1167	Equivalent Capacitance Guided Dummy Fill Insertion for Timing and Manufacturability
1173	HashHeat: An O(C) Complexity Hashing-based Filter for Dynamic Vision Sensor
1181	An Adaptive Electromigration Assessment Algorithm for Full-chip Power/Ground Networks
1184	"Defects Mitigation in Resistive Crossbars for Analog VectorMatrix Multiplication"
1185	Analyzing The Security of The Cache Side Channel Defences With Attack Graphs
1195	"Towards read-intensive key-value stores with tidal structure based on LSM-Tree"
1196	WEID: Worst-Case Error Improvement in Approximate Dividers
1199	Chiplet-Package Co-Design For 2.5D Systems Using Standard ASIC CAD Tools

1200	Co-Exploring Neural Architecture and Network-on-Chip Design for Real-Time Artificial Intelligence
1204	Synthesis of Hardware Performance Monitoring and Prediction Flow Adapting to Near-Threshold Computing and Advanced Process Nodes
1206	Lightening Asynchronous Pipeline Controller Through Resynthesis and Optimization
1219	"Workload-aware Data-eviction Self-adjusting System of Multi-SCM Storage to Resolve Trade-off between SCM Data-retention Error and Storage System Performance"
1220	DRiLLS: Deep Reinforcement Learning for Logic Synthesis
1222	Design for EM Side-Channel Security through Quantitative Assessment of RTL Implementations
1226	Scaled Population Arithmetic for Efficient Stochastic Computing
1228	A tuning-free reservoir of MOSFET crossbar array for inexpensive hardware realization of echo state network
1232	Tiny but Accurate: A Pruned, Quantized and Optimized Memristor Crossbar Framework for Ultra Efficient DNN Implementation
1235	SP&R: Simultaneous placement and routing framework for standard cell synthesis in sub-7nm
1238	LeAp: Leading-one Detection-based Softcore Approximate Multipliers with Tunable Accuracy
1243	Towards Efficient Kyber on FPGAs: A Processor for Vector of Polynomials
1245	Broadcast Mechanism Based on Hybrid Wireless/Wired NoC for Efficient Barrier Synchronization in Parallel Computing
1246	Reliability-Oriented IEEE Std. 1687 Network Design and Block-Aware High-Level Synthesis for MEDA Biochips
1249	Designing Efficient Shortcut Architecture for Improving the Accuracy of Fully Quantized Neural Networks Accelerator
1250	Security Threats and Countermeasures for Approximate Arithmetic Computing
1272	Database and Benchmark for Early-stage Malicious Activity Detection in 3D Printing
1275	Boosting the Profitability of NVRAM-based Storage Devices via the Concept of Dual-Chunking Data Deduplication
1285	"RRAM-VAC: A Variability-Aware Controller for RRAM-based Memory Architectures"
1286	Small-Area and Low-Power FPGA-Based Multipliers using Approximate Elementary Modules
1290	Parallel-Log-Single-Compaction-Tree: Flash-Friendly Two-Level Key-Value Management in KVSSDs
1292	CRANIA: Unlocking Data and Value Reuse in Iterative Neural Network Architectures
1295	Efficient Subquadratic Space Complexity Digit-Serial Multipliers over $GF(2^m)$ based on Bivariate Polynomial Basis Representation
1297	Maximizing the Communication Parallelism for Wavelength-Routed Optical Networks-on-Chips