



# Call for Papers ASP-DAC 2021

<http://www.aspdac.com/>

January 18-21, 2021

Miraikan (The National Museum of Emerging  
Science and Innovation), Tokyo, Japan

## Aims of the Conference:

ASP-DAC 2021 is the 26th annual international conference on VLSI design automation in Asia and South Pacific regions, one of the most active regions of design and fabrication of silicon chips in the world. The conference aims at providing the Asian and South Pacific CAD/DA and Design community with opportunities of presenting recent advances and with forums for future directions in technologies related to Electronic Design Automation (EDA). The format of the meeting intends to cultivate and promote an instructive and productive interchange of ideas among EDA researchers/developers and system/circuit/device designers. All scientists, engineers, and students who are interested in theoretical and practical aspects of VLSI design and design automation are welcomed to ASP-DAC. **In light of the continued Covid-19 pandemic situation, the format of the conference is subject to future change. The options include fully in-person conference, hybrid conference (in person plus live video presentation) and fully virtual conferences. All papers presented, whether in-person or online, will be published. Please check the ASP-DAC 2021 website for updates.**

## Areas of Interest:

Original papers in, but not limited to, the following areas are invited.

### [1] System-Level Modeling and Design Methodology:

- 1.1. HW/SW co-design, co-simulation and co-verification
- 1.2. System-level design exploration, synthesis, and optimization
- 1.3. System-level formal verification
- 1.4. System-level modeling, simulation and validation tools/methodology
- 1.5. Networks-on-chip and NoC-based system design

### [2] Embedded Systems and Cyberphysical Systems:

- 2.1. Many- and multi-core SoC architecture
- 2.2. IP/platform-based SoC design
- 2.3. Domain-specific architecture
- 2.4. Dependable architecture
- 2.5. Cyber physical system
- 2.6. Internet of things

### [3] Embedded Systems Software:

- 3.1. Kernel, middleware, and virtual machine
- 3.2. Compiler and toolchain
- 3.3. Real-time system
- 3.4. Resource allocation for heterogeneous computing platform
- 3.5. Storage software and application
- 3.6. Human-computer interface

### [4] Memory Architecture and Near/In Memory Computing:

- 4.1. Storage system and memory architecture
- 4.2. On-chip memory architectures and management: Scratchpads, compiler, controlled memories, etc.
- 4.3. Memory and storage hierarchies with emerging memory technologies
- 4.4. Near-memory and in-memory computing
- 4.5. Memory architecture and management for emerging memory technologies

### [5] AI/Machine Learning System Designs:

- 5.1. Hardware and devices for deep neural networks
- 5.2. Design method for learning on a chip
- 5.3. Systems and design methods for deep neural computing
- 5.4. Neural network acceleration co-design techniques
- 5.5. Design techniques for AI of Things

### [6] Photonic/RF/Analog-Mixed Signal Design:

- 6.1. Analog/mixed-signal/RF synthesis
- 6.2. Analog layout, verification, and simulation techniques
- 6.3. High-frequency electromagnetic simulation of circuit
- 6.4. Mixed-signal design consideration
- 6.5. Communication and computing using photonics

### [7] Approximate, Bio-Inspired and Neuromorphic Computing:

- 7.1. Circuit and system techniques for approximate and stochastic computing
- 7.2. Neuromorphic computing
- 7.3. CAD for approximate and stochastic systems
- 7.4. CAD for bio-inspired and neuromorphic systems

### [8] Logic/High-Level Synthesis and Optimization:

*Please note that each paper shall be accompanied by at least one different conference registration at the speaker's registration rate (e.g., two speaker registrations are needed for presenting two accepted papers). But any registered co-author can present the work at the conference. ACM and IEEE reserve the right to exclude a paper from distribution after the conference (e.g., removal from ACM Digital Library and IEEE Xplore) if the paper is not presented at the conference by the author of the paper. ASP-DAC does not allow double and/or parallel submissions of similar work to any other conferences, symposia, and journals.*

## Submission of Papers:

Deadline for submission: **5 PM AOE (Anywhere on earth) Jul. 26 (Sun), 2020**  
Notification of acceptance: **Sep. 13 (Sun), 2020**  
Deadline for final version: **5 PM AOE (Anywhere on earth) Nov. 6 (Fri), 2020**

For detailed instructions for submission, please refer to the "Authors' Guide" at: <http://www.aspdac.com/>

## ASP-DAC 2021 Chairs

General Chair:

Technical Program Chair:

Technical Program Vice Chair:

Toshihiro Hattori (Renesas Electronics Corporation)

Sheldon Tan (University of California, Riverside)

Masanori Hashimoto (Osaka University)

**Panels, Special Sessions, and Tutorials:** Suggestions and proposals are welcome and have to be addressed to the Conference Secretariat ([aspdac2021@aspdac.com](mailto:aspdac2021@aspdac.com)) no later than August 2 (Sunday), 2020.

**Contact:** Conference Secretariat: [aspdac2021@aspdac.com](mailto:aspdac2021@aspdac.com) TPC Secretariat: [aspdac2021-tpc@aspdac.com](mailto:aspdac2021-tpc@aspdac.com)

# Call for Designs

University LSI Design Contest

ASP-DAC 2021

<http://www.aspdac.com/>

January 18-21, 2021

Miraikan (The National Museum of Emerging Science and Innovation), Tokyo, Japan



## Aims of the Contest:

As a unique feature of ASP-DAC 2021, the University LSI Design Contest will be held. The aim of the Contest is to encourage education and research on VLSI design at universities and other educational organizations. We solicit designs that fit in one or more of the following categories:

- (1) Designed, and actually implemented on chips in universities or other educational organizations during the last two years;
- (2) Designs that report actual measurements from implementations;
- (3) Innovative design prototypes.

Interesting or excellent designs selected will be honored by providing the opportunities for presentation in a special session at the conference. Award(s) will be given to a few numbers of outstanding designs, selected from those presented at the conference.

## Areas of Design:

Application areas or types of circuits of the original LSI circuit designs include (but are not limited to):

- (1) Analog, RF and Mixed-Signal Circuits, (2) Digital Signal Processing, (3) Microprocessors, (4) Custom ASIC.

Methods or technology used for implementation include:

- (a) Custom ASIC and Cell-Based LSIs, (b) Gate Arrays, (c) FPGA/PLDs.

## Submission of Design Descriptions:

A camera-ready summary is requested to be prepared within 2 pages including figures, tables, and references. It is strongly recommended that measured experimental results and a chip micrograph are included in the summary.

Specification of the submission format will be available at <http://www.aspdac.com/>

<b>Deadline for summary:</b>	5 PM AOE (Anywhere on earth)	July 26 (Sun), 2020
<b>Notification of acceptance:</b>		Sep. 13 (Sun), 2020
<b>Deadline for camera-ready:</b>	5 PM AOE (Anywhere on earth)	Nov. 6 (Fri), 2020

Please note that each paper shall be accompanied by at least one different conference registration at the speaker's registration rate (e.g., two speaker registrations are needed for presenting two accepted papers). But any registered co-author can present the work at the conference. ACM and IEEE reserve the right to exclude a paper from distribution after the conference (e.g., removal from ACM Digital Library and IEEE Xplore) if the paper is not presented at the conference by the author of the paper. Please do not submit the same paper as a regular paper.

## Review:

Submitted designs will be reviewed by the Design Contest Committee in a process similar to the review process for the technical papers. The following criteria will be applied in the selection of designs:

- (1) Reliability of design and implementation, (2) Quality of implementation, (3) Performance of the design, (4) Novelty of application, algorithm, architecture, (5) Others.

Interesting or excellent designs selected will be presented at a special session of the conference.

## Presentation:

An author of each selected design will be required to make a short presentation at a special session of ASP-DAC 2021.

A digest of each design to be presented will be included in the conference proceedings. **In light of the continued Covid-19 pandemic situation, the format of the conference is subject to future change. The options include fully in-person conference, hybrid conference (in person plus live video presentation) and fully virtual conferences.**

**All papers presented, whether in-person or online, will be published. Please check the ASP-DAC 2021 website for updates.**

Contact Email: [aspdac2021-udc@aspdac.com](mailto:aspdac2021-udc@aspdac.com)

ASP-DAC 2021 Chairs	General Chair:	Toshihiro Hattori (Renesas Electronics Corp., Japan)
	Technical Program Chair:	Sheldon Tan (University of California, Riverside, USA)
	Technical Program Vice Chair:	Masanori Hashimoto (Osaka University, Japan)
	Design Contest Co-Chairs:	Kousuke Miyaji (Shinshu University, Japan)
		Akira Tsuchiya (The University of Shiga Prefecture, Japan)

Prospective Sponsors: ACM SIGDA, IEEE CASS, IEEE CEDA, IEICE ESS, IPSJ SIGSLDM