Common-Centroid Layout for Active and Passive Devices: A Review and the Road Ahead

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Background

- Analog circuits
  - Often use large-sized devices/passives
    - Divided into unit structures laid out in an array
  - Sensitive to differential mismatch
    - Process variations are a major contributor

Common centroid

Differential pair

Interdigitated

[Karmokar, DATE22]

[Spanos, ISQED05]

[Sharma, DATE21]
Variation Models

- Die-to-die variations
- Within-die random variations
  - Uncorrelated
  - Spatially correlated
- Systematic variations
  - Gradient variations
  - Layout-dependent effects (LDEs)

[Kuhn, 2010]
[Sharma, ICCAD21]
Common-Centroid Layout

- Set the centroid of unit cells of A to be the same as that of B

\[
\frac{1}{s_A} \sum_{i=1}^{s_A} x^A_1 = \frac{1}{s_B} \sum_{i=1}^{s_B} x^B_2
\]

- Can be extended to more devices

- Cancels out systematic process gradients

\[
\Delta P = S_p \Delta p
\]

\[
\Delta p = \alpha \cdot x
\]

\[
\Delta P = \alpha S_p \cdot x
\]
Trends in FinFET Technologies and Beyond

• High wire/via resistances
  – Bends discouraged
• Unidirectional transistors
• Gridded, unidirectional wires
• “Unit cells” for transistors
• Self-heating/electromigration issues

[Source: anandtech.com]

[Hou, ISSCC2017]
Capacitor Layout

- **Types of capacitors**

- **Systematic mismatch**

  Process gradients

\[
C_k^* = \sum_k C_u \frac{t_0}{t_k}
\]

where

\[
t_k = t_0 + \gamma(x_k \cos \theta + y_k \sin \theta)
\]

**Process gradients**

\[
M_{sys} = \max_{p,q \in \{1, \ldots, n\}, p \neq q} \left| \frac{(C_p^* / C_q^*) - (C_p / C_q)}{C_p / C_q} \right|
\]

[Wang, DAC20]
Random Mismatch

- Correlation function
  \[ \rho_s(r) = (\rho_0)^r \]

- For \( C_p = p C_u, C_q = q C_u \)
  \[ \rho_{pq} = \frac{Cov(p, q)}{\sigma_p \sigma_q} \]

- Metrics
  \[ \rho_{avg} = \frac{1}{C(t, 2)} \sum_{p=1}^{t-1} \sum_{q=p+1}^{t} \rho_{pq} \]

  \[ M_{rand} = \max_{p, q \in \{1, \ldots, n\}, p \neq q} \text{var} \left( \frac{C_p}{C_q} \right) \]
Circuit Performance Metrics

• Charge-sharing DAC

\[
DNL_i = \frac{V_{OUT}(i + 1) - V_{OUT}(i) - V_{LSB}}{V_{LSB}}, \quad \forall i = 0, \ldots, 2^{N-1}.
\]

\[
INL_i = \frac{V_{OUT}(i) - V_{OUT}^{\text{ideal}}(i)}{V_{LSB}}, \quad \forall i = 0, \ldots, 2^{N-1}.
\]
CC Capacitor Layout Methods

- **Heuristic**
  - No guarantee of optimality (and sometimes correctness)

- **ILP**
  - Place unit capacitors and wires into “slots”

- **Structured methods**
  - Chessboard layout

<table>
<thead>
<tr>
<th>(a) $k = N$</th>
<th>(b) $k = N - 1$</th>
<th>(c) placement $P_1$</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image" alt="Chessboard layout" /></td>
<td><img src="image" alt="Chessboard layout" /></td>
<td><img src="image" alt="Chessboard layout" /></td>
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</tbody>
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- **Iterative methods**
  - Simulated annealing based perturbation of pair sequences with routability analysis

![Diagram](image)
FinFET-based CC Capacitor Layouts

- High via counts lead to high resistance $\rightarrow$ high RC delays $\rightarrow$ low 3dB frequency
- Alternative layout styles that reduce via counts are preferred
  - Chessboard layouts achieve good dispersion, high via count
  - Block chessboard (BC) layouts achieve a good compromise

(a) Spiral  
(b) Chessboard  
(c) BC (coarser)  
(d) BC (finer)  

[Karmokar, DATE22]
Transistor Layout

• Layout-dependent effects (LDEs)

  - Diffusion breaks require spaces, can create asymmetries

  - Transistor CC placement to maximize diffusion sharing

\[
\Delta V_{th} \propto \frac{1}{\text{LOD}} = \sum_{i=1}^{n} \left( \frac{1}{SA_i + 0.5L_g} + \frac{1}{SB_i + 0.5L_g} \right)
\]
CC Transistor Placement

Placement is followed by EM-aware/IR-drop-aware routing

[Sharma, ICCAD21]
When is CC Layout (Un)necessary?

Correlation length $R_L$

$\sigma_P^2 = \sigma_g^2 + \sigma_u^2 + \sigma_z^2$

CC is not beneficial when layout size $\ll R_L$
When is CC Layout (Un)necessary?

- LDEs affect the mean value: CC does not match LDEs

\[ V_{th} \propto \frac{1}{\text{LOD}} = \sum_{i=1}^{n} \left( \frac{1}{SA_i + 0.5L_g} + \frac{1}{SB_i + 0.5L_g} \right) \]

[Sharma, DATE21]
When is CC Layout (Un)necessary?

- Impact of parasitics

Magnitude of small-signal current for a unit cell: $I_{UA}$, $I_{UB}$ AC current (into the source): $\downarrow$ AC ground: $\triangledown$

[Sharma, DATE21]
Optimal Layouts May Differ from Block to Block

[Sharma, DATE21]
Conclusion

• CC layout is important in canceling systematic variations
• CC layout styles for transistor and passive arrays are widely used
• In FinFET technologies
  – Must be aware of correlation lengths
  – Must be aware of wire/via resistances
  – Avoid diffusion breaks
  – Consider alternatives to CC due to LDEs, wire parasitics, layout size