Chiplet Placement for 2.5D IC with Sequence Pair Based Tree and Thermal Consideration

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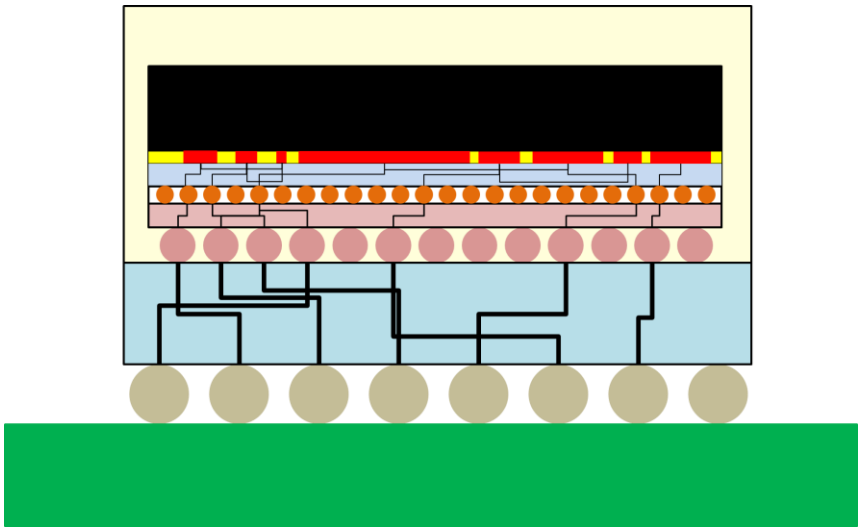
Outline

- Introduction
- The proposed framework
  - Placement with SP based tree
  - Post placement with thermal consideration
- Experimental results and summary

Introduction

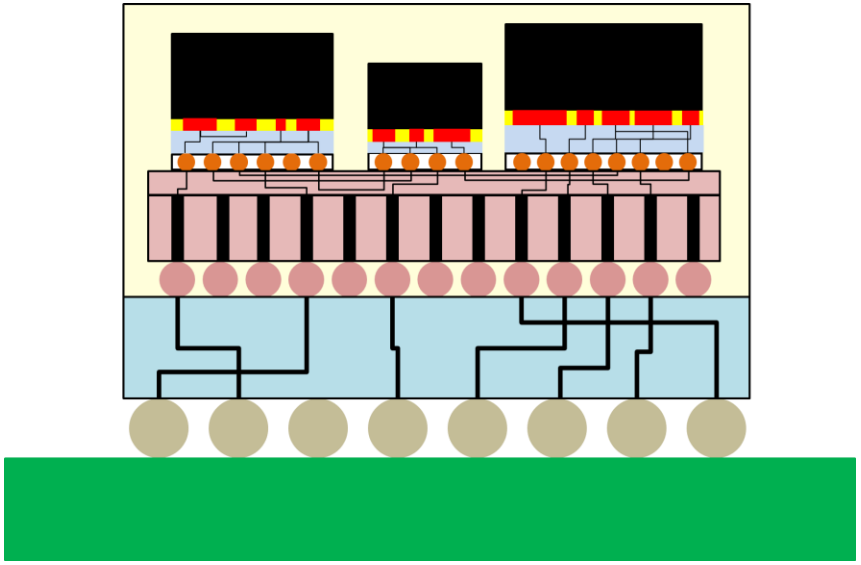
Introduction (1/5)
Motivation

While **"Moore's law"** approaches the physical limits...



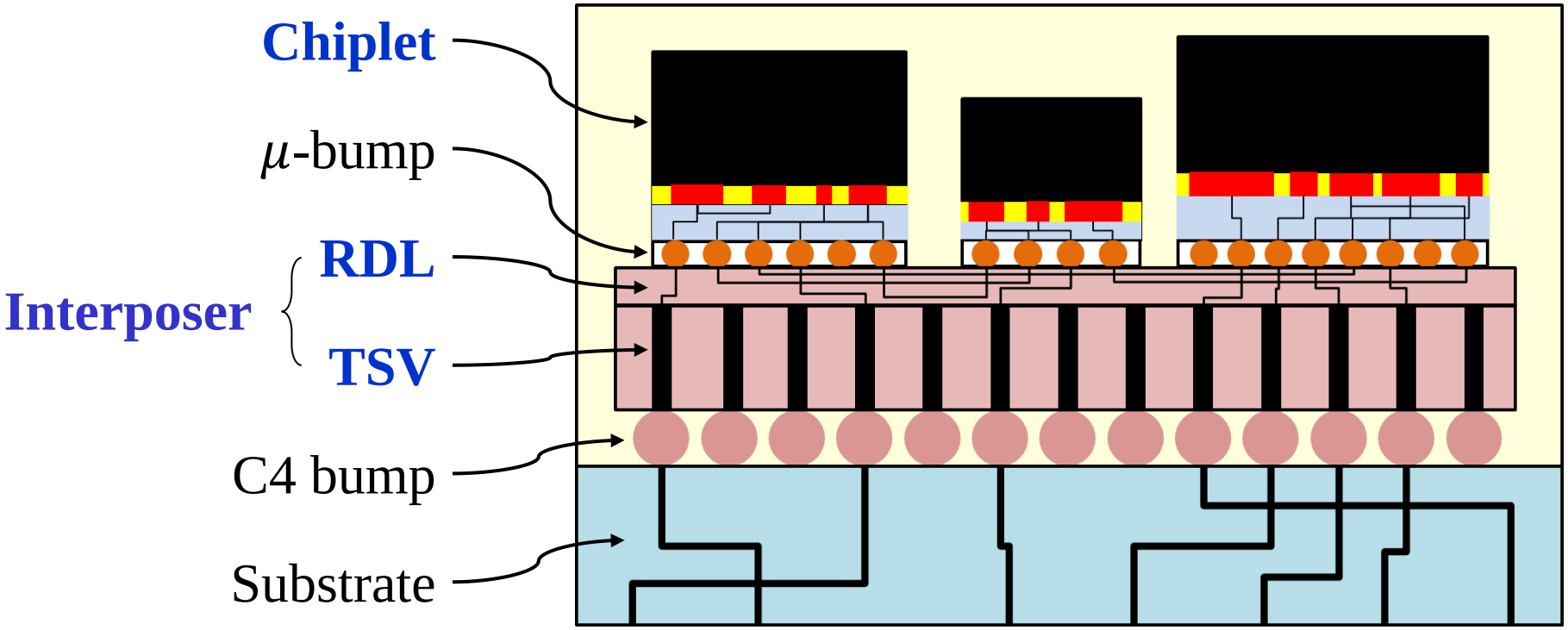
2D ICs

"More than Moore": 2.5D ICs, 3D ICs…



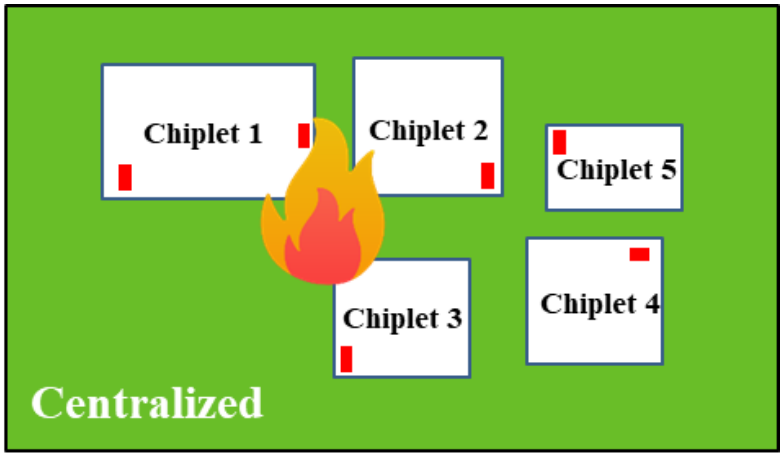
2.5D ICs

Introduction (2/5)
2.5D ICs

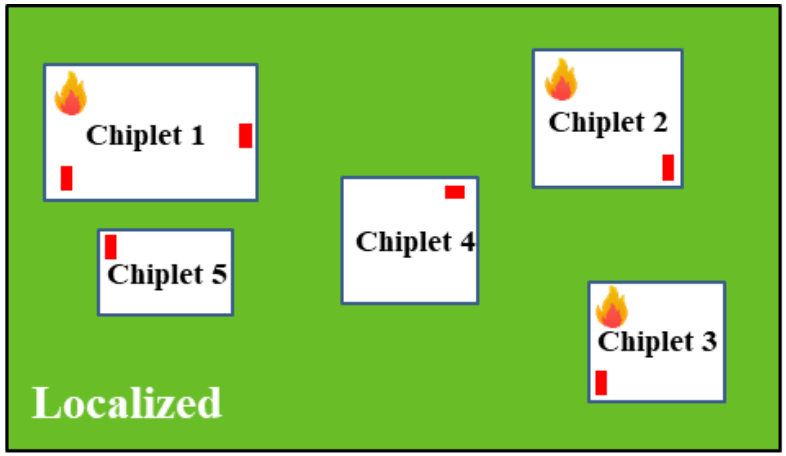


Introduction (3/5)
Thermal Issues on 2.5D ICs

When the chiplets are
placed together for optimal wirelength...



When the chiplets are
placed consider thermal effects…



Introduction (4/5)
Related Works

- Heuristic algorithms
  - Hierarchical B*-tree with SA [Ho et al., DAC'13]
  - Placement with SA & thermal constraint [Coskun et al., TCAD'20]
  - TAP-2.5D with thermal consideration [Ma et al., DATE'21]
- Combinatorial search algorithms
  - EFA with sequence pair [Liu et al., DAC'14]
  - Tree with CSP representation [Osmolovskyi et al., ASPDAC'18]

SA: simulated annealing
EFA: enumeration-based floorplanning algorithm
CSP: constraint-satisfaction problem
B&B: Branch-and-bound

Introduction (5/5)
Motivation and Contributions

- Causes
  - Heuristic algorithms may obtain sub-optimal WL-driven chiplet placement
  - Few number of chiplets (≈10) is popular in recent industry design
  - Few number of chiplets can be placed with **acceptable runtime by combinatorial search algorithms**
- Contributions
  - Build more efficient chiplet placer by combinatorial search algorithms
  - Develop post placement considering thermal effects

The Proposed Framework

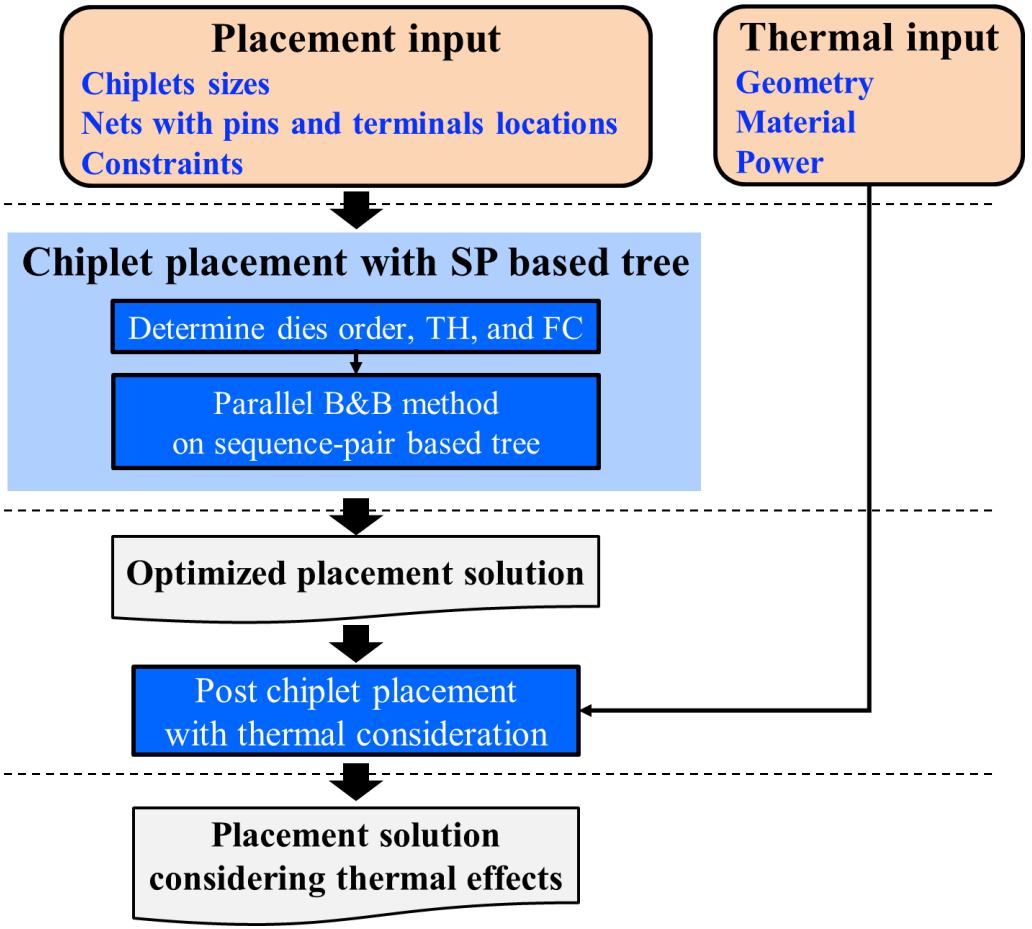
The Proposed Framework

1. **Placement/thermal input**
   Constraints:
   fixed outline with interposer size, space between chiplets (w_{space})

2. **Stage 1: WL-driven placement w/ SP based tree (SP-Tree)**

3. **Stage 2: Post placement with thermal effects**

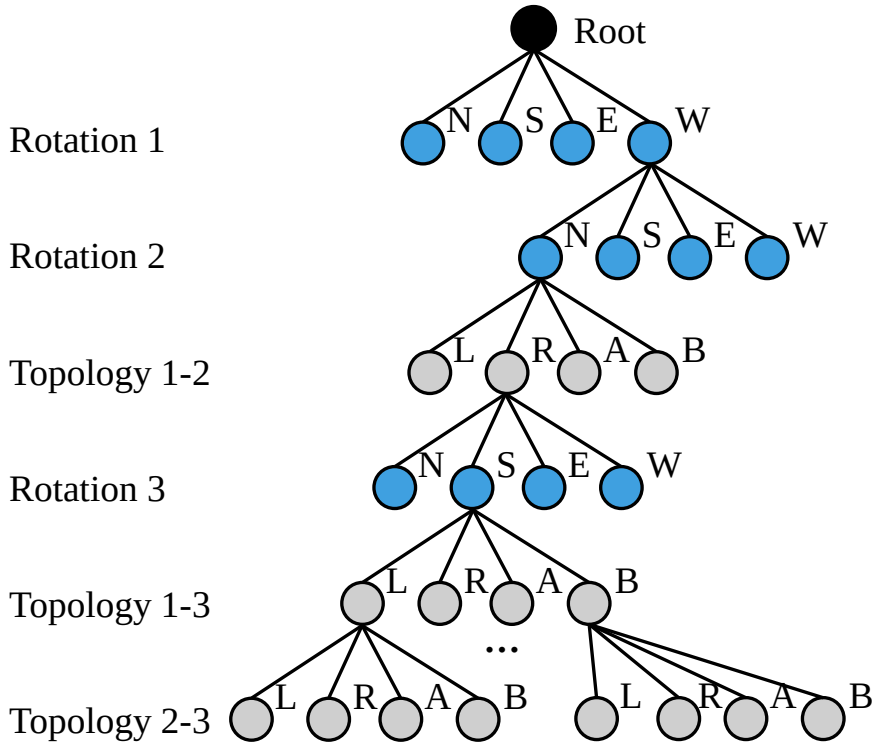
4. **Placement solution w/ thermal effects**



Placement with SP Based Tree

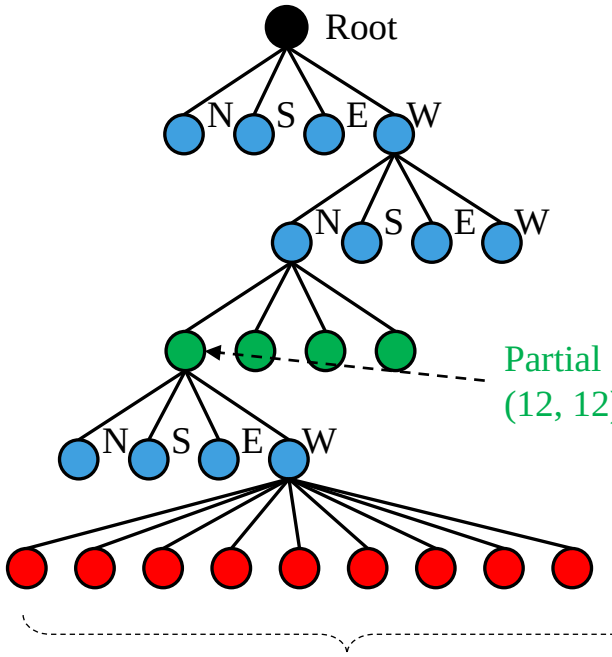
Placement with SP Based Tree (1/11)
Combinatorial Search Trees

CSP-Tree [ASPDAC'18]



Rotation and topology

SP-Tree (This work)



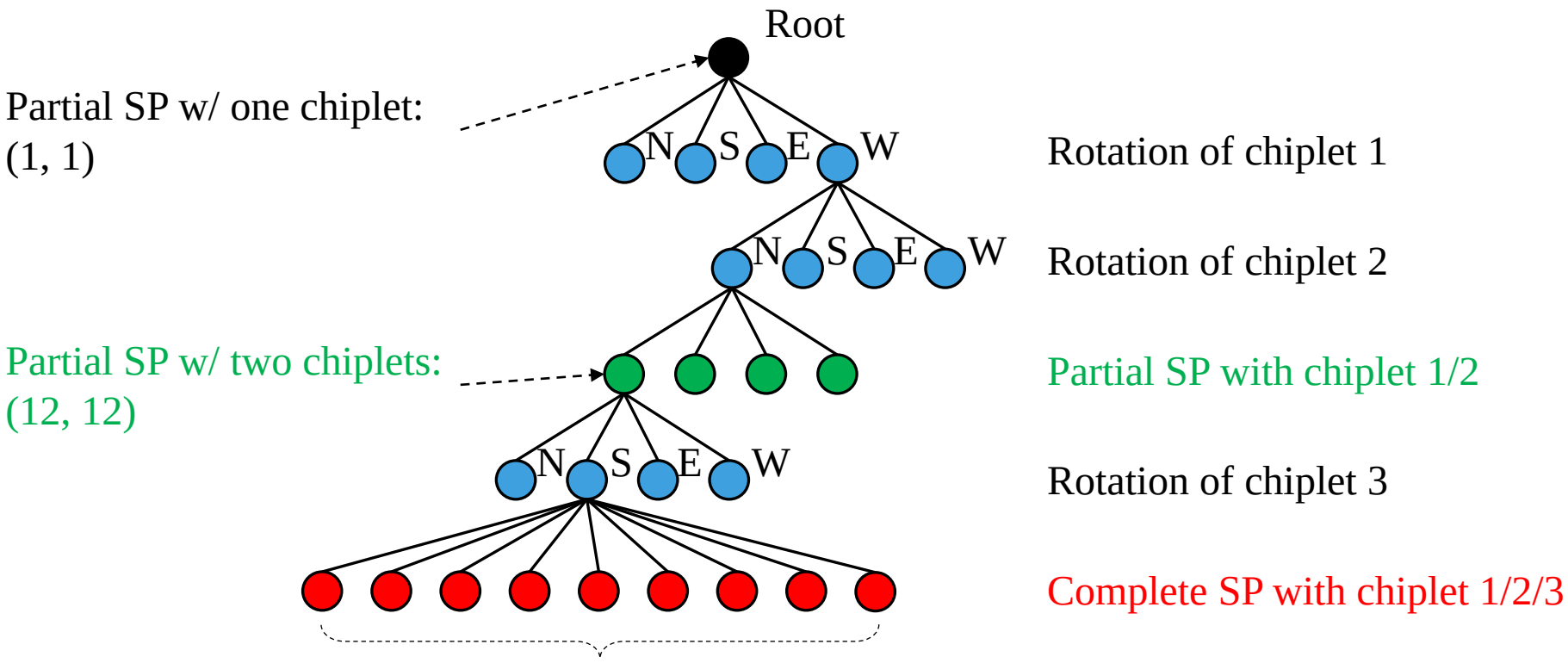
Complete SP w/ 3 chiplets: (312, 312) (312, 132) (312, 123) (132, 312) (132, 132) (132, 123) (123, 312) (123, 132) (123, 123)

Rotation and SP

Placement with SP Based Tree (2/11)

SP-Tree

Example of SP-Tree for case w/ three chiplets

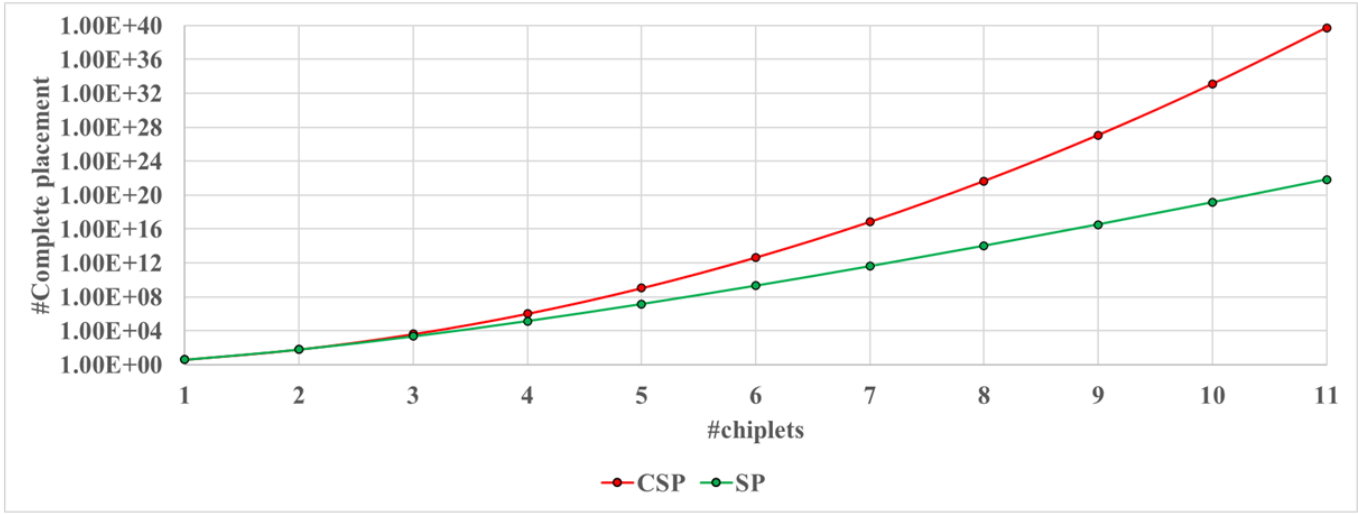


Complete SP w/ 3 chiplets: (312, 312) (312, 132) (312, 123) (132, 312) (132, 132) (132, 123) (123, 312) (123, 132) (123, 123)

Placement with SP Based Tree (3/11)
Solution Space for n Chiplets

- CSP-Tree [ASPDAC'18]
  - #complete placement: $4^n 4^{\frac{n(n-1)}{2}}$ (#rotation*#topology)
- SP-Tree (this work)
  - #complete placement: $4^n (n!)^2$ (#rotation*#SP)

#chiplets	#Complete placement	
	CSP	SP
1	4	4
2	64	64
3	4096	2304
4	1048576	147456
5	1073741824	14745600
6	4.39805E+12	2123366400
7	7.20576E+16	4.1618E+11
8	4.72237E+21	1.06542E+14
9	1.23794E+27	3.45196E+16
10	1.29807E+33	1.38078E+19
11	5.44452E+39	6.683E+21



All the numbers of complete placement are without pruning any nodes in this page

Placement with SP Based Tree (4/11)
Comparison on CSP-Tree and SP-Tree

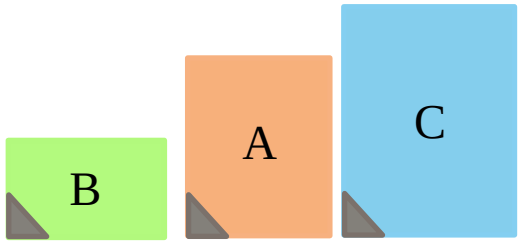
- Issue 1: Similar placement with the same SP

Example 1:

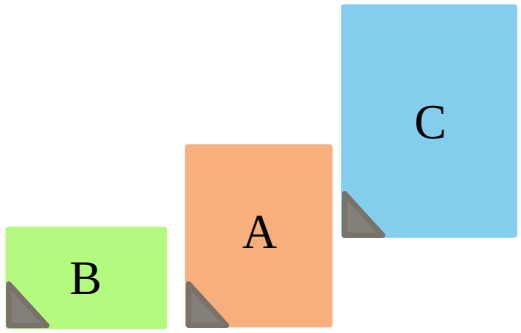
① BA relation: B is at left of A
② CA relation: C is at right of A
③ CB relation: C is at right of B

Example 2:

① BA relation: B is at left of A
② CA relation: C is at right of A
③ CB relation: C is at above of B



(BAC, BAC)



(BAC, BAC)

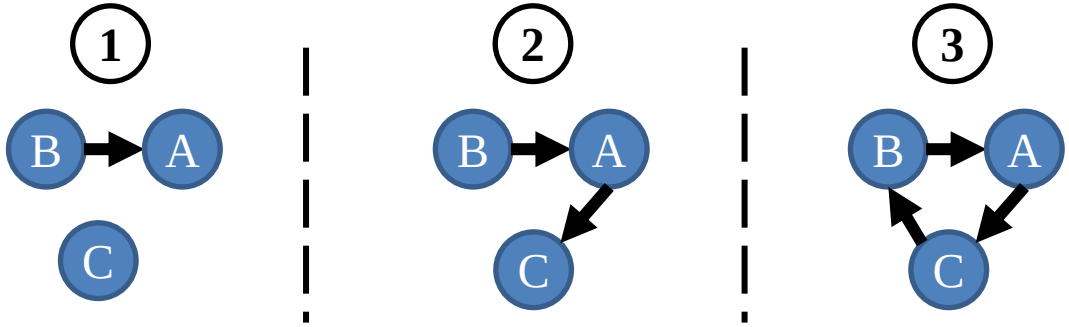
Placement with SP Based Tree (5/11)
Comparison on CSP-Tree and SP-Tree

- Issue 2: Illegal placement
  - All SP can be transformed to placement
  - Some CSP representation cannot be transformed to placement

Example 3:

① BA relation: B is at left of A
② CA relation: C is at right of A
③ CB relation: C is at left of B

Horizontal Constraint Graph

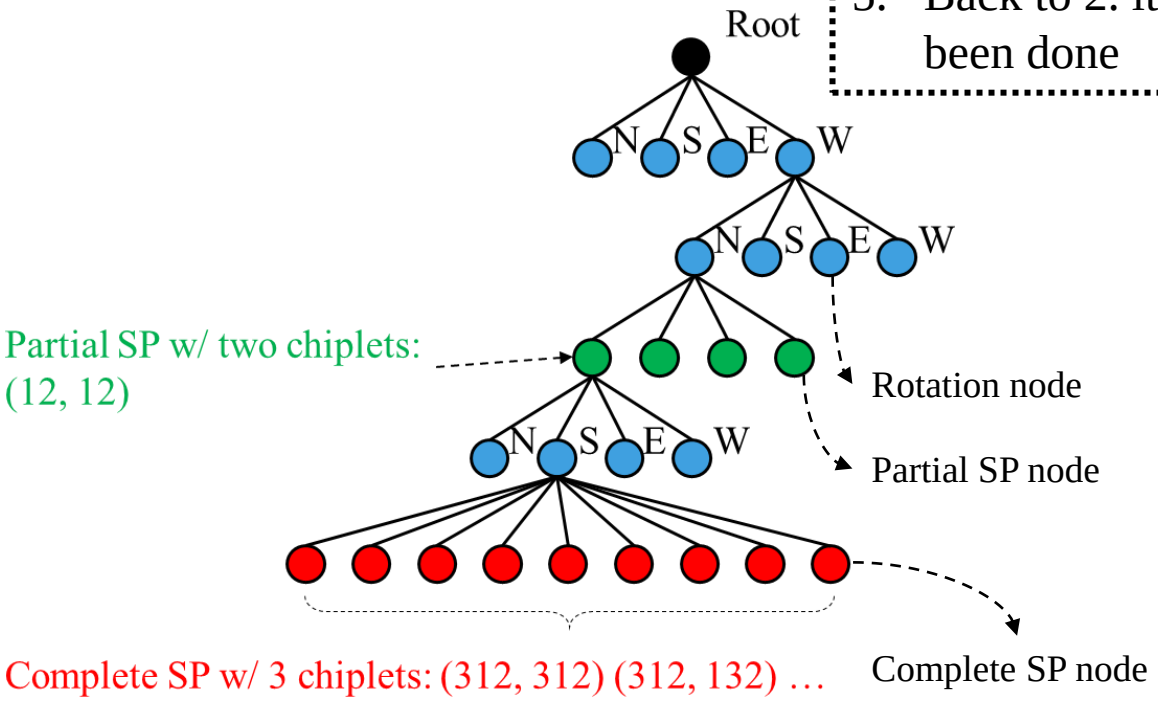


With loop, it's not a directed acyclic graph, thus it cannot be packed

Placement with SP Based Tree (6/11)
Parallel Branch and Bound Approach

Example for placement with three chiplets on "SP-Tree"

1. Branch the tree starting from root
2. Traverse the tree by depth first search (DFS)
3. Assign **rotation nodes** (*North*, *South*, *East*, *West*) or **partial/complete SP** (branch approach)
4. Bound approach
5. Back to 2. iteratively until all placement have been done



4. Bound approach
   a) The outline of placement exceeds the interposer size
   b) The estimated TWL of nodes (rotation & partial SP) > best TWL of complete SP node

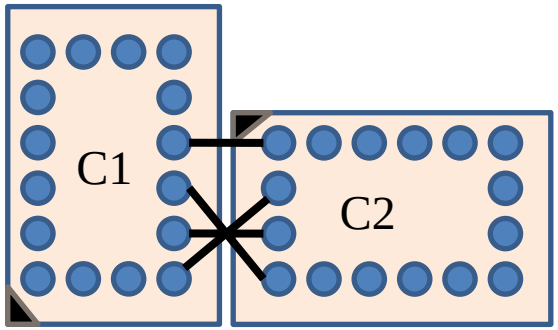
The B&B approach is parallelized with several stacks (used in DFS)

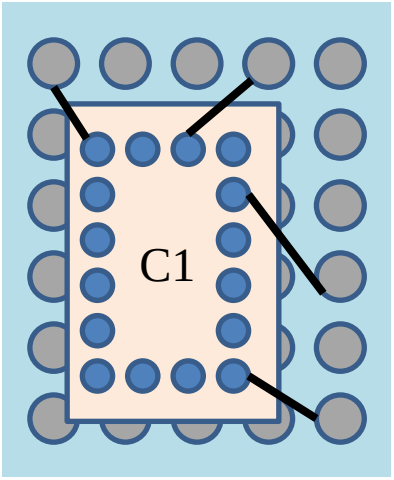
Placement with SP Based Tree (7/11)
Estimated Wirelength [ASPDAC'18]

Forward wirelength checking (FC) & Terminal handling (TH)

Topological nodes:
- Place two dies optimally "back-to-back" in all possible variations (rotations included)
- Calculate minimal WL of nets between the two dies

Rotational nodes:
- Align die (sitting alone) optimally to the interposer terminals
- Calculate minimal WL towards the terminals



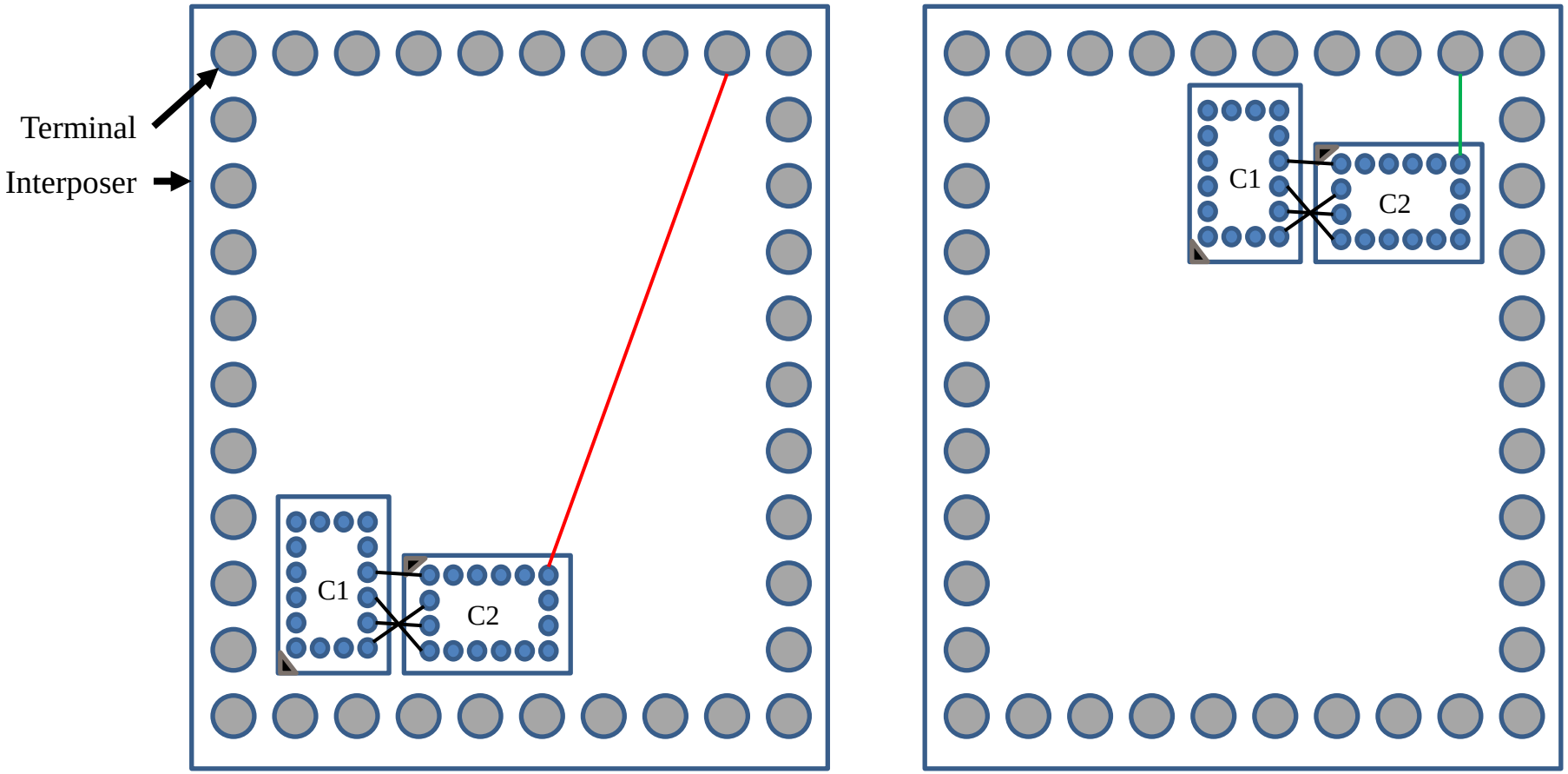


Placement with SP Based Tree (8/11)

Optimization w/ Whitespace

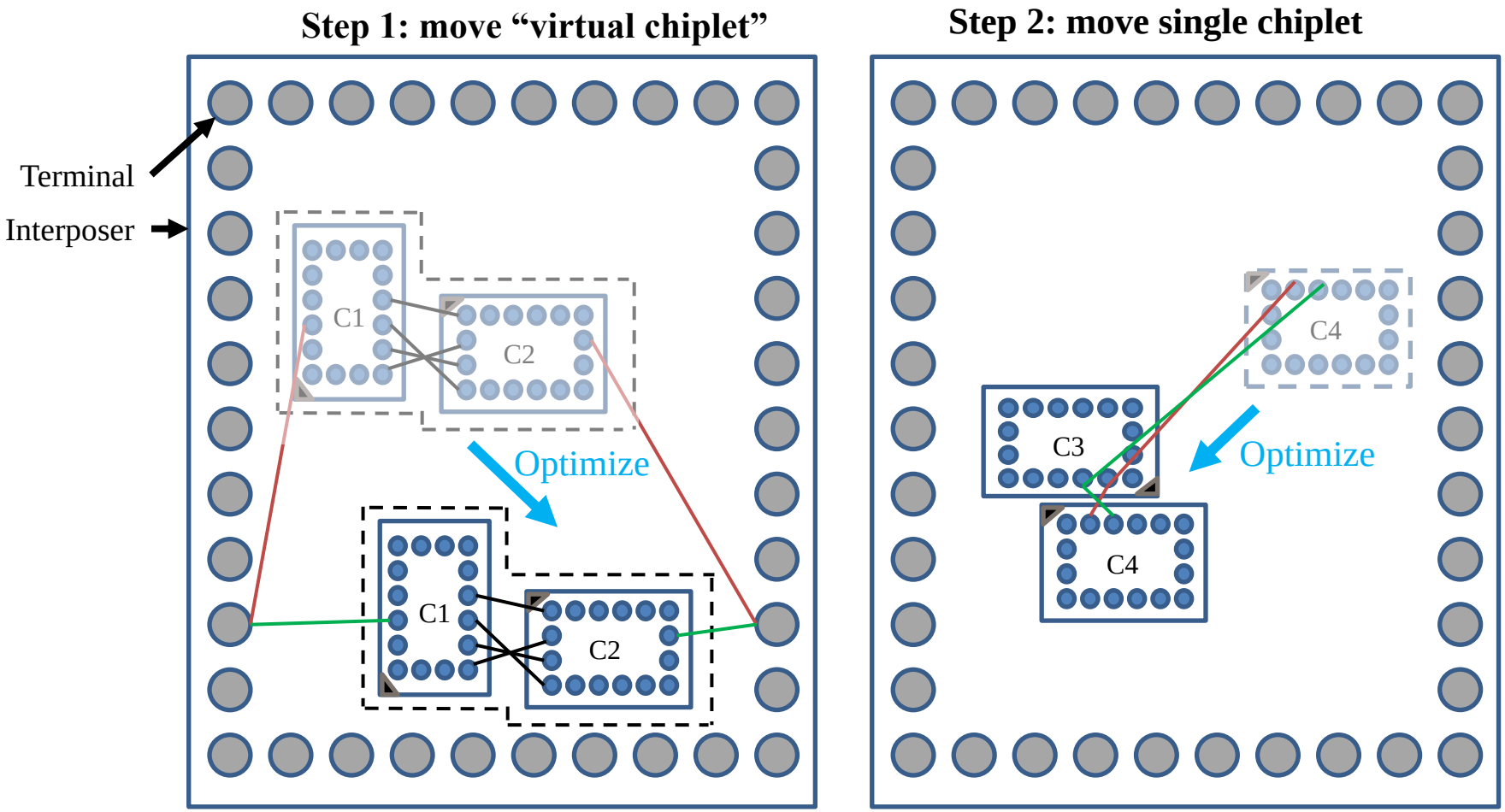
Optimization
w/o Whitespace

Optimization
w/ Whitespace



Placement with SP Based Tree (9/11)
Analytical Optimization w/ Whitespace

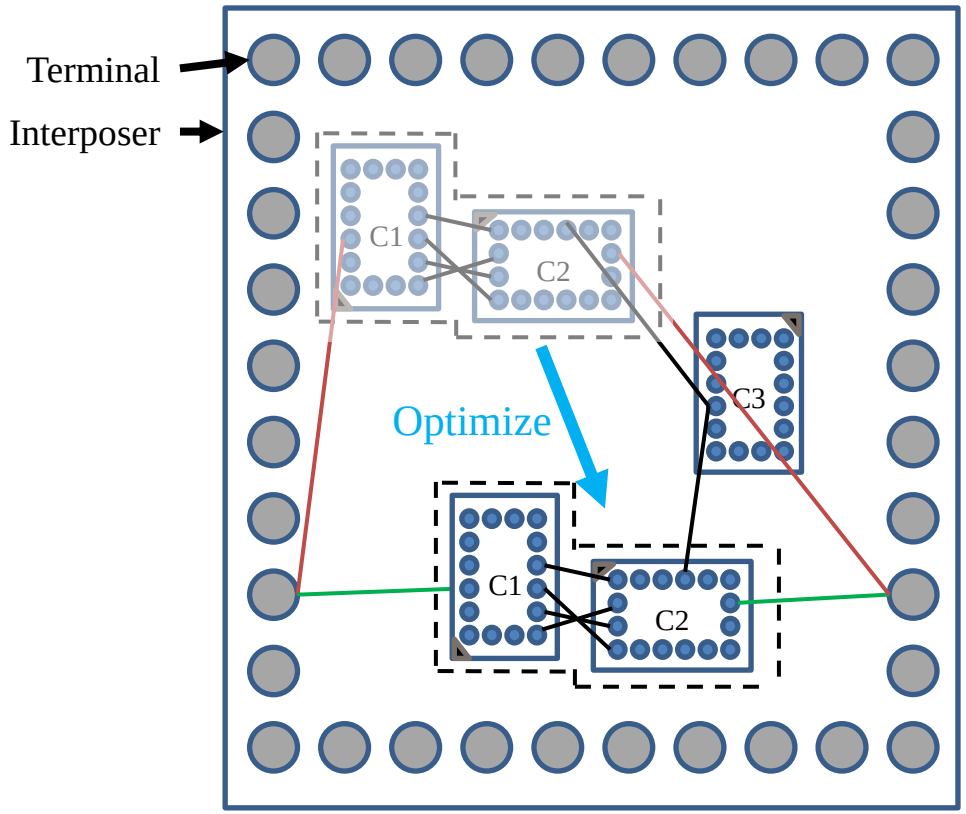
ASPDAC'18 used step 1/2



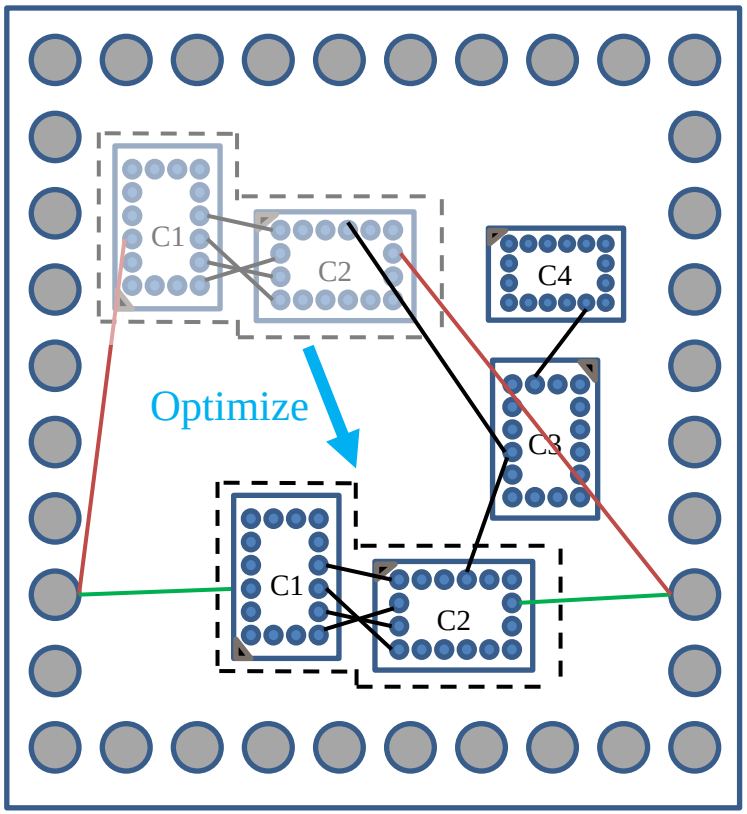
Placement with SP Based Tree (10/11)
Analytical Optimization w/ Whitespace

This work uses step 1/2 and the proposed step 3/4

Step 3: fix one chiplet,
then move others as "virtual chiplet"



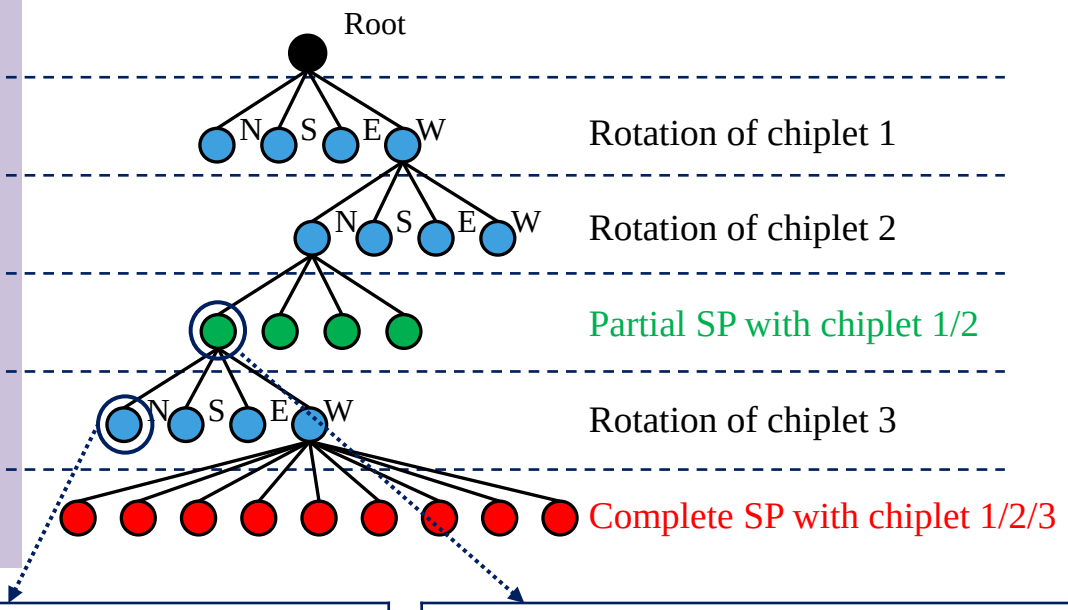
Step 4: fix two chiplet,
then move other as "virtual chiplet"



Placement with SP Based Tree (11/11)
An Example for SP-Tree

Currently best TWL = 36

Partial TWL	TH	RD
-	5	16
-	6	14
24	-	9
-	7	6
-	-	-



Rotation node
Estimated HPWL: $TWL_{partial,\ chiplet\ 2} + TH_{chiplet\ 3} + RD_{level5}$ 24+7+6=37 > 36 → **bound (pruning) this node**

Partial SP node
Estimated HPWL: $TWL_{partial,\ chiplet\ 2} + RD_{level4}$ 24+9=33 < 36 → **branch this node**

Post Placement with Thermal Consideration

Post Placement with Thermal Consideration (1/4)

- Thermal simulation for 2.5D ICs

$$\mathbf{G}T = P$$

$\mathbf{G}$: thermal conductance, T: temperatures, P: power values

- Mesh size is set as $64 * 64 * 5$ (the error is less than 1% compared to commercial tool Icepak)
- The heat transfer coefficient of top: 8700 W/m^2k
- The heat transfer coefficient of bottom: 2017 W/m^2k
- We solve T of chiplets directly using the matrix solver, SuperLU 5.3.0

Post Placement with Thermal Consideration (2/4)

- Post placement with thermal effects
  - One is ***moving only one chiplet at a time***
  - The other is ***moving all chiplets together***

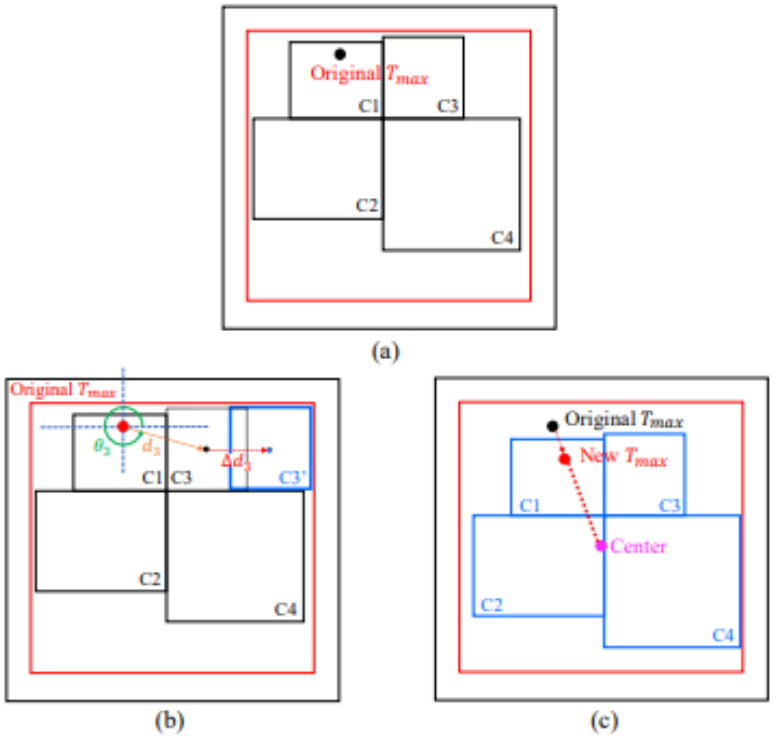
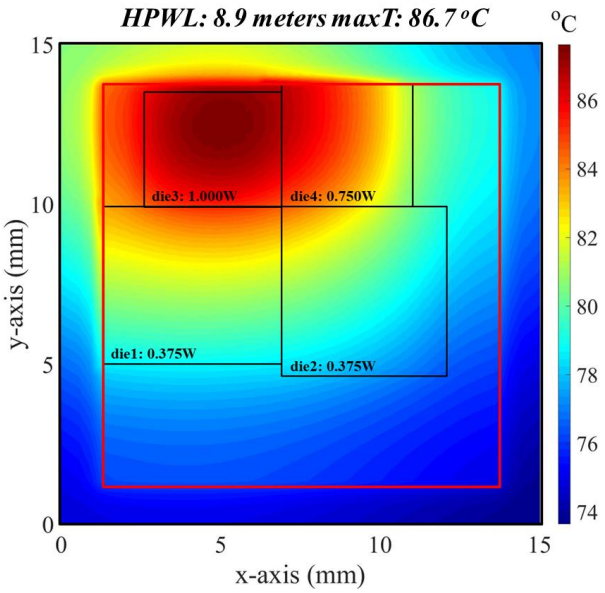


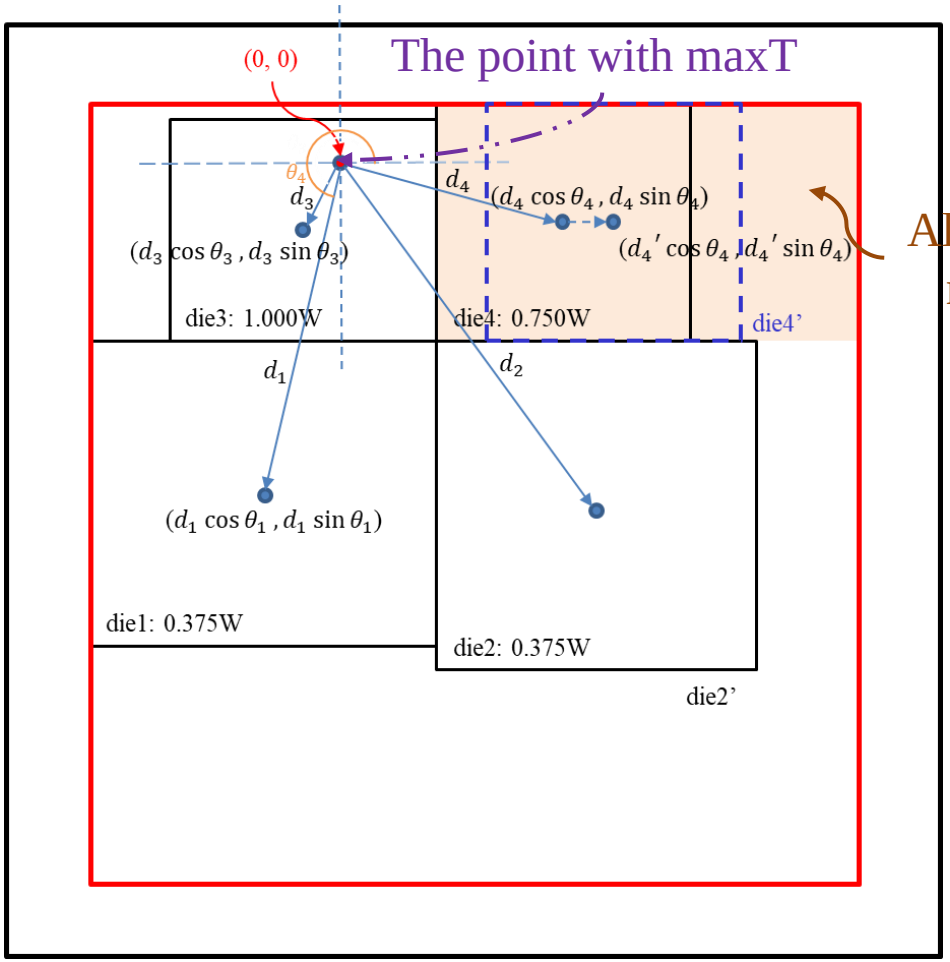
Figure 6: Placement refinement. (a) The original placement, (b) Move one chiplet (C3), (c) Move all chiplets (C1–C4).

Post Placement with Thermal Consideration (3/4)

Move 1: Move Single Chiplet

1. Calculate allowable region
2. Move die1 in the region

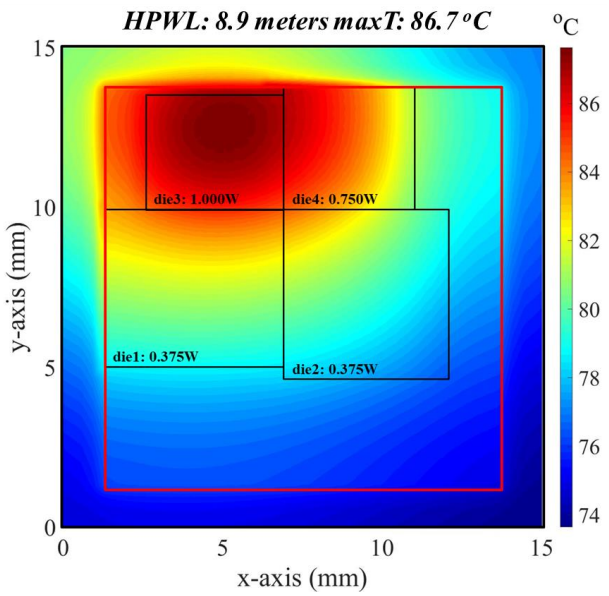


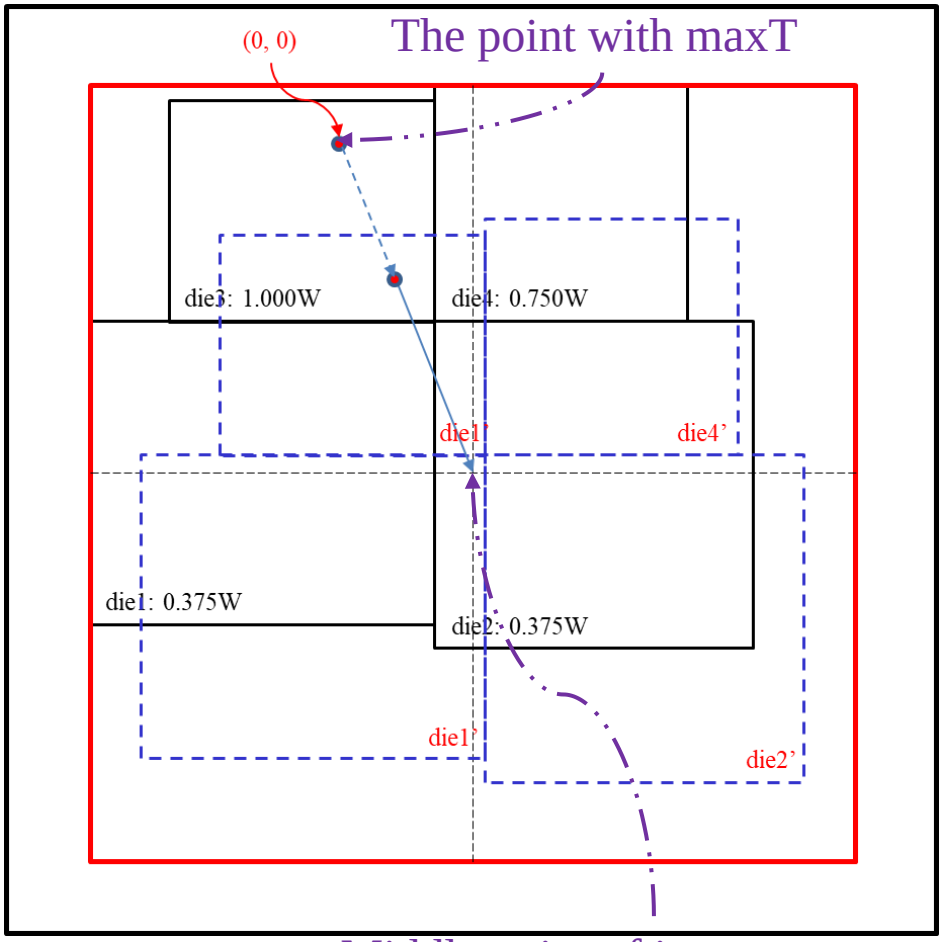


Post Placement with Thermal Consideration (4/4)

Move 2: Move Whole Chiplets

1. Move the whole chiplets (without changing their relative positions)





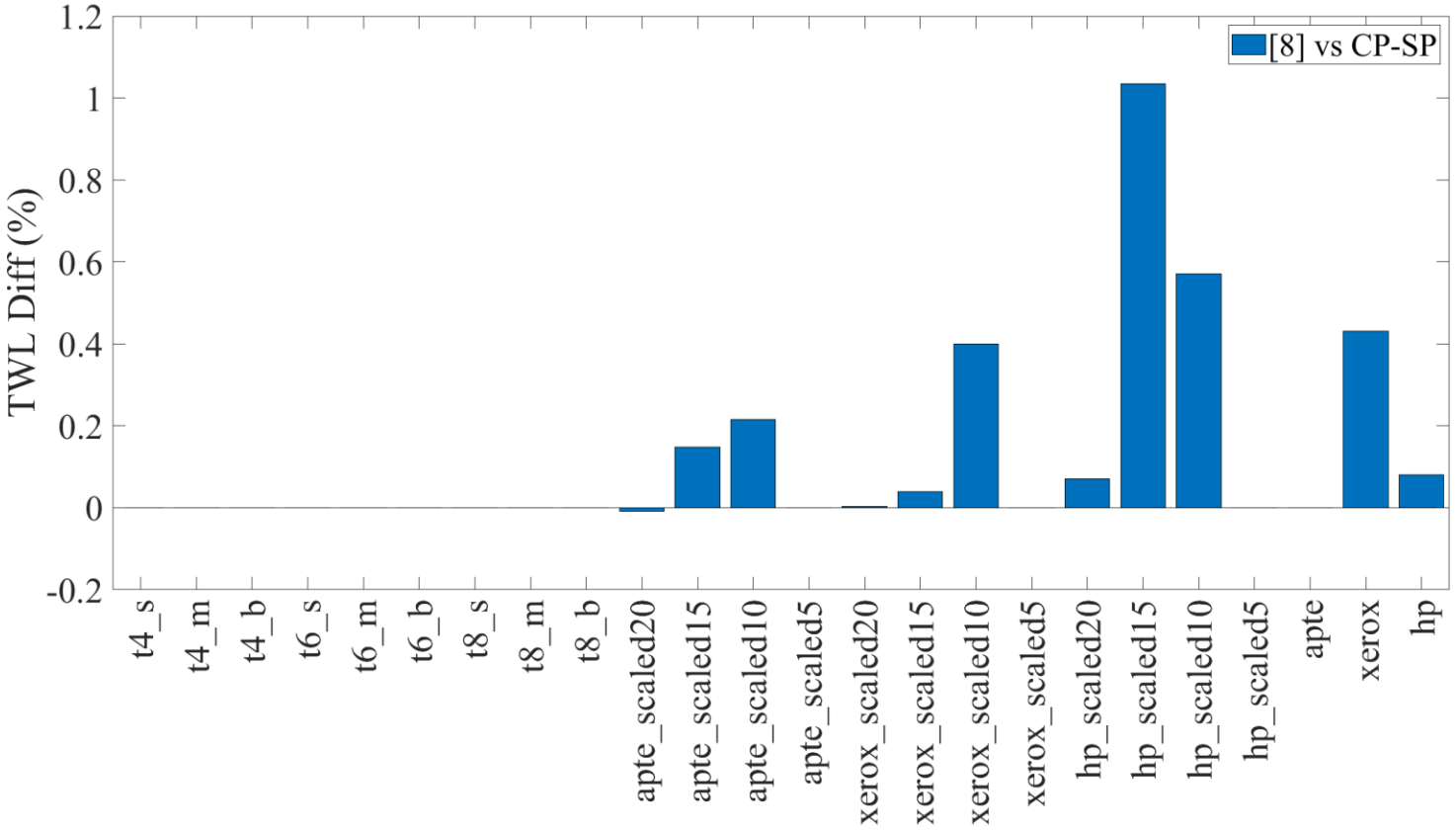
Experimental Results and Summary

Experimental Results (1/5)
Setup

- Programming with C/C++ language with compiler gcc 8.3.1
- Linux workstation with Intel CPU Xeon E5-2620 v4 at 2.10 GHz with #cores = 8
- Benchmark
  - Modified cases with #chiplets = 4, 6, 8 from [Liu et al., DAC'14] & [Osmolovskyi et al., ASPDAC'18]
  - Modified cases with #chiplets = 9, 10, 11 from MCNC benchmark & [Osmolovskyi et al., ASPDAC'18]

Experimental Results (2/5)
Wirelength-Driven Placement Comparison

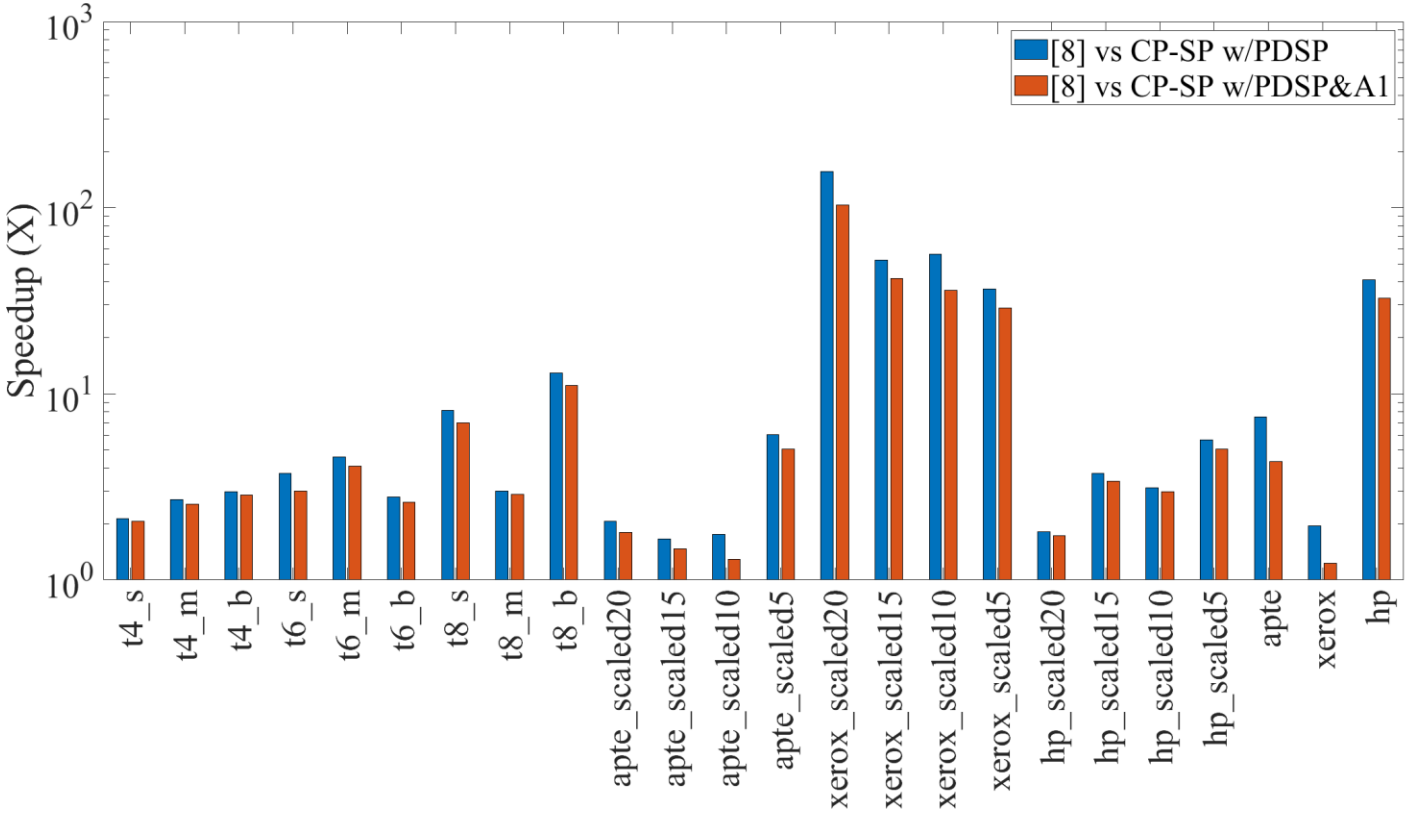
The optimized TWL of SP-CP is at most 1.035% better than [8]



[8] Sergii Osmolovskyi, Johann Knechtel, Igor L. Markov, Jens Lienig, Optimal Die Placement for Interposer-Based 3D ICs. Asia and South Pacific Design Automation Conference, pages 513-520, 2018. [ASPDAC'18]

Experimental Results (3/5)
Wirelength-Driven Placement Comparison

The speedup of SP-CP at most 156X than [8]



[8] Sergii Osmolovskyi, Johann Knechtel, Igor L. Markov, Jens Lienig, Optimal Die Placement for Interposer-Based 3D ICs. Asia and South Pacific Design Automation Conference, pages 513-520, 2018. [ASPDAC'18]

Experimental Results (4/5)
Placement with Thermal Consideration

Placement w/ SP-Tree (SP-CP) | **Placement w/ SP-Tree & post placement (SP-CP & Post-CP)**

Case	SP-CP			SP-CP & Post-CP					
	TWL (m)	Max. Temp. (℃)	Time (s)	TWL (m)	Max. Temp. (℃)	Time (s)	Increasing TWL (%)	Max. Temp. Reduction (℃)	Runtime Overhead (s)
apte_scaled30	0.40872	92.669	17.504	0.42707	84.455	75.605	4.490	8.214	58.101
apte_scaled25	0.40213	91.889	15.803	0.43193	84.979	87.846	7.411	6.910	72.043
apte_scaled20	0.39267	99.579	9.782	0.41887	94.562	83.610	6.672	5.017	73.828
apte_scaled15	0.41692	95.123	43.177	0.43818	91.556	88.489	5.099	3.567	45.312
xerox_scaled30	0.40664	88.631	149.792	0.42894	83.603	184.882	5.484	5.028	35.090
xerox_scaled25	0.42087	89.632	71.292	0.45233	84.673	187.037	7.475	4.959	115.745
xerox_scaled20	0.48135	87.810	192.405	0.50846	84.091	220.035	5.632	3.719	27.630
xerox_scaled15	0.51508	86.778	334.773	0.56097	84.918	344.944	8.909	1.860	10.171
hp_scaled30	0.16144	86.284	10.252	0.16362	84.773	23.564	1.350	1.511	13.312
hp_scaled25	0.19377	85.050	265.859	0.19617	84.584	320.769	1.239	0.466	54.910
Avg.							5.376	4.125	50.614

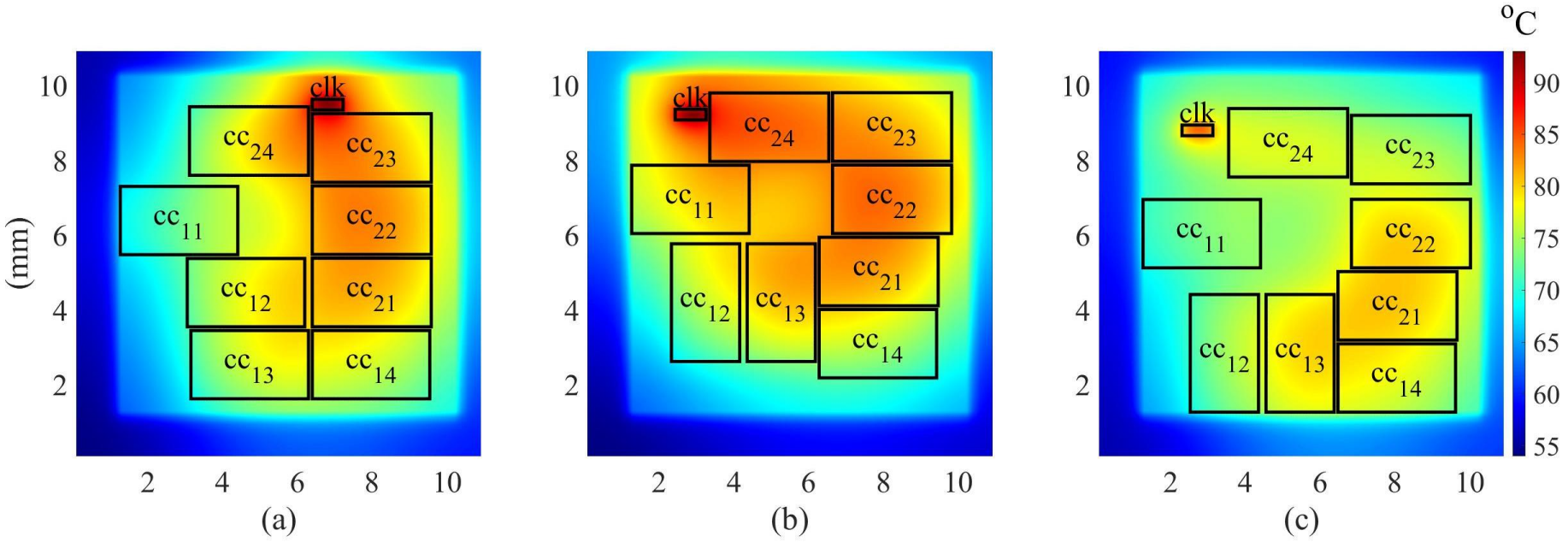
Satisfy thermal constraint 85 ℃

Not satisfied thermal constraint but reduced 3~5 ℃

Average runtime overhead: 50.614 seconds
Average increasing TWL: 5.376%

Experimental Results (5/5)
Placement with Thermal Consideration

Thermal Maps on case apte_scaled30



Optimal placement
TWL = 0.40872m (+0.00%)
maxT = 92.669 ℃

Sub-optimal placement
TWL = 0.41076m (+0.49%)
maxT = 90.308 ℃

Sub-optimal placement
TWL = 0.42707m (+4.48%)
maxT = 84.455 ℃

Summary

- Innovation
  - Propose a novel combinatorial search tree, called SP-Tree
  - Build parallel B&B chiplet placement on SP-Tree
  - Develop post placement with thermal consideration
- Achievements
  - The placer can speed up with at most **two order** than prior-art and **reduce 1% TWL** at most
  - The placer with thermal consideration can reduce the maximum temperature **up to 8.214 °C** with average **5.376% increasing TWL**

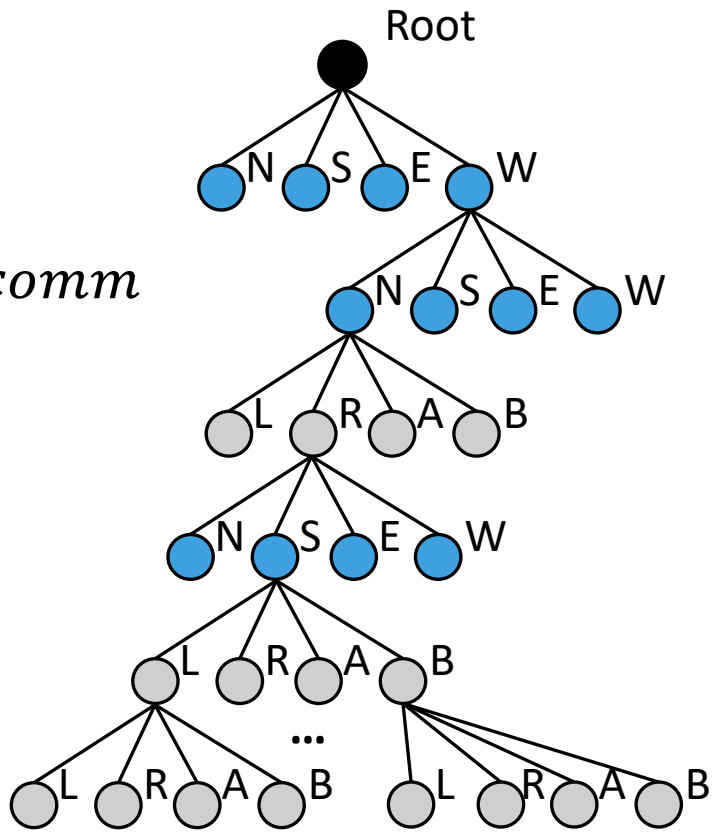
Appendix

Preliminary
Chiplet Ordering [ASPDAC'18]

- The order of chiplet addition can significantly affect the B&B process.

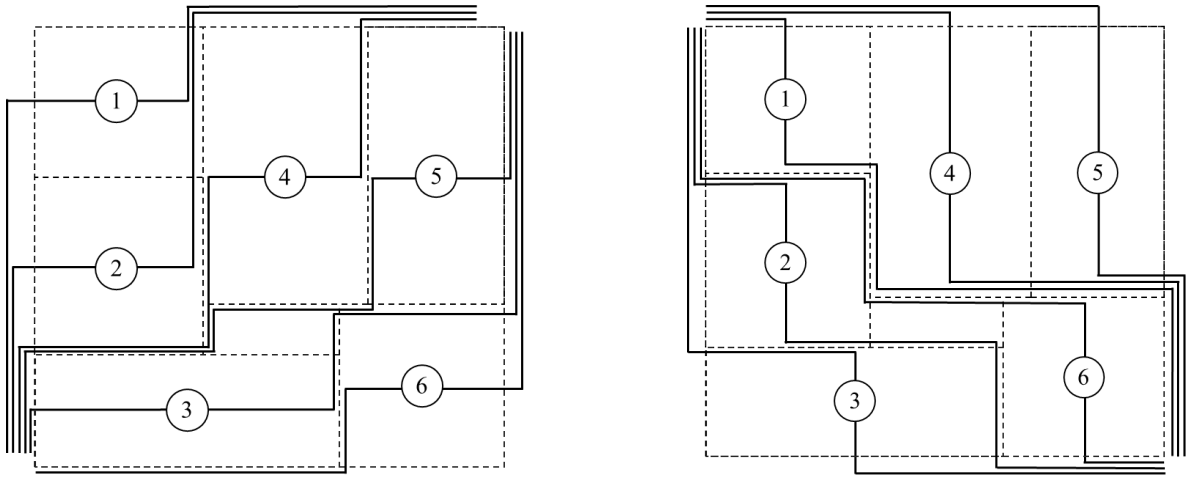
$$c_{i,j} = (w_i + h_i + w_j + h_j) \,/\, 2 \cdot n_{comm}$$

where $c_{i,j}$ is weight of the graph



Preliminary
Sequence Pair Representation

- Sequence pair uses two sequences to express the topological relationship between blocks (chiplets)..
  - H-constraint: (...*i*...*j*..., ...*i*...*j*...) iff *i* is left of *j*
  - V-constraint: (...*i*…*j*..., ...*j*...*i*...) iff *j* is below *i*



$$(\Gamma_+, \Gamma_-) = (124536, 326145)$$

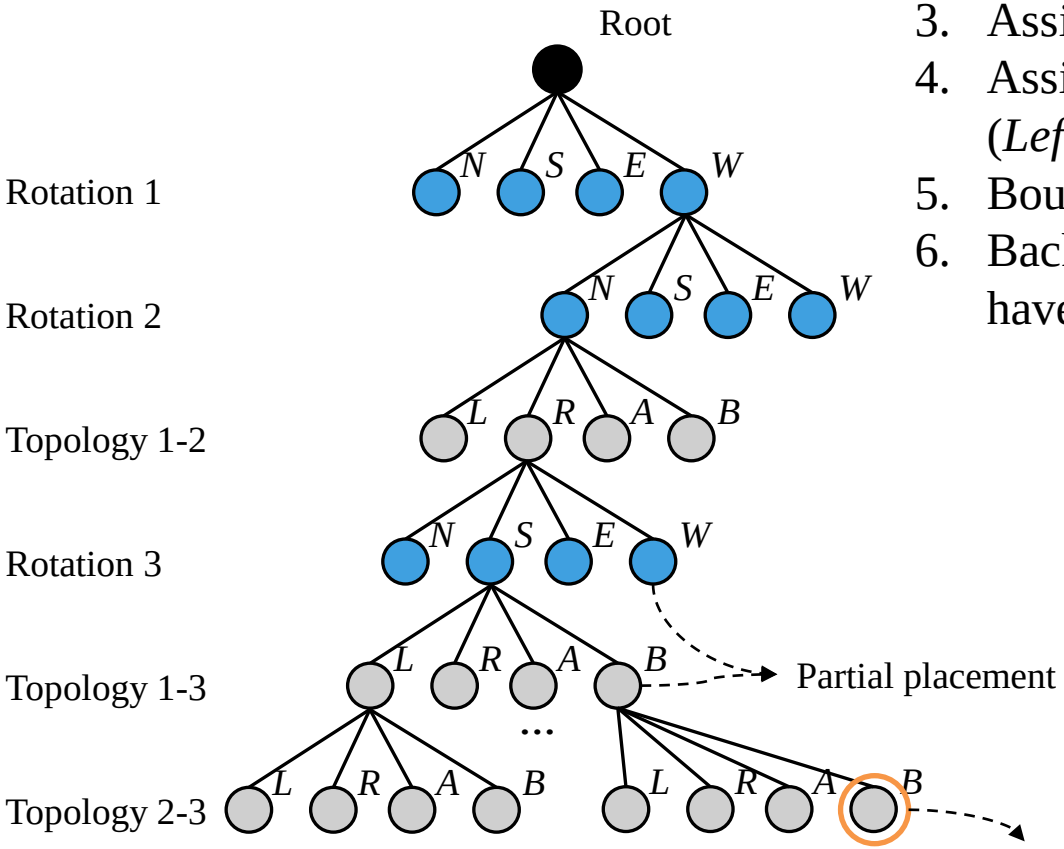
[14] H. Murata, K. Fujiyoshi, S. Nakatake, and Y. Kajitani, “VLSI module placement based on rectangle-packing by the sequence-pair,”IEEE TCAD, vol. 15, no. 12, pp. 1518–1524, 1996

Wang, Laung-Terng, Yao-Wen Chang, and Kwang-Ting Tim Cheng, eds. *Electronic design automation: synthesis, verification, and test*. Morgan Kaufmann, 2009.

Preliminary
Branch and Bound Method for CSP-Tree

Branch Approach

Example for placement with three chiplets for CSP-Tree



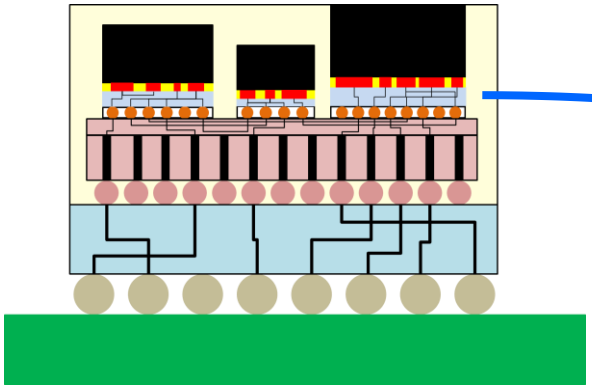
1. Branch the tree start from root
2. Traverse the tree by depth first search
3. Assign **rotations** (*North*, *South*, *East*, *West*)
4. Assign **topology** for two adjacent chiplets (*Left*, *Right*, *Above*, *Below*)
5. Bound approach (next page, p. 10)
6. Back to 2. iteratively until all placement have been done

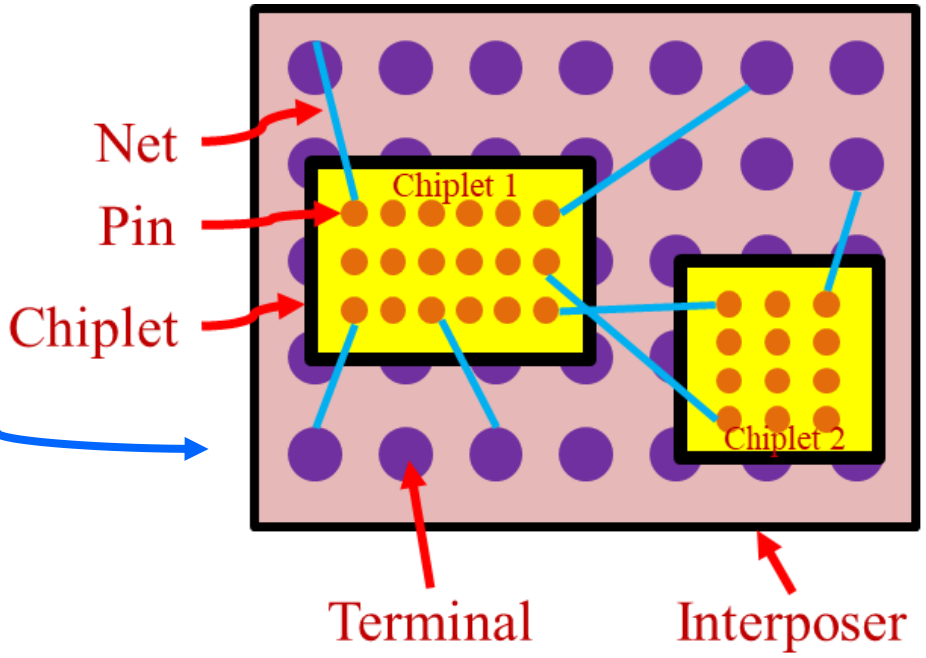
#Chiplets	#Complete placements
3	$4.096 * 10^3$
4	$1.048 * 10^6$
5	$1.073 * 10^9$
6	$4.398 * 10^{12}$

How to deal with **"trillions" of complete placements** efficiently?

Placement Information

- Terminologies
  - Chiplet: modules commonly designed beforehand
  - Net: wire
  - Pins: *micro bumps*
  - Terminals: *C4 bumps*





[1] Sergii Osmolovskyi, Johann Knechtel, Igor L. Markov, Jens Lienig, Optimal Die Placement for Interposer-Based 3D ICs. Asia and South Pacific Design Automation Conference, pages 513-520, 2018.

Problem Formulation

$$\min \quad \sum_{k}^{\#nets} HPWL_k \tag{2}$$

subject to

$$x_{left,i} \geq 0, W \geq x_{right,i},$$
$$y_{bottom,i} \geq 0, H \geq y_{top,i}. \tag{3a}$$

$$min\{\left|x_{left,i} - x_{right,j}\right|, \left|x_{left,j} - x_{right,i}\right|, \left|y_{bottom,i} - y_{top,j}\right|, \left|y_{bottom,j} - y_{top,i}\right|\} \geq w_{space}. \tag{3b}$$

$$cost = \phi * \frac{\mathrm{TWL} - \mathrm{TWL}^{opt}}{\mathrm{TWL}^{max} - \mathrm{TWL}^{opt}} + (1-\phi) * \frac{T_{max} - T_{max}^{min}}{T_{max}^{max} - T_{max}^{min}}, \tag{4}$$

where TWL^{max} is the maximum TWL, and T_{max}^{max} and T_{max}^{min} are the maximum and minimum of maximum temperatures of the placements with increasing TWL $< \eta\%$.

Placement with SP Based Tree (12/11)
Analytical Optimization w/ Whitespace

1. Place chiplets toward to the left and lower corner with sequence pair as default (with HCG/VCG)
   - To check that fixed outlined (interposer size) constraint is satisfied
2. Analytical optimize the chiplets placement w/ whitespace
   - $\min \sum_{i=1}^{\#nets} \left(\sum_{j,k=1;\ j \neq k}^{\#pins} (x_j - x_k)^2 \right) + \sum_{i=1}^{\#nets} \left(\sum_{j,k=1;\ j \neq k}^{\#pins} (y_j - y_k)^2 \right)$, subject to fixed outlined (interposer size) and space constraints

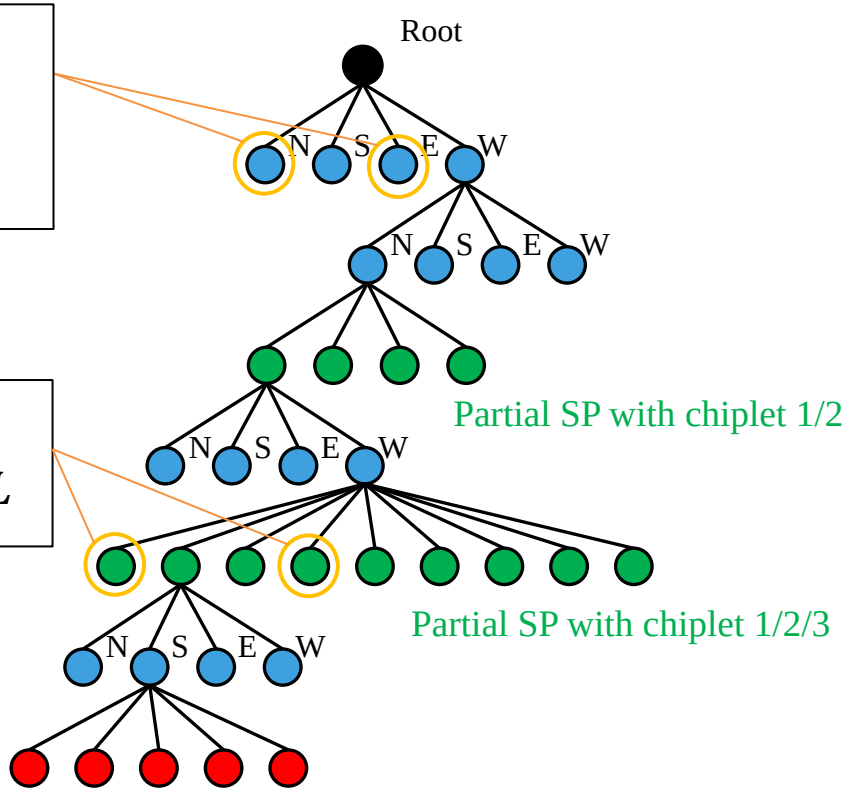
Placement with SP Based Tree (13/11)
Pruning Dominated Nodes for SP-Tree

- Pruned nodes which appear much worse than others at the same level in the SP-Tree

Criteria1: difference between WL estimations in same level > $\frac{1}{chiplets\ numbers+1} * bestTWL$ **[ASPDAC'18]**

Criteria 2: difference between WL estimations in same level > $\frac{1}{chiplets\ numbers+1} * \gamma[i] * bestTWL$

Example of SP-Tree for case w/ four chiplets



Placement with SP Based Tree (14/11)
Pruning Dominated Nodes for SP-Tree

- Pruned nodes which appear much worse than others at the same level in the SP-Tree

After insert C3 in SP (12, 12)

Partial SP	best estimated HPWL	$\alpha[i]$	$\gamma[i]$
(312, 312)			
(312, 132)	**vs (312, 312)**	1+0=1	1-1/3=2/3
(312, 123)		1+1=2	1-2/3=1/3
(132, 312)		1+0=1	1-1/3=2/3
(132, 132)		1+0=1	1-1/3=2/3
(132, 123)		1+1=2	1-2/3=1/3
(123, 312)		1+1=2	1-2/3=1/3
(123, 132)		1+1=2	1-2/3=1/3
(123, 123)		1+1=2	1-2/3=1/3

Example:
$\alpha[i]$ is difference between the partial SP at node i and the partial SP having the best estimated HPWL at the same level

1) (312, 312) and (312, 132) the topology of C3 and C1 is different. ⇒ this case contributes 1 to $\alpha[1]$.

2) (312, 312) and (312, 132) the topology of C3 and C2 is the same. ⇒ this case contributes 0 to $\alpha[1]$.

Then, we can get $\gamma[i] = 1 - (1+0)/3 = 2/3$

If $\alpha[i]$(difference) ↑, $\gamma[i]$ ↓, pruning criteria ↓

Placement with SP based tree (15/11)
Pruning Dominated Nodes for SP-Tree

Algorithm 1 Modified coefficient γ on the same level of partial SP

Input: integer array $[1, 2, ..., n^2]$ IP_1, IP_2 — Record the insertion positions of the chiplet inserted by two sequences
float array $[1, 2, ..., n^2]$ TWL

Output: float array $[1, 2, ..., n^2]$ γ

integer array $[1, 2, ..., n^2]$ α

$IP_{1min} = |\min(IP_1)|$;
$IP_{2min} = |\min(IP_2)|$; — Insertion position of the node with the minimum estimated HPWL

$n = n_k$;

for each $i \in [1, n^2]$ **do**

$IP_{gap}[i] = IP_1[i] - IP_2[i]$ — Record the gap between the insertion positions of these two sequences

$IP_{gap\ min} = IP_{1\ min} - IP_{2\ min}$

$\alpha[i] = (|IP_1[i] - IP_{1\ min}| + |IP_2[i] - IP_{2\ min}| + |IP_{gap}[i] - IP_{gap\ min}|)/2$; — $\alpha[i]$ is half of the sum of differences between insertion positions and minimum insertion positions at the same level

end for

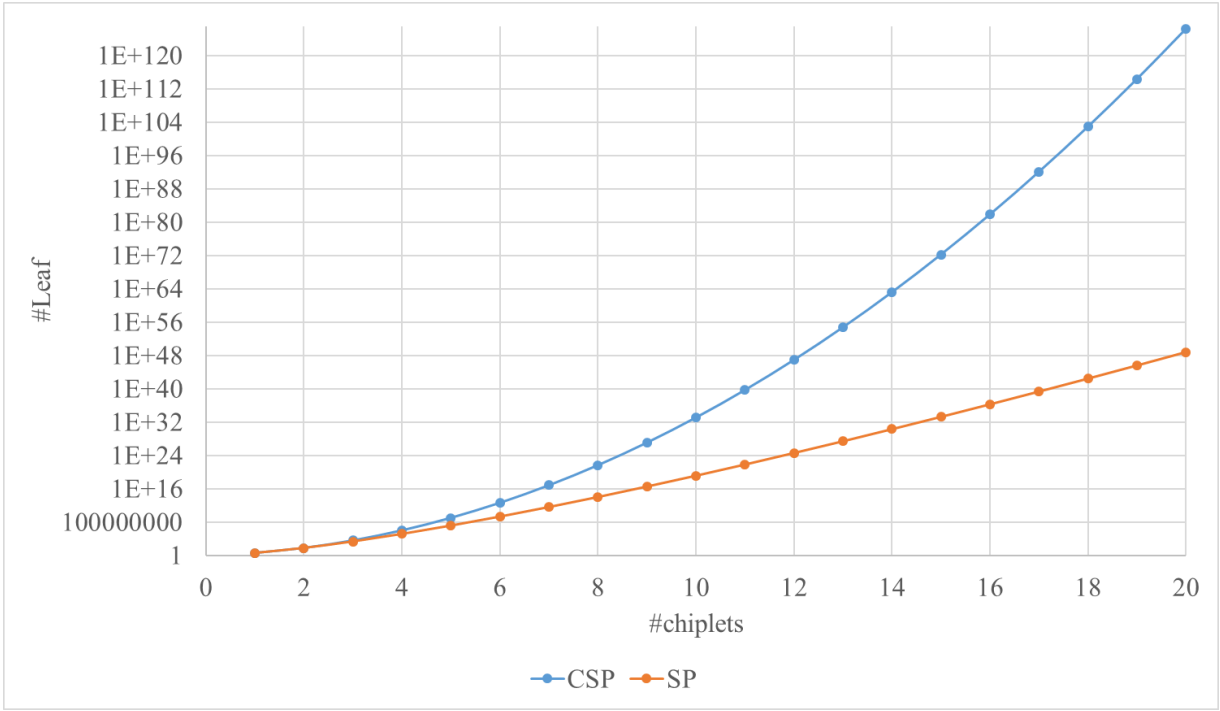
for each $i \in [1, n^2]$ **do**

$\gamma[i] = 1 - \frac{\alpha[i]}{n_k}$;

end for

Solution Space for n Chiplets

#chiplets	#leafs	
	CSP	SP
1	4	4
2	64	64
3	4096	2304
4	1048576	147456
5	1073741824	14745600
6	4.39805E+12	2123366400
7	7.20576E+16	4.1618E+11
8	4.72237E+21	1.06542E+14
9	1.23794E+27	3.45196E+16
10	1.29807E+33	1.38078E+19
11	5.44452E+39	6.683E+21
12	9.13439E+46	3.84941E+24
13	6.12998E+54	2.6022E+27
14	1.6455E+63	2.04012E+30
15	1.76685E+72	1.83611E+33
16	7.58855E+81	1.88018E+36
17	1.3037E+92	2.17349E+39
18	8.959E+102	2.81684E+42
19	2.4626E+114	4.06751E+45
20	2.7077E+126	6.50802E+48



Post Placement with Thermal Consideration (5/4)

1) Calculate *T*max and its position of a given placement by using CTS
2) Define and calculate the thermal gain of each chiplet i, $g_i = \frac{T_{max,1}}{P_i}$, i=1~n. P_i is the power of chiplet i and $T_{max} = \sum_{i=1}^{n} g_i P_i$
3) Partially differentiate $T_{max,d} = \sum_{i=1}^{n} g_i P_i/(d_i + \Delta d_i)$
4) Calculate the increasing HPWL per unit moving length of a chiplet i to be $\delta W_i = (|\cos\theta_i + \sin\theta_i|) * (\#net_i)$
5) Calculate the thermal−wirelength product$\delta T_i/\delta W_i$for each chiplet i and choose the chiplet m with the lowest value
6) Calculate $\Delta d_{m,max}$ to be $(T_{max} - T_{threshold}) \div \frac{g_i P_i}{d_i}$
7) Move chiplet *m* away from the point of T_{max} with a suitable distance $\Delta d_m \leq \Delta d_{m,max}$
8) Renew the position and value of T_{max}

Post Placement with Thermal Consideration (6/4)

9) Move all chiplets simultaneously along the direction of interposer center from the position of T_{max} , and the displacement is r% of the distance between the position of Tmax and the interposer center (the default value of r is 1).
10) Repeat the above steps iteratively until the temperature meets the thermal threshold, the chiplet cannot be moved,
11) If none of the placements with increasing TWL < η% is satisfied $T_{constrain}$, then choose the minimum cost from equation (4) of those placements

Wirelength-Driven Placement Comparison

Table 1: Results on wirelength driven placement with w_{space} = 0 mm

Case	Chiplets	Pins	Nets	Terminals	[8]		CP-SP-Tree			Comparison		
					TWL (m)	Time (s)	TWL (m)	w/ [8]'s PDC Time (s)	w/ Sec. 5.2.3 Time (s)	TWL Diff. (%)	w/ [8]'s PDC Speedup (×)	w/ Sec. 5.2.3 Speedup (×)
t4_s	4	15611	1808	789	10.87000	0.263	10.87000	0.127	0.123	0.000	2.071	2.138
t4_m	4	91005	5326	1174	38.14000	0.577	38.14000	0.226	0.214	0.000	2.553	2.696
t4_b	4	223781	12265	1033	58.92000	1.180	58.92000	0.411	0.396	0.000	2.871	2.980
t6_s	6	20138	1720	639	9.01000	0.366	9.01000	0.122	0.098	0.000	3.000	4.572
t6_m	6	121935	7123	1162	33.77000	1.791	33.77000	0.439	0.392	0.000	4.080	4.572
t6_b	6	229228	14264	1192	62.71000	2.470	62.71000	0.945	0.886	0.000	2.614	2.788
t8_s	8	18689	1918	882	23.51000	1.341	23.51000	0.192	0.165	0.000	6.984	8.127
t8_m	8	159149	8391	1391	36.39000	2.058	36.39000	0.711	0.683	0.000	2.895	3.013
t8_b	8	306057	12593	1049	66.61000	12.116	66.61000	1.094	0.933	0.000	11.075	12.986
apte_scaled20	9	287	97	73	0.37701	17.620	0.37704	9.782	8.501	0.008	1.801	2.073
apte_scaled15	9	287	97	73	0.37320	14.087	0.37265	9.559	8.457	-0.147	1.474	1.666
apte_scaled10	9	287	97	73	0.36630	12.192	0.36551	9.430	6.963	-0.216	1.293	1.751
apte_scaled5	9	287	97	73	0.37526	31.774	0.37526	6.299	5.270	0.000	5.044	6.029
xerox_scaled20	10	698	203	2	0.36399	22881.822	0.36398	220.391	146.051	-0.003	103.824	156.670
xerox_scaled15	10	698	203	2	0.37876	4634.995	0.37861	111.165	88.330	-0.040	41.695	52.474
xerox_scaled10	10	698	203	2	0.41998	3685.743	0.41830	101.963	65.245	-0.400	36.148	56.491
xerox_scaled5	10	698	203	2	0.43747	1853.318	0.43747	64.173	50.623	0.000	28.880	36.610
hp_scaled20	11	309	83	45	0.14002	17.315	0.13992	10.044	9.524	-0.071	1.724	1.818
hp_scaled15	11	309	83	45	0.14342	9.649	0.14194	2.851	2.580	-1.035	3.384	3.740
hp_scaled10	11	309	83	45	0.14377	5.140	0.14295	1.729	1.641	-0.570	2.974	3.132
hp_scaled5	11	309	83	45	0.16401	4718.180	0.16401	930.729	836.377	0.000	5.069	5.641
apte	9	287	97	73	0.43751	1397.697	0.43751	323.930	186.660	0.000	4.315	7.488
xerox	10	698	203	2	0.36587	>12hr	0.36430	34994.700	22187.000	-0.430	X	X
hp	11	309	83	45	0.15026	14281.288	0.15014	438.440	348.699	-0.080	32.573	40.956
Avg.										-0.124	13.406	18.242

Placement with Thermal Consideration

Table 2: Results on placement with thermal consideration and w_{space} = 0.1 mm

Case	CP-SP-Tree			CP-SP-Tree + Post CP					
	TWL (m)	Max. Temp. (℃)	Time (s)	TWL (m)	Max. Temp. (℃)	Time (s)	Increasing TWL (%)	Max. Temp. Reduction (℃)	Runtime Overhead (s)
apte_scaled30	0.40872	92.669	17.504	0.42707	84.455	75.605	4.490	8.214	58.101
apte_scaled25	0.40213	91.889	15.803	0.43193	84.979	87.846	7.411	6.910	72.043
apte_scaled20	0.39267	99.579	9.782	0.41887	94.562	83.610	6.672	5.017	73.828
apte_scaled15	0.41692	95.123	43.177	0.43818	91.556	88.489	5.099	3.567	45.312
xerox_scaled30	0.40664	88.631	149.792	0.42894	83.603	184.882	5.484	5.028	35.090
xerox_scaled25	0.42087	89.632	71.292	0.45233	84.673	187.037	7.475	4.959	115.745
xerox_scaled20	0.48135	87.810	192.405	0.50846	84.091	220.035	5.632	3.719	27.630
xerox_scaled15	0.51508	86.778	334.773	0.56097	84.918	344.944	8.909	1.860	10.171
hp_scaled30	0.16144	86.284	10.252	0.16362	84.773	23.564	1.350	1.511	13.312
hp_scaled25	0.19377	85.050	265.859	0.19617	84.584	320.769	1.239	0.466	54.910
Avg.							5.376	4.125	50.614

Thank You !