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# An On-line Aging Detection and Tolerance Framework for Improving Reliability of STT-MRAMs

EDA LAB

# Outline

- Introduction
- Preliminaries
- Proposed Framework
- Experimental Results
- Conclusions

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# Introduction

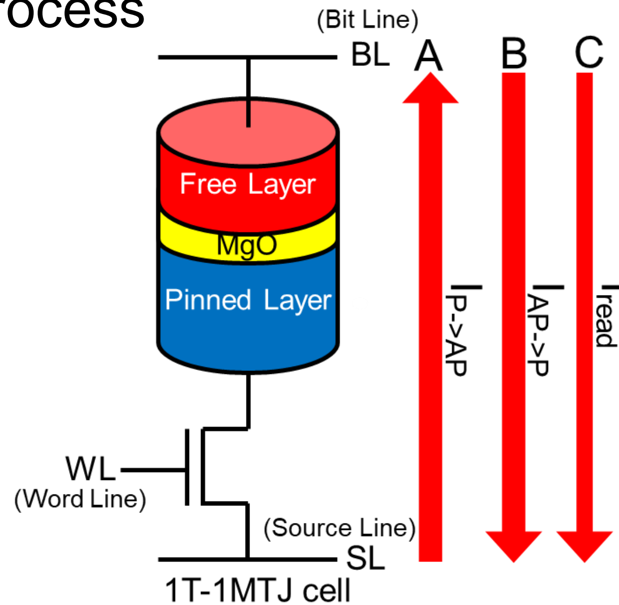
- With the rapid development of AIoT (Internet of Things), the market of smart device growing extremely fast in the past few years.

- However, downscaling CMOS memory technologies (SRAM and/or embedded DRAM) lead to increased leakage power.

- The investigation of next generation memory designs to replace CMOS memory technologies.
  - Phase change memory (PCM)
  - Spin-transfer-torque magnetic random-access memory (STT-MRAM)
  - Resistive random-access memory (ReRAM)

# Introduction

- Among them, STT-MRAM is a promising candidate for on-chip memory
  - High density
  - Relative Fast speed
  - Nonvolatile
  - Negligible leakage power
  - Compatibility with CMOS process



1T-1MTJ cell

| Arrow A | Write 1 |
|---|---|
| Arrow B | Write 0 |
| Arrow C | Read |

| Operations | Write '1'('0') | Read |
|---|---|---|
| WL | VDD | VDD |
| BL | GND(VDD) | $V_{read}$ |
| SL | VDD(GND) | GND |

Operation conditions of STT-MRAM

# Introduction

- There are various researchers have proposed different aging detection and tolerance techniques.
  - [4] proposed a design-for-testability (DFT) scheme to monitor the electrical parameter deviations over time.
  - [15] proposed a self-activated build-in self-test (BIST) and build-in self-repair (BISR) engine to detect and tolerate the aging failure of an MTJ.

[4] G. Radhakrishnan, Y. Yoon and M. Sachdev, "Monitoring Aging Defects in STT-MRAMs," in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 39, no. 12, pp. 4645-4656, Dec. 2020

[15] Y. Zhou, H. Cai, M. Zhang, L.A.B. Naviner, J. Yang, A novel BIST for monitoring aging/temperature by self-triggered scheme to improve the reliability of STT-MRAM, Microelectronics Reliability, Volume 114, 2020, 113735, ISSN 0026-2714.

# Contributions

- We propose a novel on-line aging detection and tolerance framework for improving reliability of STT-MRAMs.
- In our aging detection mechanism, we define four health levels of an MTJ and perform early aging detection to identify aged rows before they are breakdown.
- We compensate the aging-induced resistance drop of the aged words by a well-designed reference resistance generator to ensure the correctness of the reading results.
- Simulation results show that our framework can successfully detect 99% aging word under process variation and can achieve at most 25% reliability improvement of STT-MRAMs.

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  - STT-MRAM Basics
  - Aging Effect on MTJ
  - MTJ Defect Model
- Proposed Framework
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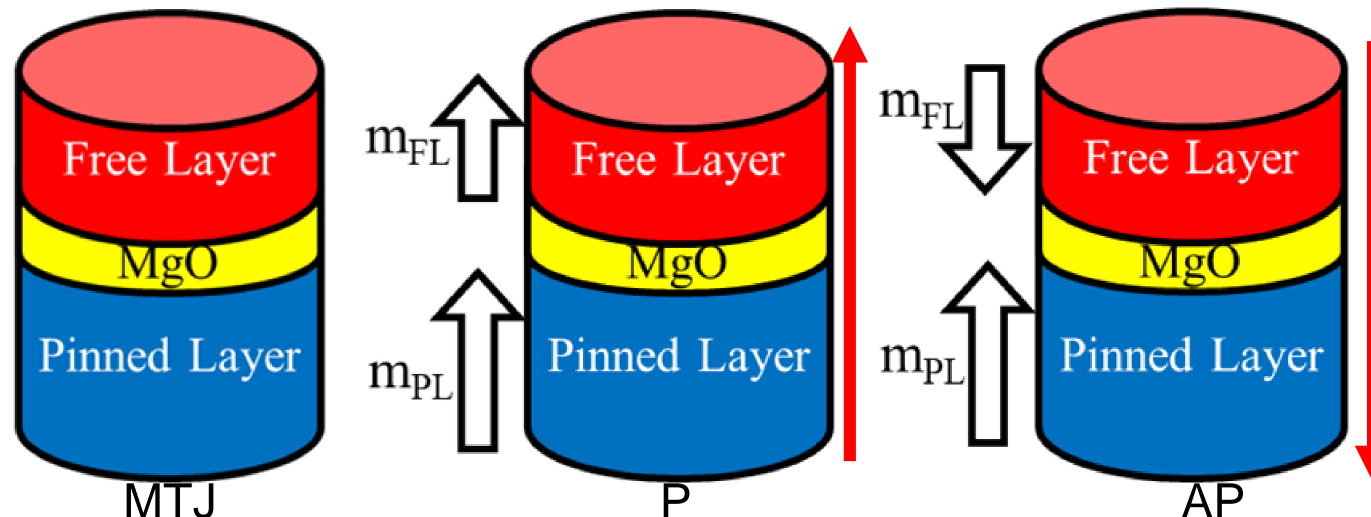
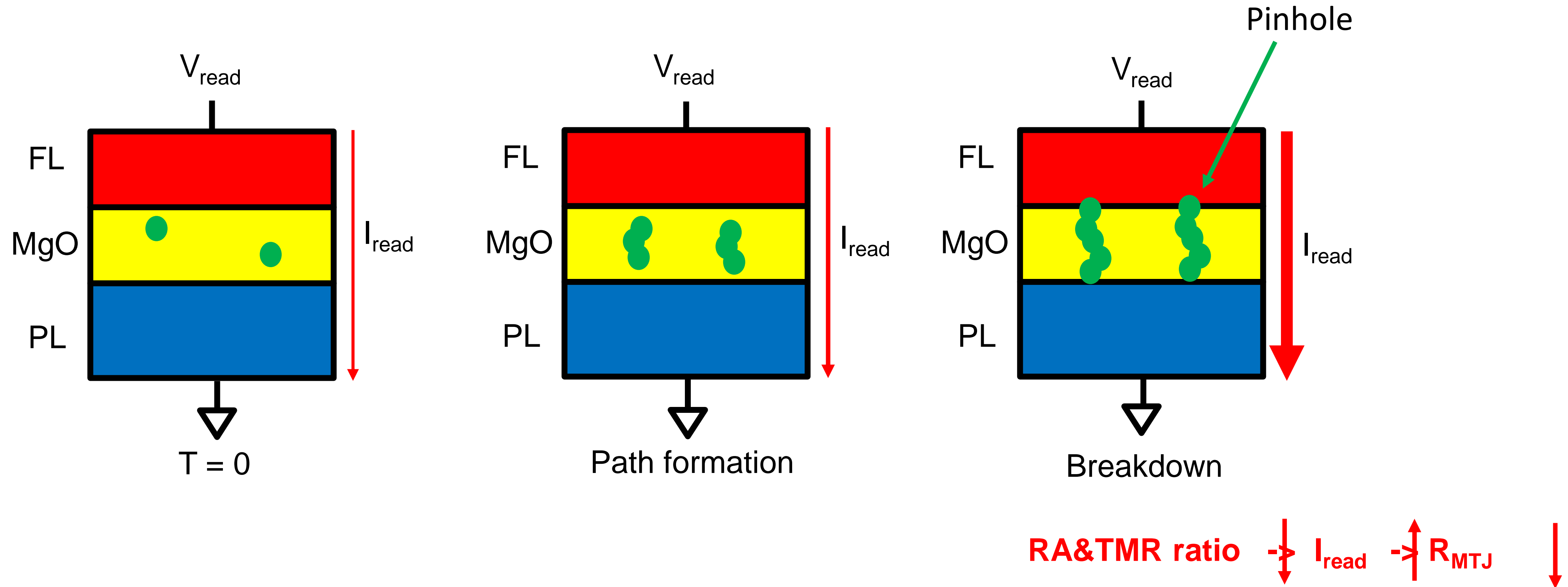
# STT-MRAM Basics

- Magnetic tunnel junction (MTJ) basics:
  - MTJ is the core of STT-MRAM
  - MTJ has two states due to TMR (Tunnel Magneto-Resistance) effect:
    - AP (Anti-Parallel) is high resistance and represents as logic 1
    - P (Parallel) is low resistance and represents as logic 0
  - TMR ratio is defined: $TMR = \frac{(R_{AP} - R_P)}{R_P}$
  - Resistance-area (RA) product show the resistance property of layer materials in MTJ devices



# Aging Effect of MTJ

- Time-dependent dielectric breakdown (TDDB) is considered as one of the most prominent aging mechanism in MTJ devices.



# MTJ Defect Model

- The pinhole defect degrades both TMR and RA of MTJ.
  - Cause resistance degradation.
- The defective TMR and RA of defective MTJ can be calculated by the equations below [11].

$$RA_{\mathrm{eff}}(A_{\mathrm{ph}}) = \frac{A_0}{\frac{A_0(1 - A_{\mathrm{ph}})}{RA_{\mathrm{df}}} + \frac{A_0 \cdot A_{\mathrm{ph}}}{RA_{\mathrm{bd}}}}$$

$$TMR_{\mathrm{eff}}(A_{\mathrm{ph}}) = TMR_{\mathrm{df}} \cdot \frac{RA_{\mathrm{eff}}(A_{\mathrm{ph}}) - RA_{\mathrm{bd}}}{RA_{\mathrm{df}} - RA_{\mathrm{bd}}}$$

[11] L. Wu et al., "Pinhole Defect Characterization and Fault Modeling for STT-MRAM Testing," 2019 IEEE European Test Symposium (ETS), 2019, pp. 1-6.

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  - Aging Detection Mechanism
  - Aging Tolerance Mechanism
  - Look-up Table Design
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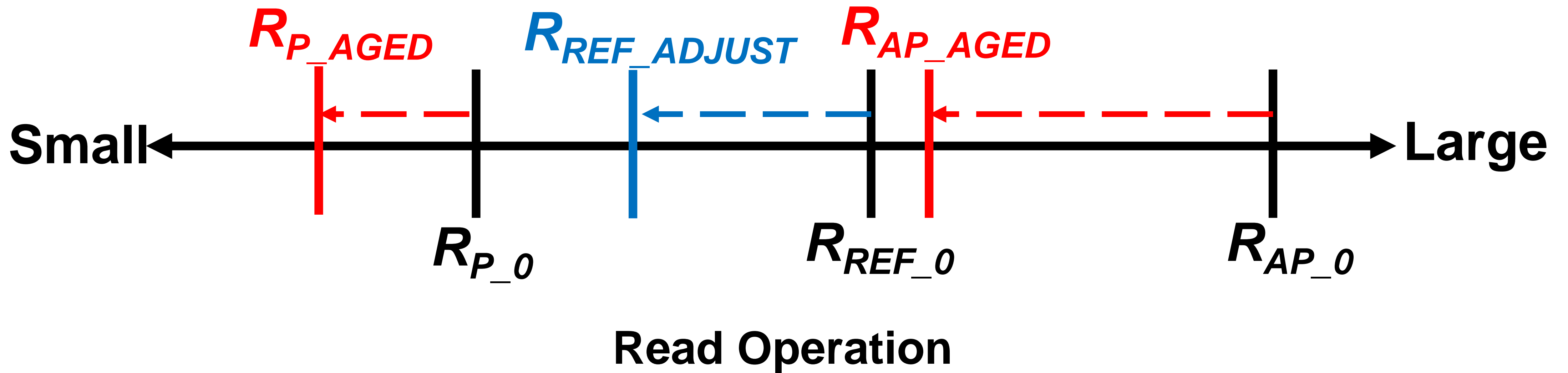
# Problem Formulation

- In this paper, we majorly focus on the TDDB-induced pinhole defects on MTJ, and assume peripherical circuits are ideal to reduce the problem complexity.

- Here we formally formulate the problem we address in this paper as follows:
  - Given a STT-MRAMs and the number of bits in a word.
  - We want to develop an on-line aging detection circuit and an on-line aging tolerance circuit can identify TDDB-induced aging word and read the aged word correctly.
  - Our development should not cause significant performance loss and large area overhead.

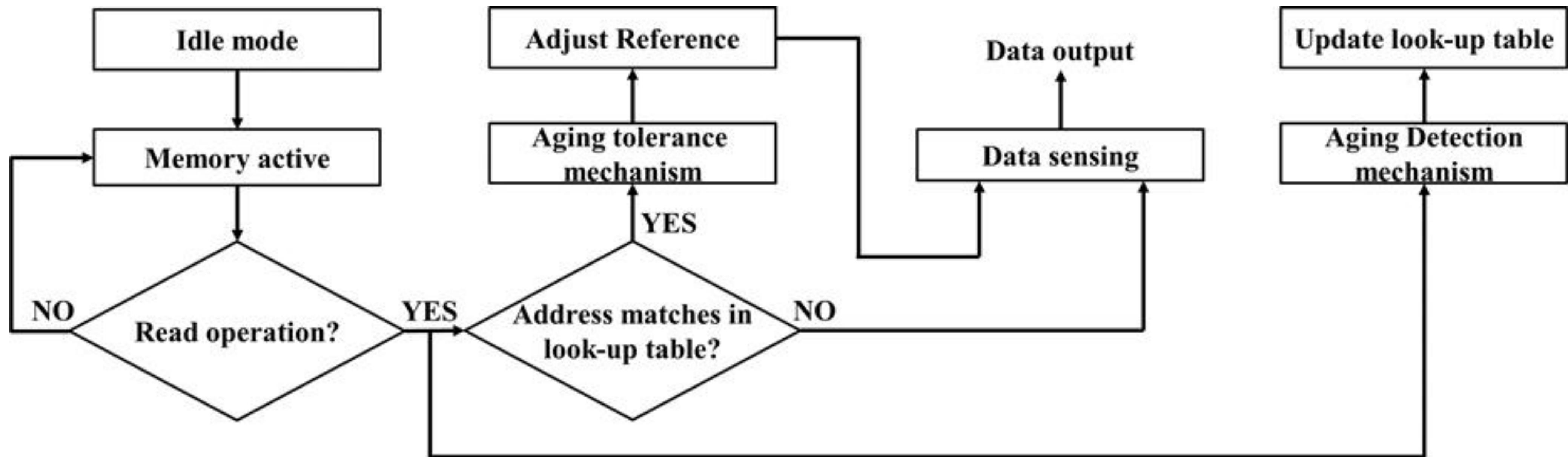
# Proposed Framework

- The main concept of our framework.



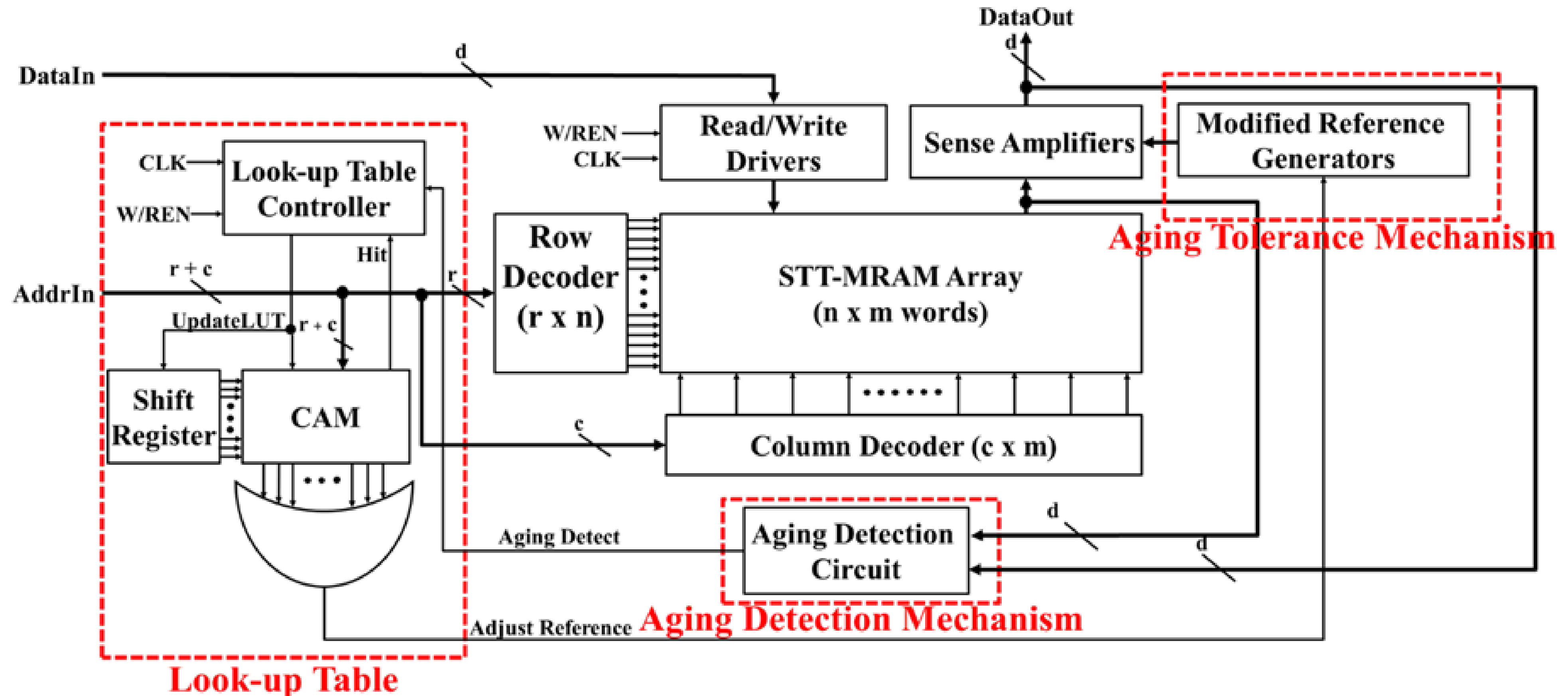
# Proposed Framework

- The flow chart of our framework.



# Proposed Framework

- The architecture diagram of our framework.



# Aging Detection Mechanism

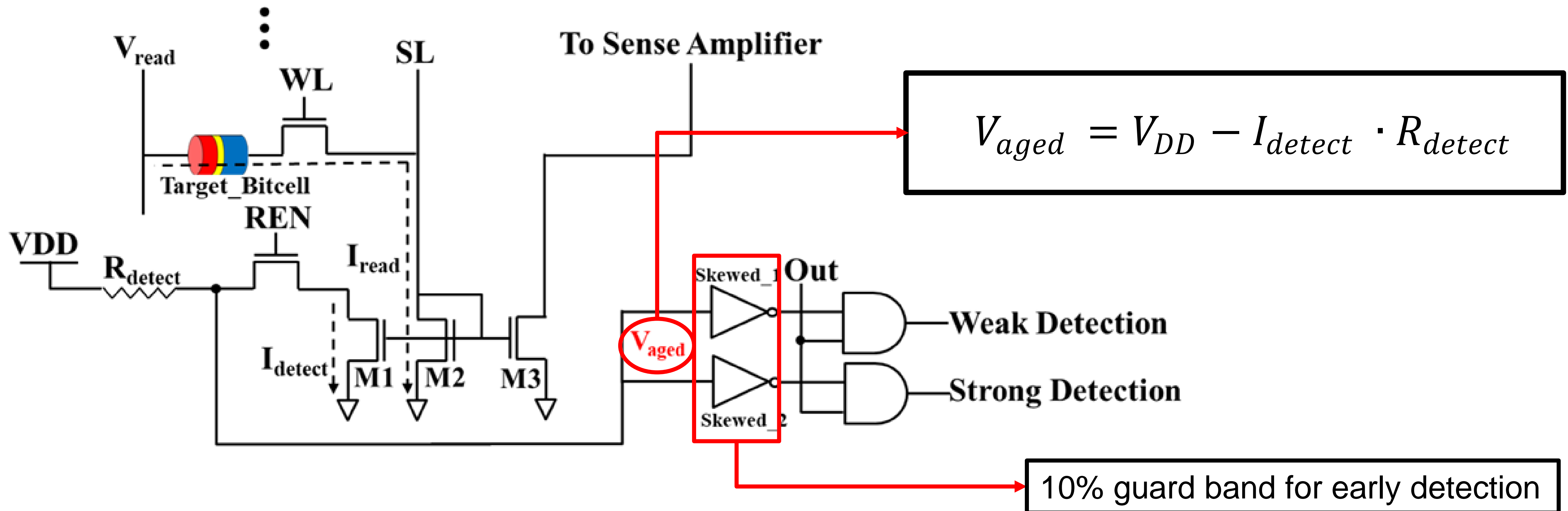
- The degradation of $R_{AP_AGED}$ is more serious than $R_{P_AGED}$.

Table I Definition of health level of MTJ and reference adjustment range.

| Health level of MTJ | Relations of $R_{AP_AGED}$ and $R_{REF_0}$ | Rf. Adjustment |
|---|---|---|
| Nominal | $R_{REF_0} < R_{AP_AGED}$ | No Adjust |
| Weak aging | $\frac{2}{3} \cdot R_{REF_0} < R_{AP_AGED} < R_{REF_0}$ | $\frac{2}{3} \cdot R_{REF_0}$ |
| Strong aging | $\frac{1}{2} \cdot R_{REF_0} < R_{AP_AGED} < \frac{2}{3} \cdot R_{REF_0}$ | $\frac{1}{2} \cdot R_{REF_0}$ |
| Breakdown | $R_{AP_AGED} < \frac{1}{2} \cdot R_{REF_0}$ | X |

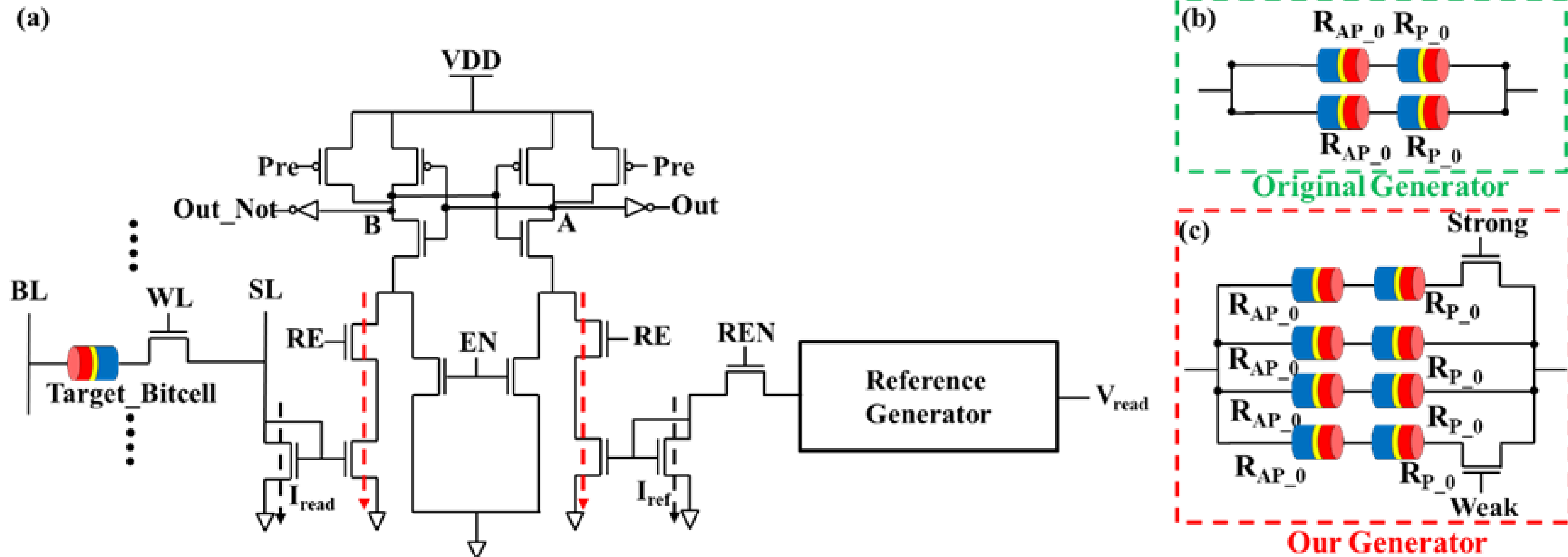
# Aging Detection Mechanism

- The schematic circuit diagram of aging detection circuit.



# Aging Tolerance Mechanism

- The schematic circuit diagram of current mirror-based sense amplifier [14] and the modified reference generator.




[12] S. Jain, A. Ranjan, K. Roy and A. Raghunathan, "Computing in Memory With Spin-Transfer Torque Magnetic RAM," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 26, no. 3, pp. 470-483, March 2018.

# Look-up Table Design

- Our LUT consists of three fields: Valid bit, Address, and W/S.
  - Valid bit indicates whether the corresponding row in the LUT stores information of an aged word.
  - Address represents the row and column information for the aged word.
  - W/S bit is used to indicate the health level of aged word.
    - Weak: W/S = 0.
    - Strong: W/S = 1.

Table III An example of LUT that only contains 1 weak-aged word.

| Row | Valid | Address | W/S |
|---|---|---|---|
| 0 | 1 | Addr1 | 0 |
| 1 | 0 | Don’t care (X) | 0 |
| 2 | 0 | Don’t care (X) | 0 |
| … | … | … | … |

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  - Aging Tolerance Mechanism Validation
  - Overhead Analysis
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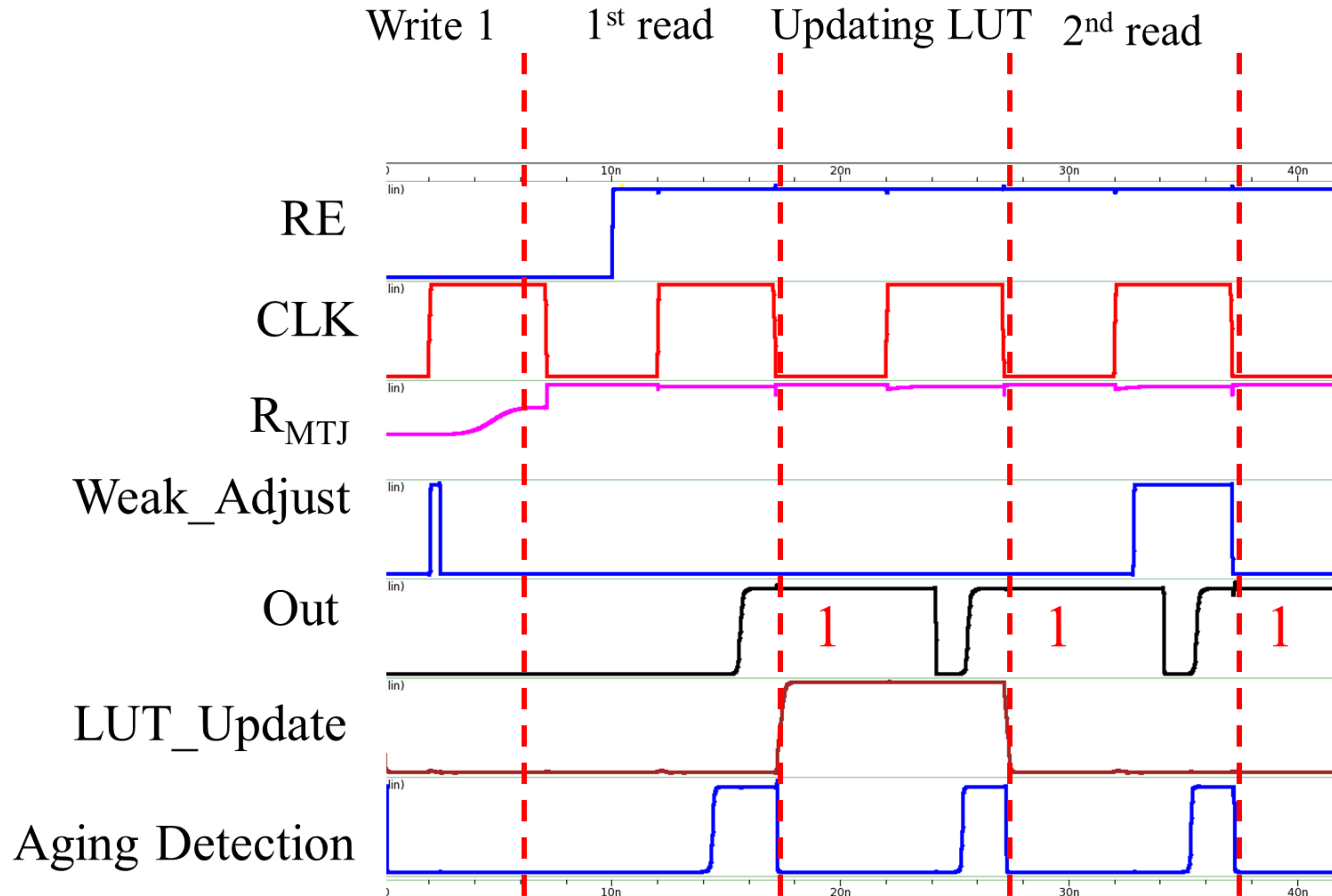
# Experimental Results

- We implement a 32K-bit STT-MRAMs in 90nm CMOS technology.
  - Row and column decoders, write drivers, and sense amplifiers, following by integrating the STT-MRAM structure with our aging detection circuit, aging tolerance circuit, and LUTs in SPICE.
  - Operating voltage is 1V.
- We perform HSPICE simulations with write and read operations under different aging status to valid the proposed aging detection and tolerance mechanisms.
- All experiments are performed on a 20-core, 2.5GHZ, Intel Xeon Gold 6248 CPU, with 160GB memory, and CentOS release 6.10 machine.

# Experimental Results

- The waveform of read operation with our proposed framework.



# Aging Detection Mechanism Validation

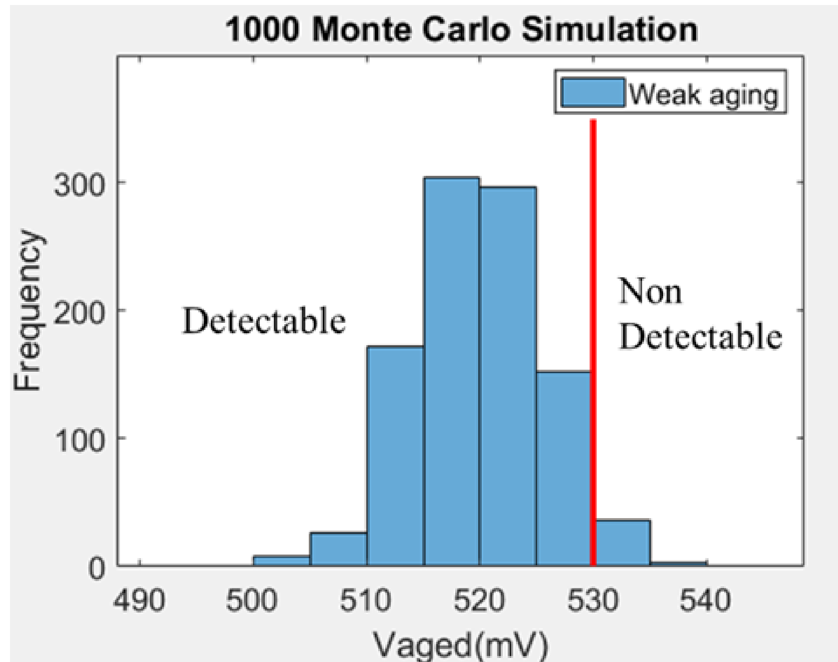
- Aging detection result.

Table IV Aging detection result for different aging situations.

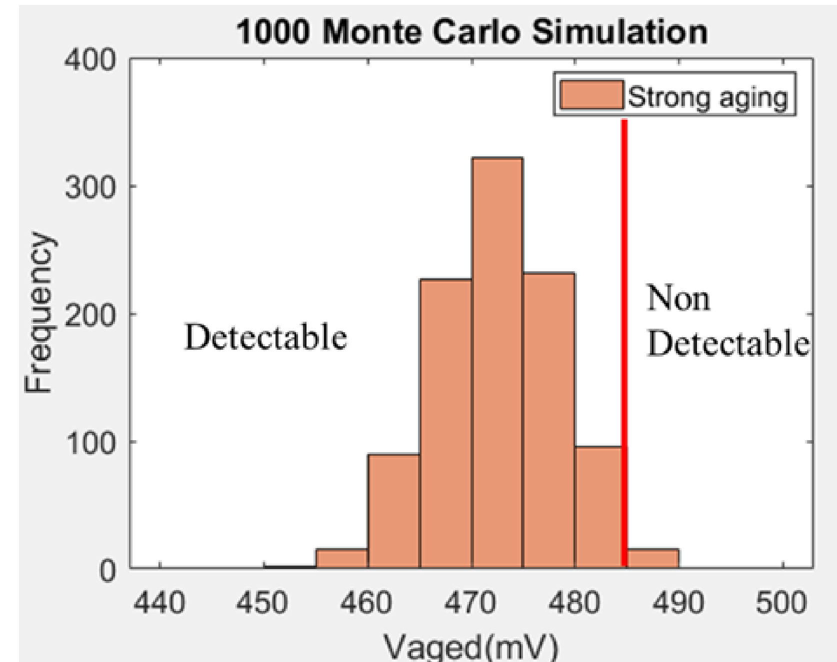
| Health level | $R_{AP}$ (kΩ) | $R_P$ (kΩ) | $V_{aged}$ (mV) | W | S |
|---|---|---|---|---|---|
| Nominal | >= 4.1 | >= 1.94 | >= 520 | 0 | 0 |
| Weak aging | 3.91~3.01 | 1.89~1.58 | 514~475 | 1 | 0 |
| Strong aging | 2.87~2.05 | 1.53~1.22 | 468~422 | 1 | 1 |

# Aging Detection Mechanism Validation

- To observe the effectiveness in the consideration of variations, we perform 1000 Monte-Carlo simulations with 5% variation.



Weak aging



Strong aging

# Aging Tolerance Mechanism Validation

- The reliability of STT-MRAM array at different time can be expressed as follows:

$$R(t) = e^{-\left[(SIZE - SIZE_e)\lambda\left(R_{REF_{initial}}, t\right) + SIZE_e \lambda\left(R_{REF_{adjust}}, t\right)\right]}$$

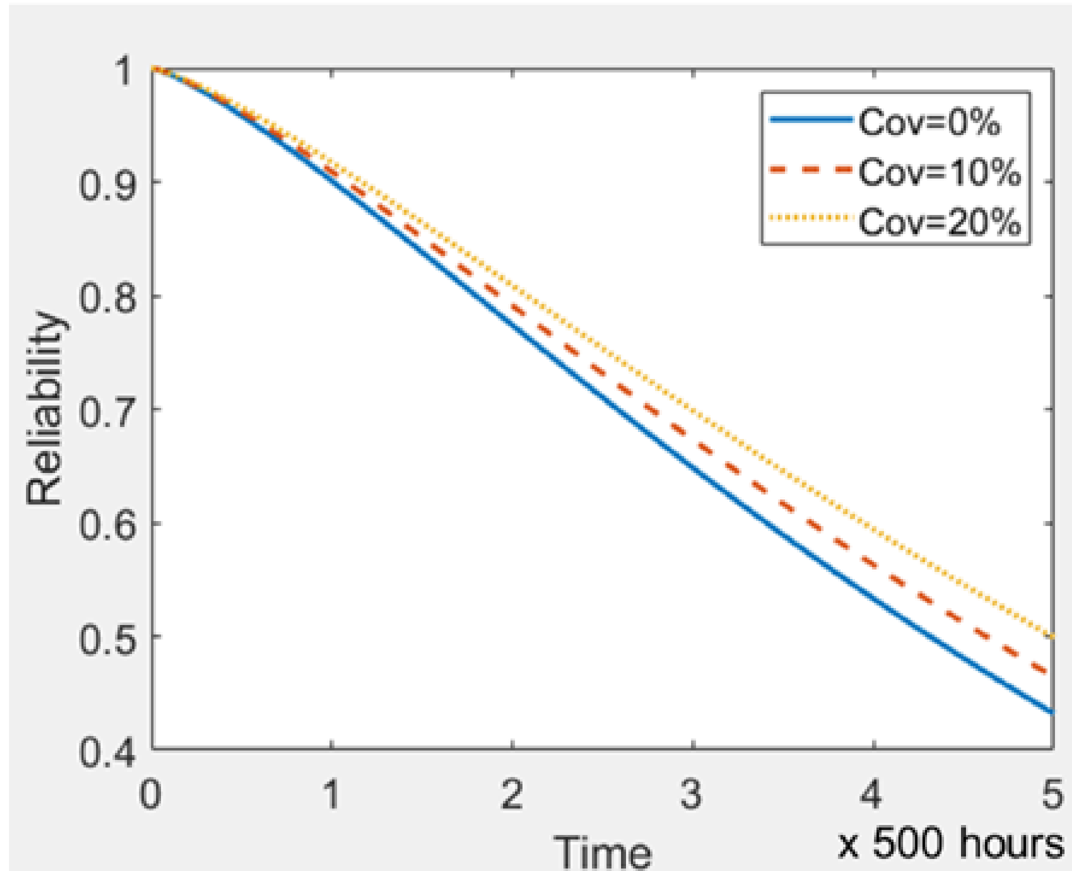
  - $\lambda(R_{REF}, t)$ is the failure rate at different time and it can be shown as follows:

$$\lambda(R_{REF}, t) = \frac{\beta}{T1} e^{\left(R_{REF} - R_{MTJ}(t)\right)}$$

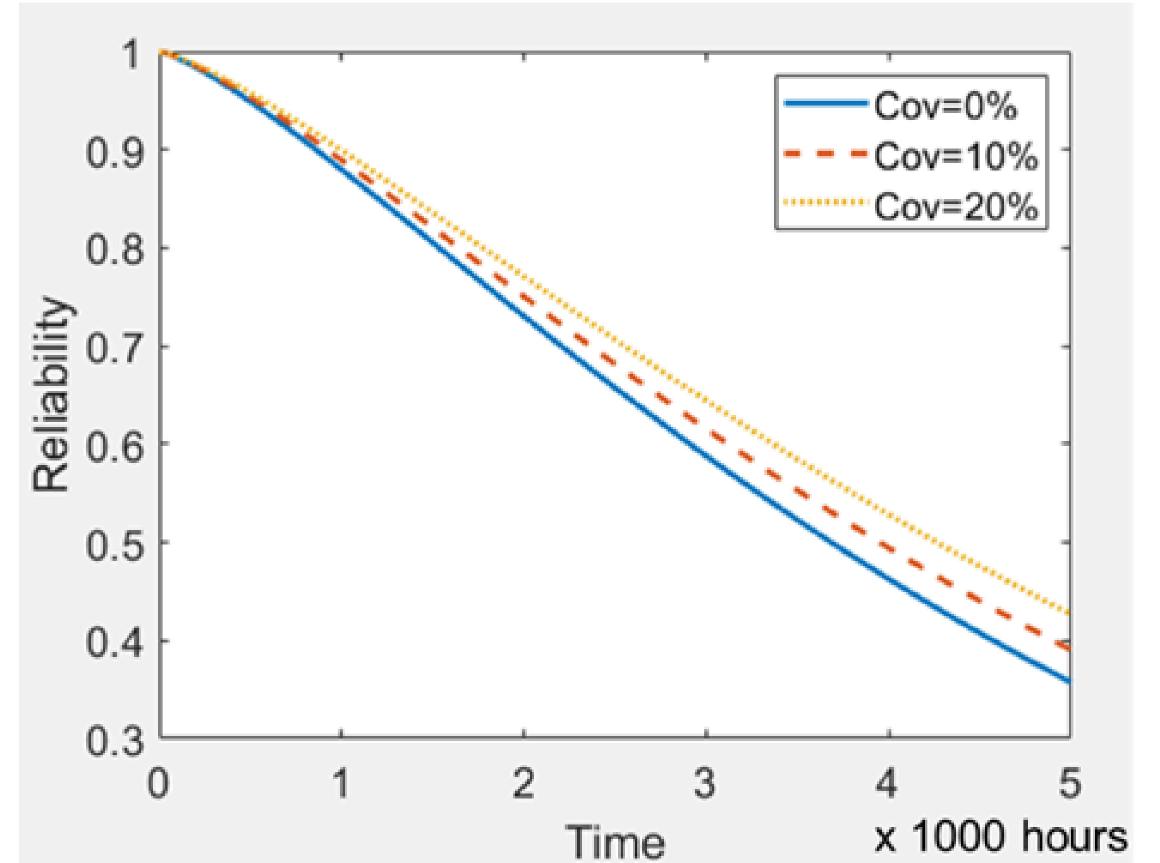
- To show the feasibility of our framework, we analyzed 500, 1000, 1500, and 2000 hours as $T1$ time to observe the effectiveness of the aging tolerance mechanism for reliability enhancement.

# Aging Tolerance Mechanism Validation

- T1 = 500 hours

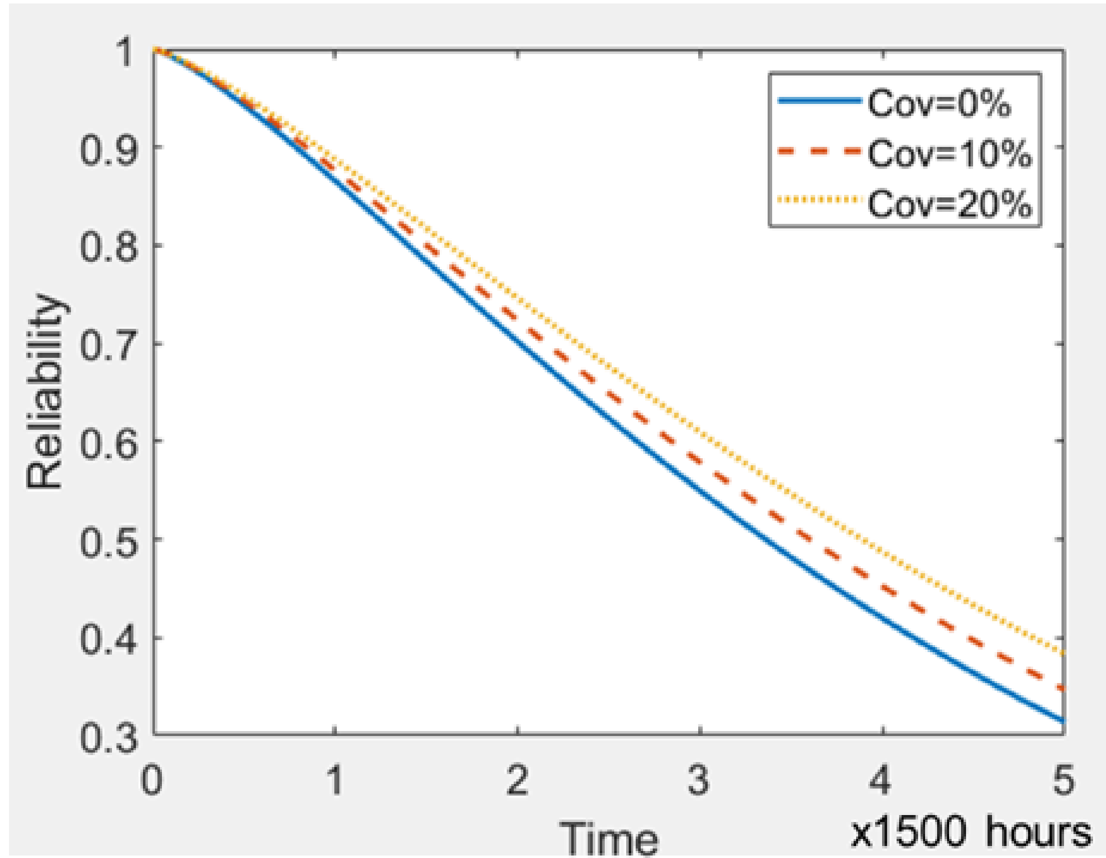



- T1 = 1000 hours

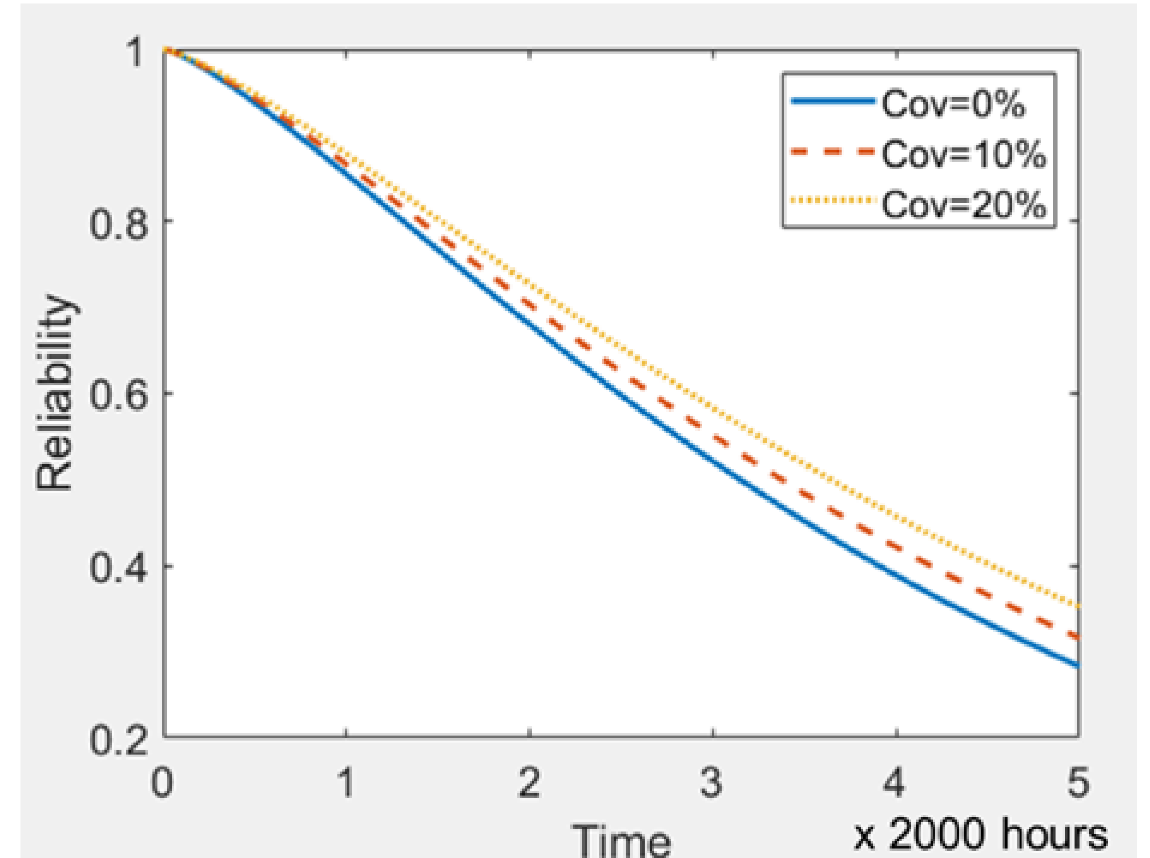


# Aging Tolerance Mechanism Validation

- T1 = 1500 hours




- T1 = 2000 hours



# Overhead Analysis

- Overhead.

Table V The area ($um^2$) of our framework which consists of memory array, aging detection and tolerance mechanism and LUT.

| Bit-width | *Cov* = 0% | *Cov* = 10% | *Cov* = 20% |
|---|---|---|---|
| 16 bits | 16981.8 | 18217.0 (+7.2%) | 19445.8 (+14.5%) |
| 32 bits | 17128.4 | 17714.6 (+3.4%) | 18288.1 (+6.7%) |
| 64 bits | 17336.0 | 17626.8 (+1.6%) | 17892.0 (+3.2%) |

Table VI The power (mW) of our framework which consists of memory array, aging detection and tolerance mechanism and LUT.

| Bit-width | *Cov* = 0% | *Cov* = 10% | *Cov* = 20% |
|---|---|---|---|
| 16 bits | 355 | 382 (x1.07) | 399 (x1.12) |
| 32 bits | 710 | 734 (x1.034) | 740 (x1.04) |
| 64 bits | 1434 | 1456 (x1.015) | 1457 (x1.016) |

# Conclusions

- We propose a novel on-line aging detection and tolerance framework for improving reliability of STT-MRAMs.
- Our aging detection mechanism is based on monitoring the variation of read current of the MTJ, and our aging tolerance mechanism is based on reference resistance adjustment.
- Simulation and analysis results show that the proposed techniques can successfully detect 99% aging words under process variation and achieve at most 25% reliability improvement of STT-MRAMs with $COV = 20\%$.

# Thank you

# Q&A