

# EFFICIENT HIERARCHICAL MM-WAVE SYSTEM SYNTHESIS WITH EMBEDDED ACCURATE TRANSFORMER AND BALUN ML MODELS

FÁBIO PASSOS

N. LOURENÇO, R. MARTINS, L. MENDES, J. VAZ, N. HORTA



instituto de  
telecomunicações



DEEC  
DEPARTAMENTO DE ENGENHARIA  
ELETROTÉCNICA E DE COMPUTADORES  
TÉCNICO LISBOA



# Overview



MOTIVATION



SYSTEM DESIGN  
METHODOLOGIES



MODELING PASSIVE COMPONENTS



EXPERIMENTAL RESULTS



CONCLUSIONS

**01**

# **MOTIVATION**

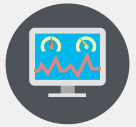
# MOTIVATION



Entering in 5G/6G era, mm-Wave circuits and systems are key technology enablers



We need circuits with high performances, low cost (small area), power efficient, etc



Such performances are difficult to obtain using manual/traditional design methodologies

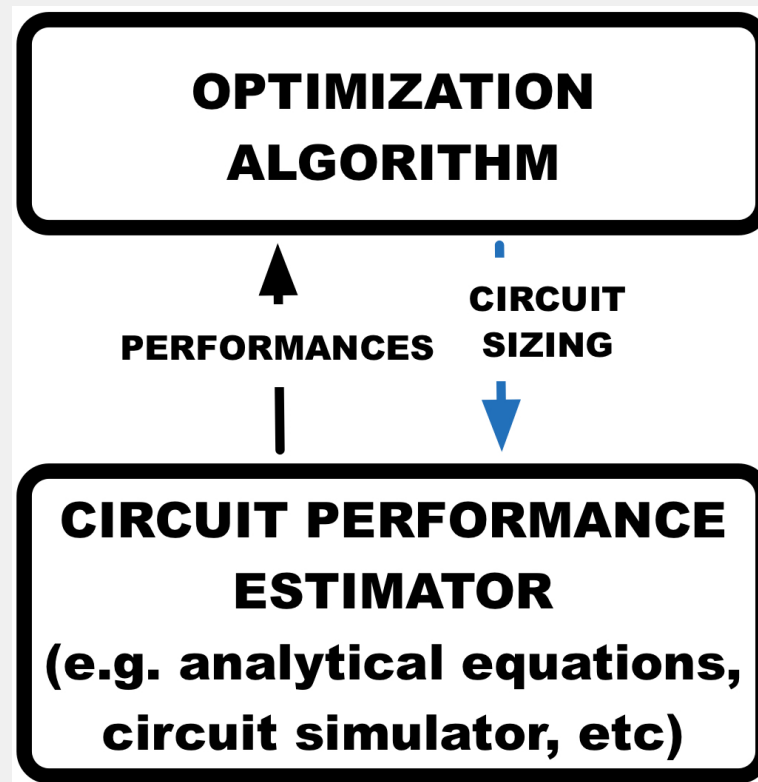


Therefore, there is a need for a more efficient methodology that can be used by designers



# OUR APPROACH...

Usage of optimization algorithms to automatically design circuits...



02

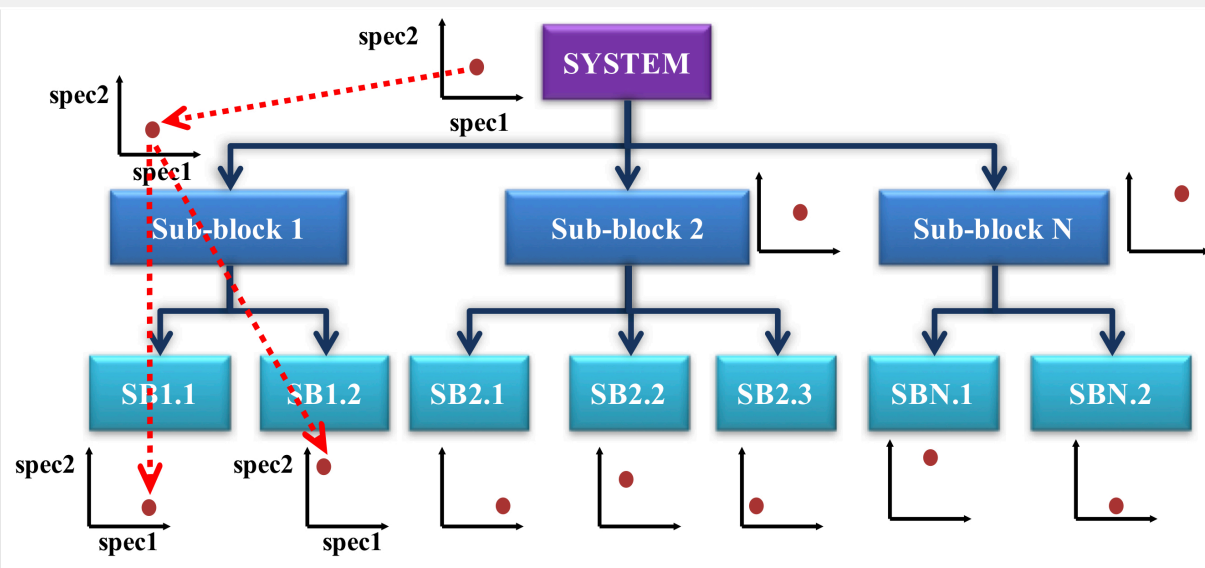
# SYSTEM DESIGN METHODOLOGIES

(...focusing on optimization-based design methodologies)

# TOP-DOWN METHODOLOGIES

- ◉ Divide and conquer strategies, system hierarchical decomposition

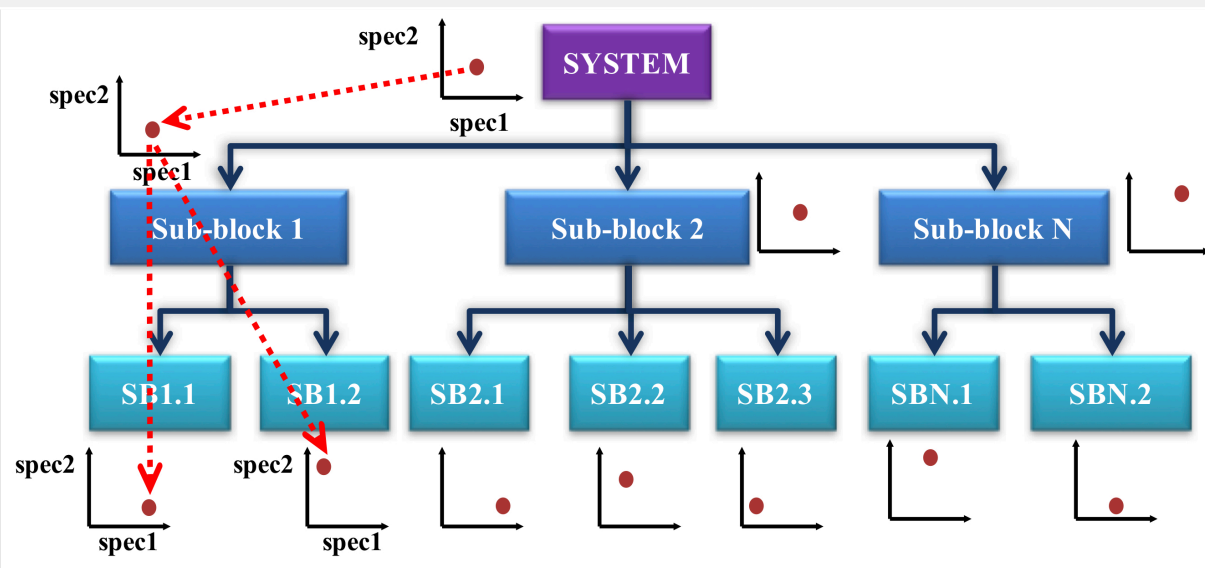
- ◉ Designer starts from the system level specifications



# TOP-DOWN METHODOLOGIES

- ◉ Divide and conquer strategies, system hierarchical decomposition

- ◉ Designer starts from the system level specifications
- ◉ Specifications transmitted down the hierarchy



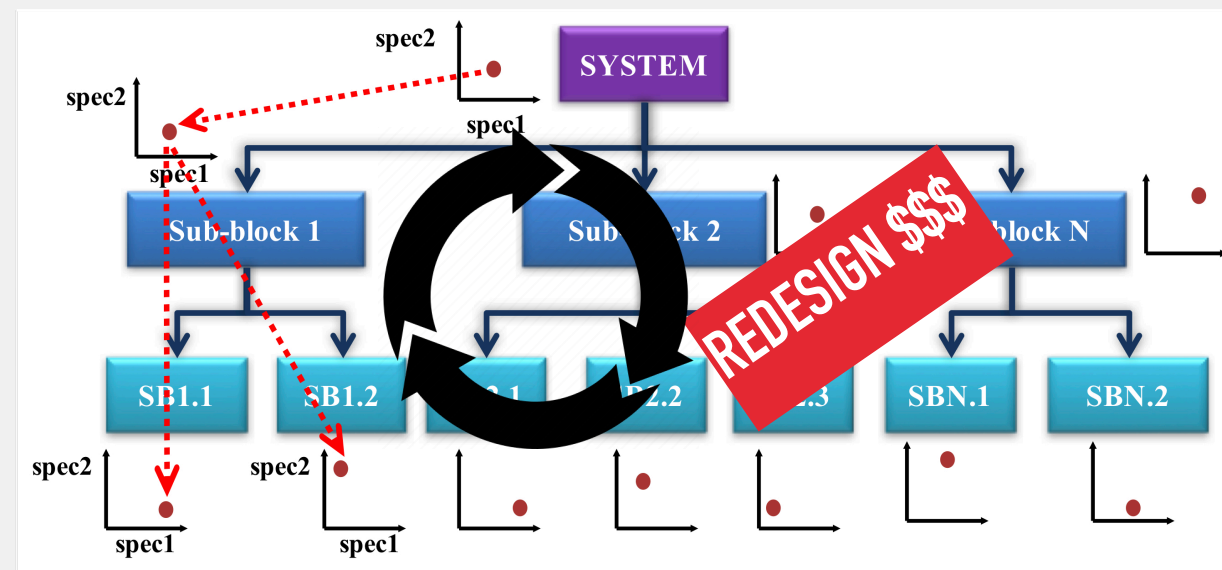
# TOP-DOWN METHODOLOGIES

- ◉ Divide and conquer strategies, system hierarchical decomposition

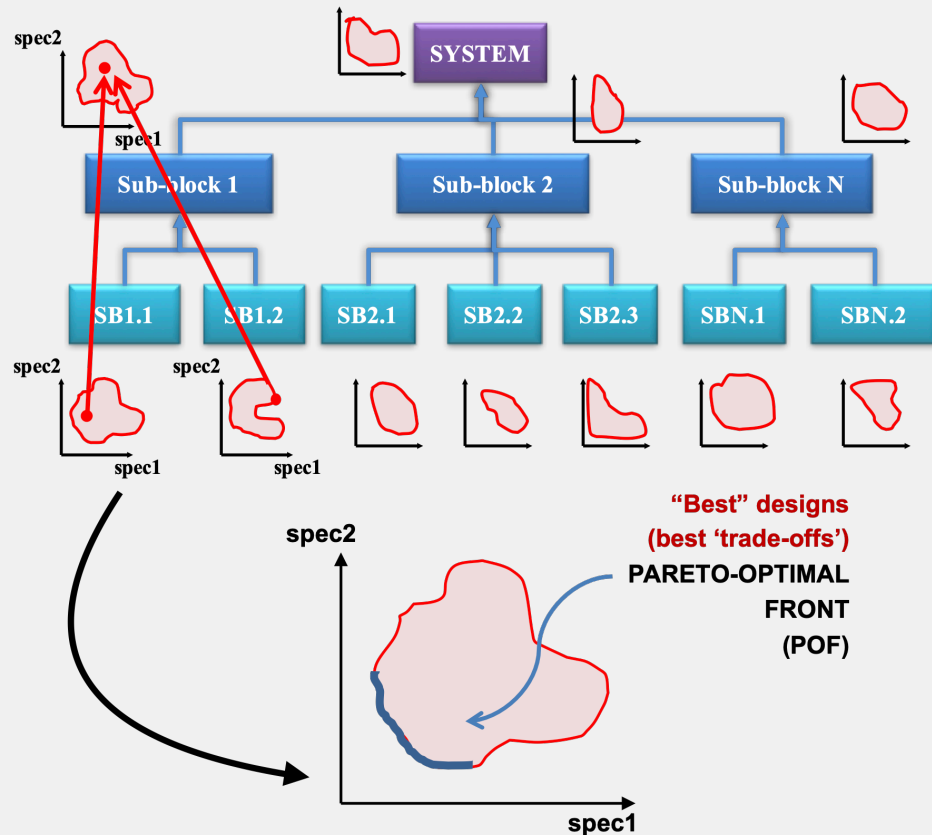
- ◉ Designer starts from the system level specifications

- ◉ Specifications transmitted down the hierarchy

- ◉ The fact that specifications are transmitted down without knowing if they will be realizable by lower level sub-blocks may lead to costly redesign iterations...!



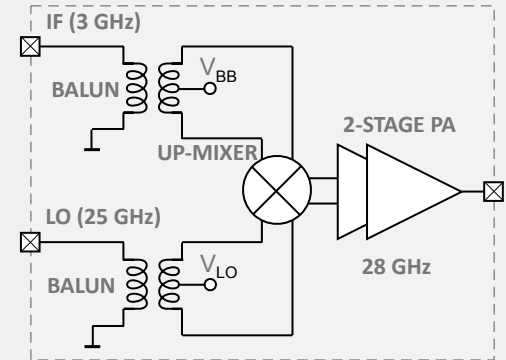
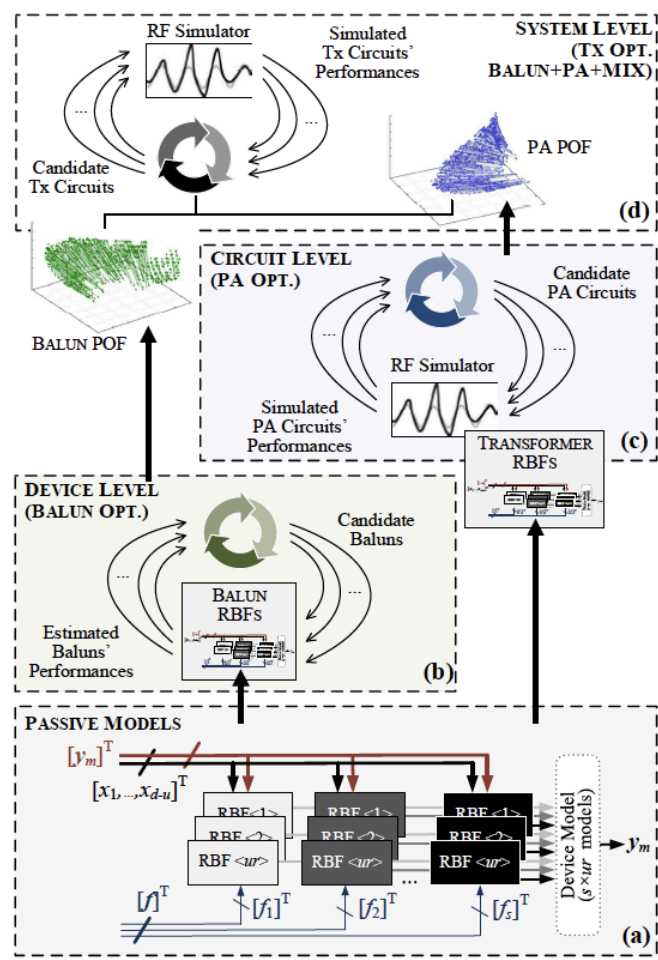
# BOTTOM-UP METHODOLOGIES



- Designer starts from the bottom level
- Ensures all levels are feasible (with the desired specifications)
- Multi-objective algorithms are used to pass POFs to the upper level

# EXPERIMENTAL CASE

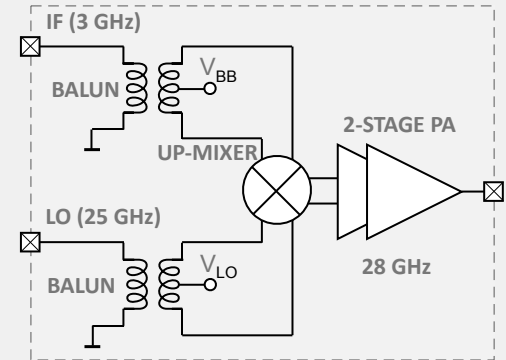
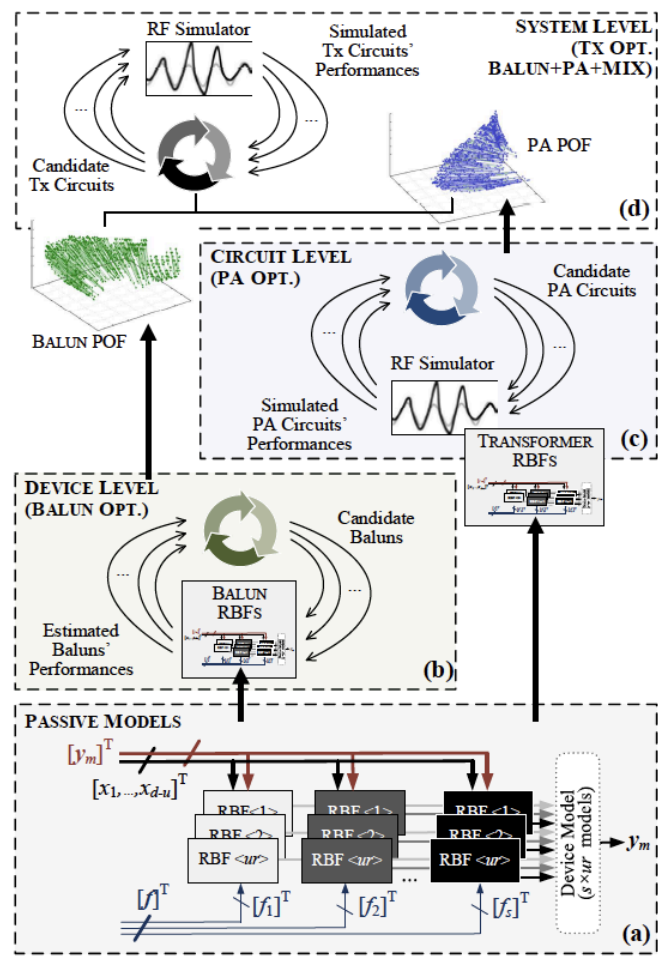
- 28GHz mm-Wave transmitter in 65nm CMOS technology



- passive component level: baluns

# EXPERIMENTAL CASE

- 28GHz mm-Wave transmitter in 65nm CMOS technology



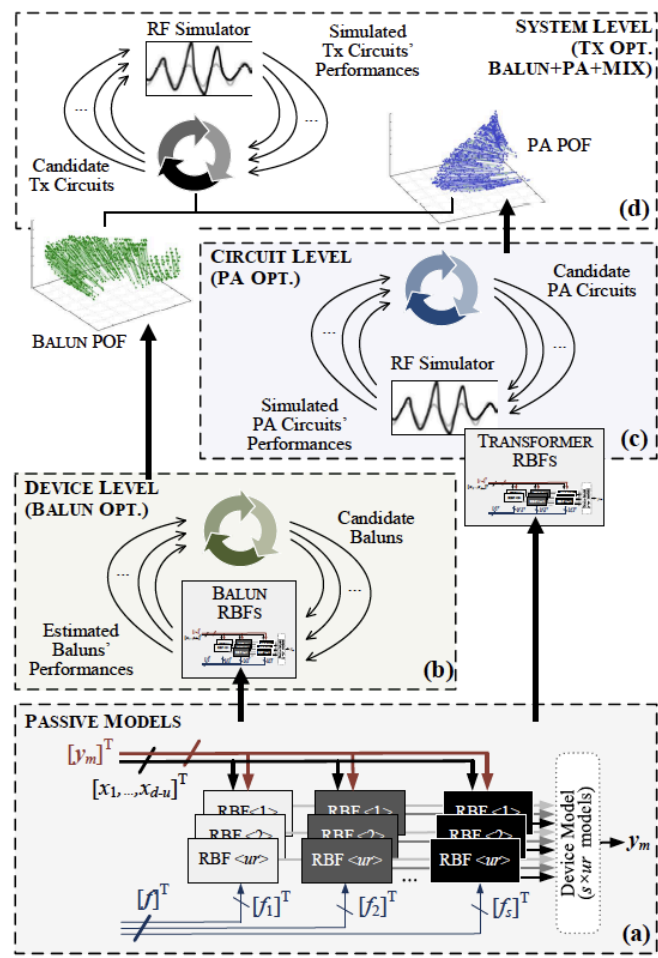
— — — — — ► ● circuit level: power amplifier (PA)

— — — — — ► ● passive component level: baluns



# EXPERIMENTAL CASE

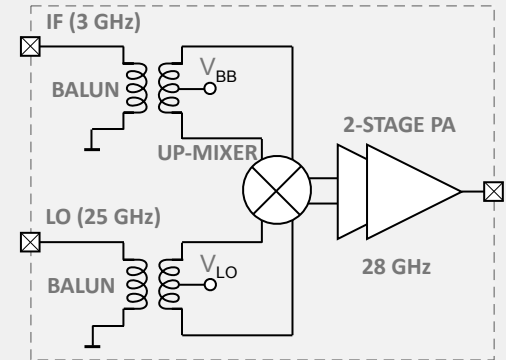
- 28GHz mm-Wave transmitter in 65nm CMOS technology



---> system level optimization: complete transmitter (with mixer)

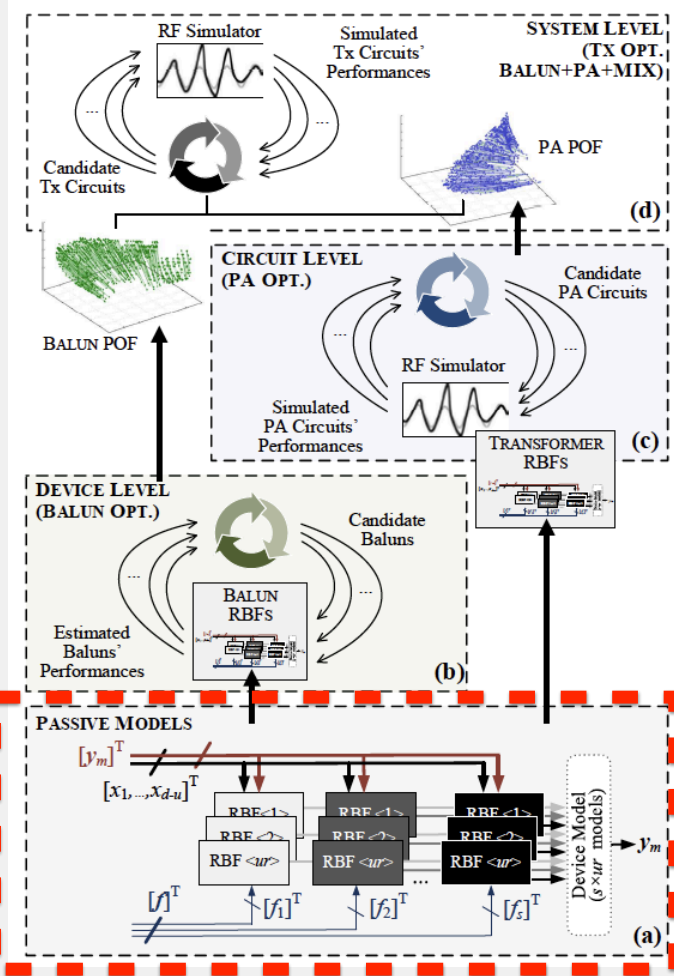
---> circuit level: power amplifier (PA)

---> passive component level: baluns



# EXPERIMENTAL CASE

- 28GHz mm-Wave transmitter in 65nm CMOS technology

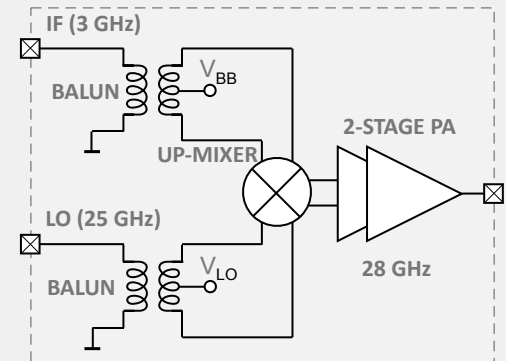


— — — — — ► ● system level optimization: complete transmitter (with mixer)

— — — — — ► ● circuit level: power amplifier (PA)

— — — — — ► ● passive component level: baluns



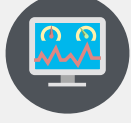


— — — — — ► ● Custom passive component models for transformers and baluns



03

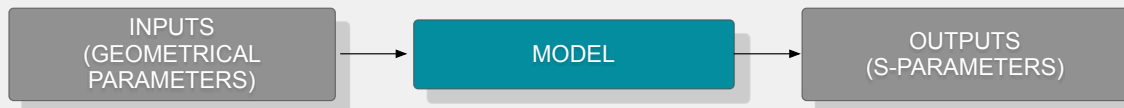
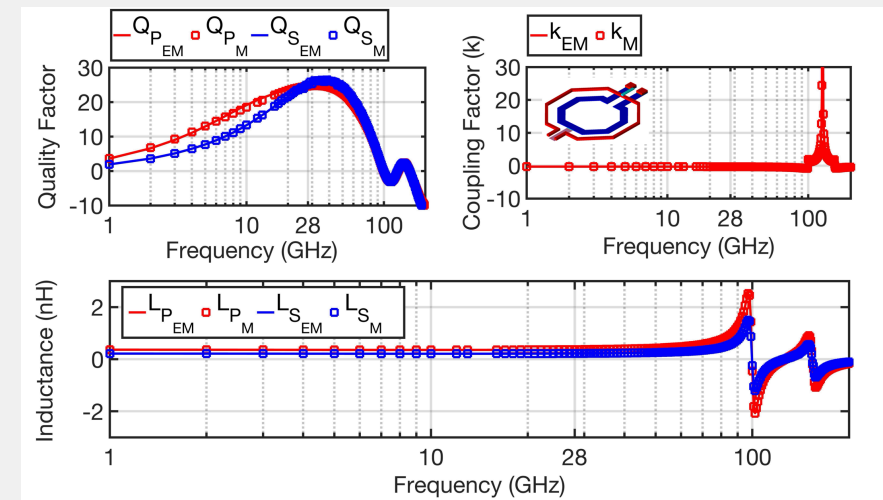
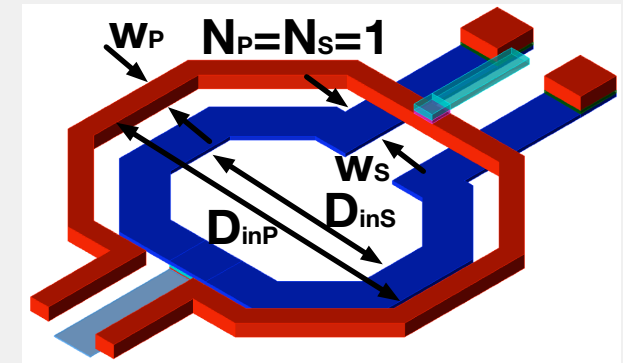
# MODELING PASSIVE COMPONENTS

# WHY?

-  Transformers/baluns are highly used in RF/mm-Wave circuits
-  Foundry's usually do not provide models for transformers (when they do, they are not valid over 20/30GHz)
-  EM simulations are time-consuming and integrating an EM simulator in optimization-based methodologies is time-prohibitive
-  Therefore, there is a need for an efficient and accurate model
-  Machine learning techniques have been applied successfully to the modeling of passive structures and they are proven themselves a valuable candidate solution

# MODELING PARAMETERS

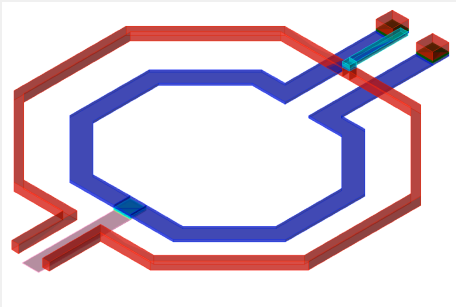
- Transformer design parameters and performances
- Design parameters
  - Number of turns of the primary ( $N_p$ ) and secondary ( $N_s$ ) coils, their inner diameters ( $D_{inP}$  and  $D_{inS}$ ), and their turn widths ( $W_p$  and  $W_s$ ).
- Performances parameters
  - S-Parameters
  - Inductance ( $L$ ) and quality factor ( $Q$ ) of the primary and secondary
  - coupling factor ( $k$ )
  - SRF



# MODEL VALIDATION (EM SIM)

- Radial Basis Functions based-model with an intelligent modeling strategy
- Two types of models were built: one for transformers and another for baluns (stacked transformers)

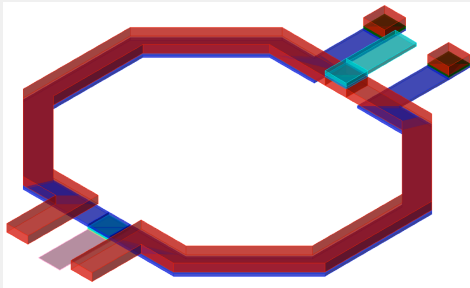
## TRANSFORMERS



- 1500 transformers for training and 100 for test
- 200 baluns for training and 50 for test

Model	Mean Square Error (%)				
	Lp	Qp	Ls	Qs	k
Transformer	0.14	1.54	0.11	1.93	0.17
Balun	0.15	2.09	0.12	1.57	0.26

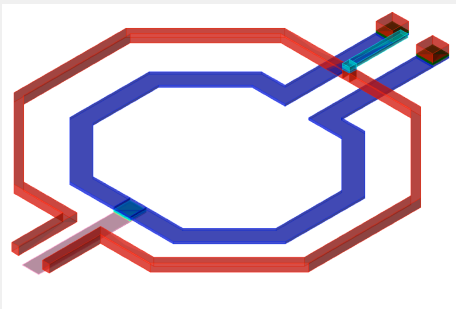
## BALUNS



# MODEL VALIDATION (MEAS.)

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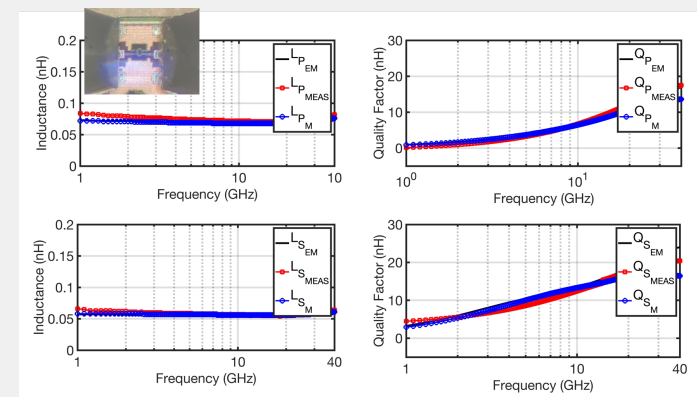
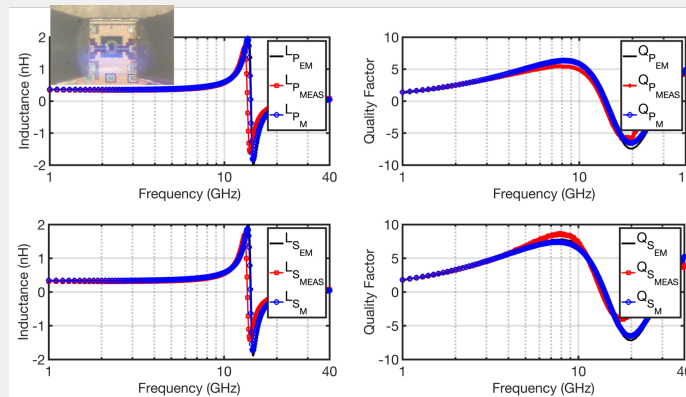
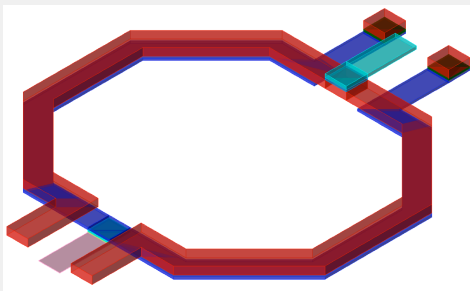
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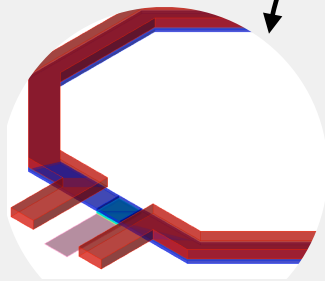
## BALUNS



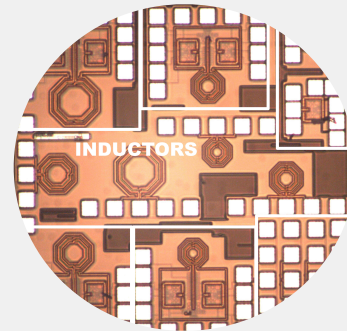
[1] F. Passos *et al.*, "Machine Learning Approaches for Transformer Modeling", *SMACD*, 2022

# MODEL APPLICATIONS

Usage of the model as a normal PDK model inside a design framework

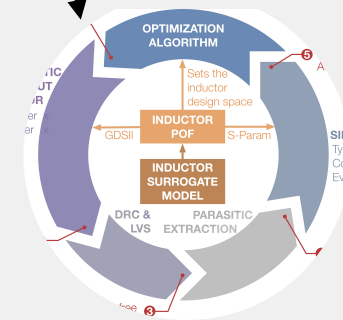


**USAGE AS 'PDK' MODEL**



**RF/MM-WAVE DESIGN**

Circuit/passive component optimization using evolutionary algorithms

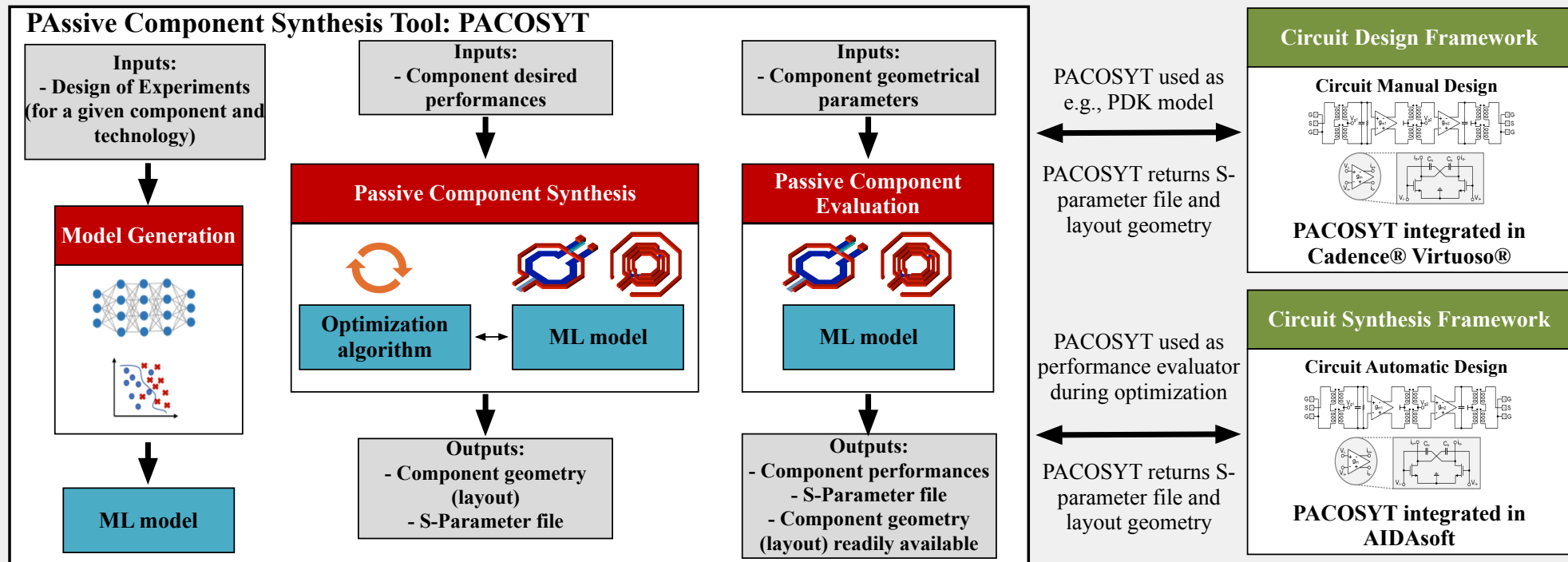


**USAGE IN OPTIMIZATION**



# PASSIVE COMPONENT SYNTHESIS TOOL: PACOSYT

- A tool (PACOSYT) was created to ease the model usage either as a PDK or in optimization



★ Being tested in industrial environment

# PACOSYT GUI

## TRANSFORMER SIMULATION (USAGE AS 'PDK' MODEL)

Select transformer parameters  
and see the performances

## TRANSFORMER OPTIMIZATION

Select the desired transformer  
performances and get the  
geometry

PACOSYT: a Machine Learning based for PAssive COmponent SYthesis Tool

**Geometric Parameters:**

Np: 1  
Dinp: 117  
Wp: 14  
Ns: 1  
Dins: 56  
Ws: 6

Optimize  
Simulate

**Find Device:**

Freq = 28 [GHz]

Lp = 0.3 +/- 5 % [nH]  
Ls = 0.3 +/- 5 % [nH]  
Qp > 10  
Qs > 10

Target: Max. Q

**Simulation:**

Working Frequency (GHz)	Inductance Primary (nH)	Inductance Secondary (nH)	Quality Factor Primary	Quality Factor Secondary	coupling k factor
28.0	0.2638	0.2119	33.91	17.24	-0.2044

Shell:

```
'save(sri = None, lq = None)' - saves the required sri and/or LQ response obtained from the current simulation.
Python 3.8.10 (v3.8.10:3d8993a744, May 3 2021, 09:09:08)
[Clang 12.0.5 (clang-1205.0.22.9)] on darwin
Type "help", "copyright", "credits" or "license" for more information.
>>> load('/Users/fabiopassos/Desktop/WORK/PACOSYT/pacosyt/PASSIVES_RBF_TRANSF_BALUN_28G_SRF38.model')
>>> resp, resp_meta = simulate(np = 1, dinp = 117, wp = 14, ns = 1, dins = 56, ws = 6, nt = 1, din = 117, w = 14)
>>>
```

# PACOSYT USABILITY

- Integrated in Cadence® Virtuoso® for usage as PDK and “inductor finder”

Geometric Parameters:

Np: 1  
Dimp: 135  
Wp: 14  
Ns: 1  
Dms: 89  
Ws: 8

Find Device:

Freq = 28 [GHz]  
Lp = 0.3 +/- 5 [%][nH]  
Ls = 0.3 +/- 5 [%][nH]  
Cp = 10  
Qp > 10

Simulation:

Inductance (nH)

Quality Factor

Working Frequency (GHz)	Inductance Primary (nH)	Inductance Secondary (nH)	Quality Factor Primary	Quality Factor Secondary	coupling k factor
52.0	0.3782	0.3572	21.87	19.65	-0.4172

```

Shell:
This is the PACOSYT shell. Available commands are:
'create(datapath, **options)' - TBD Fits a model using the data from the data file.
'load(filepath)' - Loads the model from the file.
'simulate(*geometry)' - predict S-Param and I/Q for specified geometry.
'optimize(freq, objectives, constraints)' - finds the best geometry
'save(sri = None, ls = None)' - saves the required sri and/or I/Q response obtained from the current simulation.
Python 3.8.5 (default, Feb 18 2022, 13:43:12)
[GCC 4.8.5 20150623 (Red Hat 4.8.5-44)] on Linux
Type 'help', 'copyright', 'credits' or 'license()' for more information.
>>> load('/home/nlourenco/vscode_aida/pacosyt/models/PASSIVES_RFB_TRANSF_280_SRF38.model')
>>> opt_geom = optimize(freq = 28, constraints = [['lp', 0.3, 5.0], ['ls', 0.3, 5.0]], objectives = ['qs', 'qp'])
    
```



- Integrated in AIDAsoft for circuit optimization  
<http://www.aidasoft.com/Home>

2 Stage Amplifier - Original models: /home/aida/works/pace/Circuits/Journal2014Integration/TwoStage/umc\_013

Results	area
89.817	2.6075e-09
89.786	2.4508e-09
89.692	2.4200e-09
89.508	2.3588e-09
88.718	2.0814e-09
87.875	2.0396e-09
87.607	2.0183e-09
87.161	1.9815e-09
86.764	1.8284e-09
86.492	1.7789e-09
85.993	1.7195e-09
85.852	1.6963e-09
85.781	1.6768e-09
85.588	1.6319e-09
85.572	1.5555e-09
84.563	1.5252e-09
84.401	1.5218e-09
84.383	1.3801e-09
84.35	1.3751e-09
83.551	1.3486e-09
82.976	1.3170e-09
82.471	1.1846e-09
82.141	1.1604e-09
81.833	1.1548e-09
81.733	1.1416e-09
81.416	1.1020e-09
81.071	1.0739e-09
80.962	1.0544e-09
80.249	1.0470e-09
80.058	1.0271e-09
79.934	9.9591e-10
79.214	8.8814e-10
77.257	7.8902e-10
76.552	6.8137e-10
75.842	6.4365e-10
75.202	6.1809e-10
74.885	5.9815e-10
74.748	5.9531e-10
74.548	5.8961e-10
74.488	5.8547e-10

Design Variables

- l2p = 8.0000e-07 close to lower limit [1.2E-7]
- l1a = 2.0000e-06
- l1c = 1.3400e-05 close to lower limit [4.4E-6]
- l1e = 7.0000e-07 close to lower limit [1.2E-7]
- l2p = 8.0000e-07 close to lower limit [1.0]
- l1a = 2.0000e-06 close to lower limit [1.0]
- l1b = 1.0000e-01 close to lower limit [1.0]
- l1p = 2.0000e-06 close to lower limit [1.0]
- l1c = 2.0000e-06 close to lower limit [1.0]
- l1e = 4.4000e-06

04

# EXPERIMENTAL RESULTS

# IN HOUSE TOOL: AIDASOFT

- In-house tool developed to optimize circuits
- AIDA uses NSGA-II evolutionary algorithm for circuit optimization
- PACOSYT is integrated and used to create the S-parameter description of passives



The screenshot displays the AIDAsoft software interface for a '2 Stage Amplifier'. The main window shows a circuit schematic on the left and an 'Estimated Layout' on the right. The 'Results' table in the center provides optimization data for various parameters.

Results	gdc	area
89.817	2.6075e-09	
89.786	2.4508e-09	
89.692	2.4260e-09	
89.508	2.3588e-09	
88.718	2.0814e-09	
87.875	2.0396e-09	
87.607	2.0183e-09	
87.161	1.8815e-09	
86.764	1.8284e-09	
86.492	1.7786e-09	
85.993	1.7195e-09	
85.852	1.6963e-09	
85.781	1.6358e-09	
85.588	1.6319e-09	
85.572	1.5555e-09	
84.563	1.5252e-09	
84.401	1.5218e-09	
84.383	1.3801e-09	
84.35	1.3751e-09	
83.551	1.3486e-09	
82.976	1.3170e-09	
82.471	1.1846e-09	
82.141	1.1804e-09	
81.833	1.1548e-09	
81.733	1.1416e-09	
81.416	1.1020e-09	
81.071	1.0739e-09	
80.962	1.0544e-09	
80.249	1.0470e-09	
80.056	1.0071e-09	
79.834	9.9591e-10	
79.214	8.8614e-10	
77.257	7.8902e-10	
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75.842	6.4385e-10	
75.202	6.1808e-10	
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74.548	5.8961e-10	
74.488	5.8547e-10	

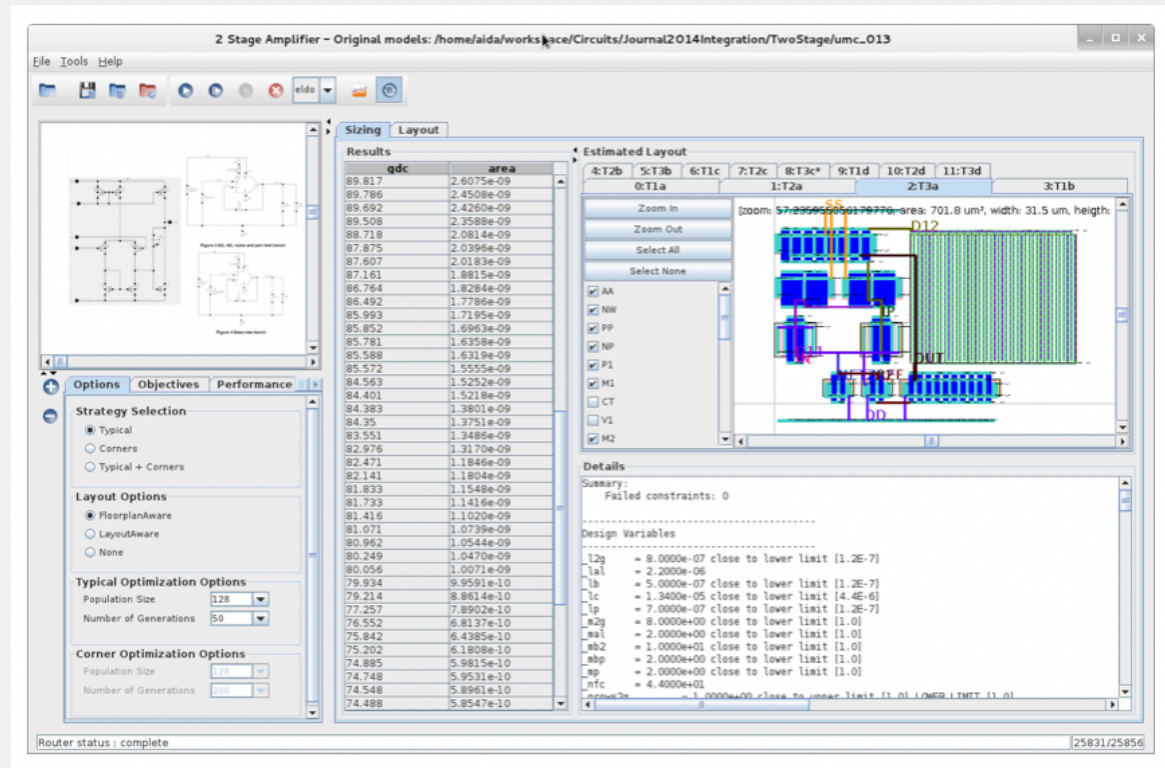
The 'Estimated Layout' window shows a detailed view of the circuit components, including resistors (R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, R21, R22, R23, R24, R25, R26, R27, R28, R29, R30, R31, R32, R33, R34, R35, R36, R37, R38, R39, R40, R41, R42, R43, R44, R45, R46, R47, R48, R49, R50, R51, R52, R53, R54, R55, R56, R57, R58, R59, R60, R61, R62, R63, R64, R65, R66, R67, R68, R69, R70, R71, R72, R73, R74, R75, R76, R77, R78, R79, R80, R81, R82, R83, R84, R85, R86, R87, R88, R89, R90, R91, R92, R93, R94, R95, R96, R97, R98, R99, R100) and capacitors (C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, C31, C32, C33, C34, C35, C36, C37, C38, C39, C40, C41, C42, C43, C44, C45, C46, C47, C48, C49, C50, C51, C52, C53, C54, C55, C56, C57, C58, C59, C60, C61, C62, C63, C64, C65, C66, C67, C68, C69, C70, C71, C72, C73, C74, C75, C76, C77, C78, C79, C80, C81, C82, C83, C84, C85, C86, C87, C88, C89, C90, C91, C92, C93, C94, C95, C96, C97, C98, C99, C100). The 'Details' window shows a summary of failed constraints (0) and design variables (l2g, l1a, l1b, l1c, l1p, n2g, n1a, n1b, n1c, n1p, n1f, n1g).

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- In-house tool developed to optimize circuits
- AIDA uses NSGA-II evolutionary algorithm for circuit optimization
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- Tackles PVT variations
- Yield-aware optimization
- Layout-aware optimization





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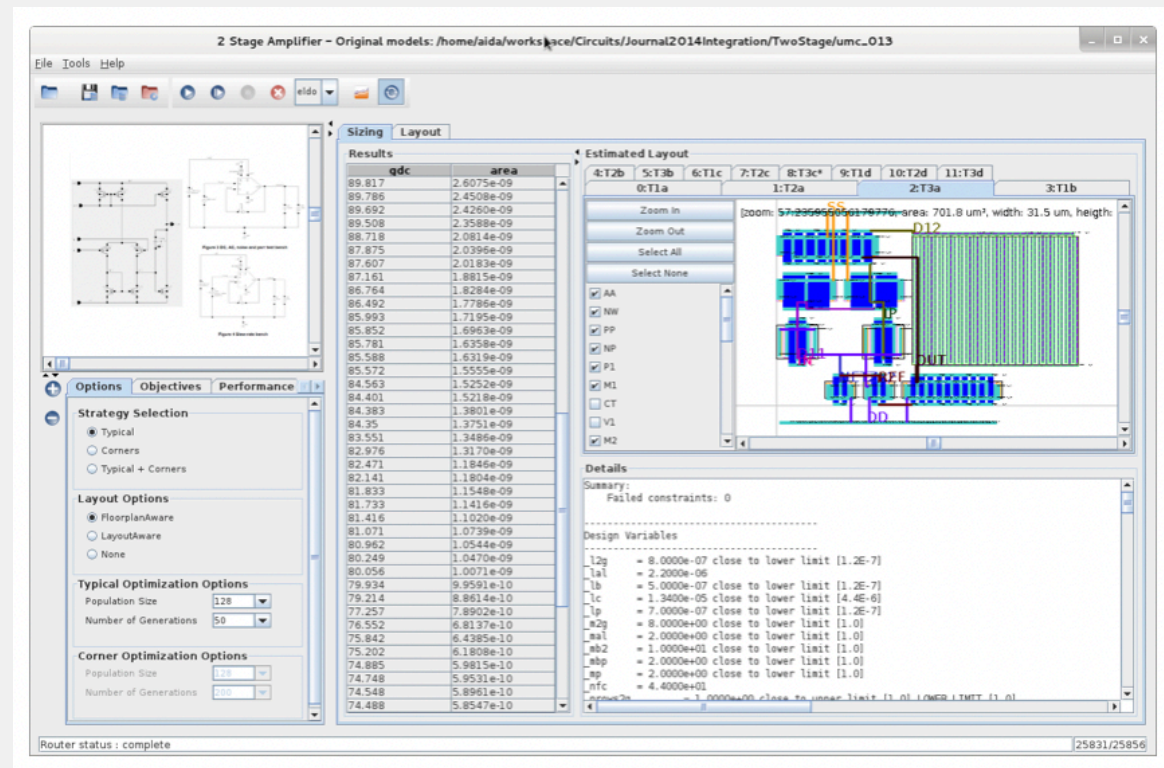


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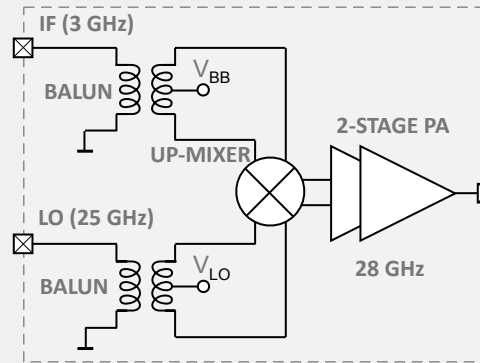
- All tested in Analog/RF circuits
- Currently being extended into mm-Wave and system-level designs

★ Being tested in industrial environment



# PAPER CASE STUDY

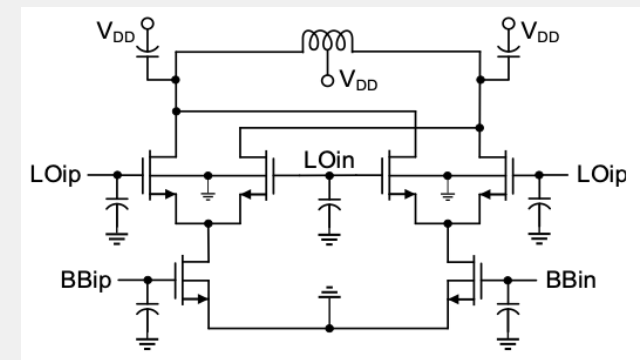
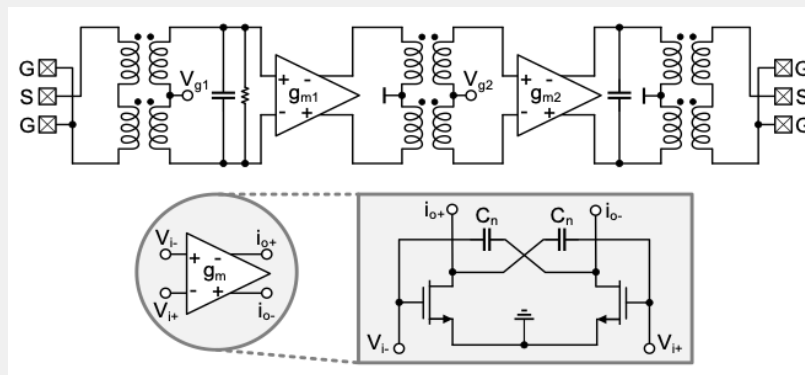
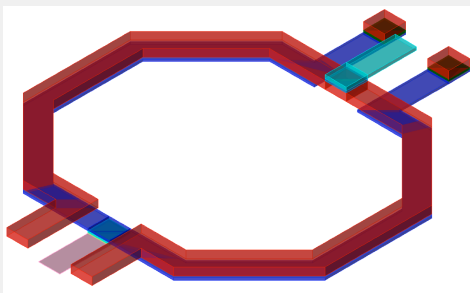
- Transmitter optimization in 65nm technology operating at 26~30GHz with a  $V_{DD}=1.2V$



Baluns

Power Amplifier

Up-Conversion Mixer

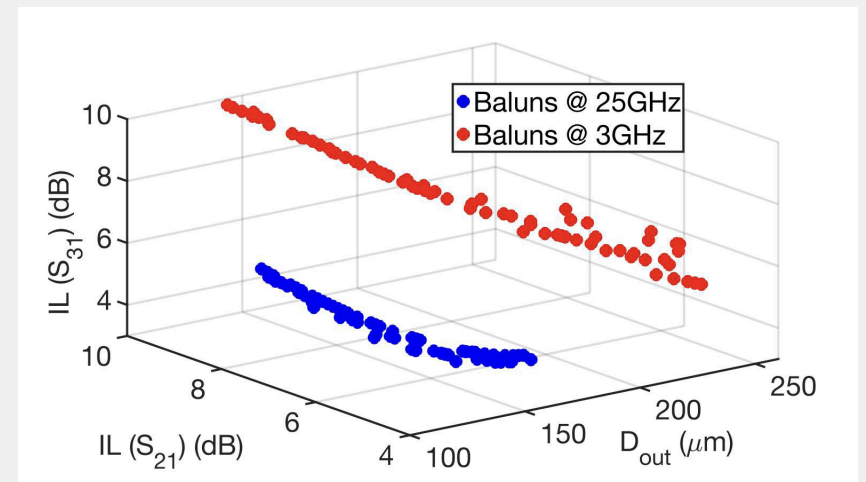




# PASSIVE LEVEL SYNTHESIS

Balun Performance	Balun Specifications
Amplitude imbalance	< 1 dB
Phase Imbalance	< 10°
Insertion Loss ( $S_{21}$ )	Minimize
Insertion Loss ( $S_{21}$ )	Minimize
Area	Minimize

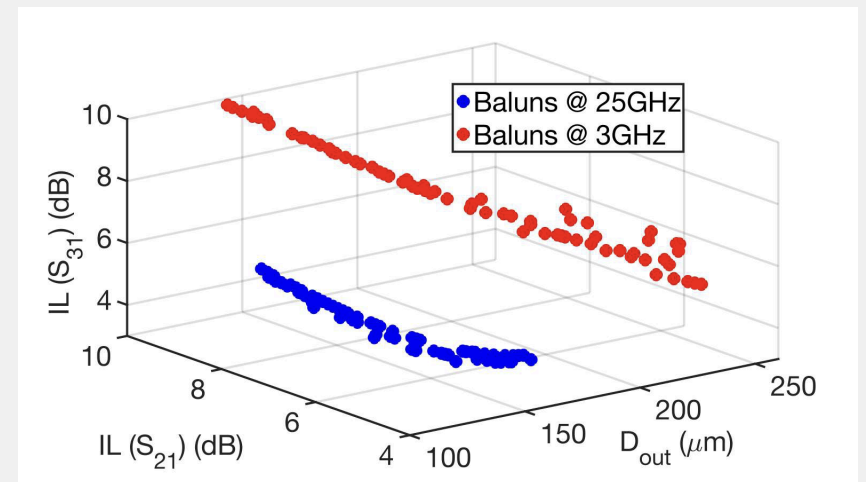
- Two optimizations performed with 64 individuals and 50 generations
- Optimization lasted 4m



# PASSIVE LEVEL SYNTHESIS

Balun Performance	Balun Specifications
Amplitude imbalance	< 1 dB
Phase Imbalance	< 10°
Insertion Loss ( $S_{21}$ )	Minimize
Insertion Loss ( $S_{21}$ )	Minimize
Area	Minimize

- Two optimizations performed with 64 individuals and 50 generations
- Optimization lasted 4m
- 3,200 transformers evaluated
- If performed with EM simulation it would last approx. 11 days (average of 5 minutes per EM simulation)



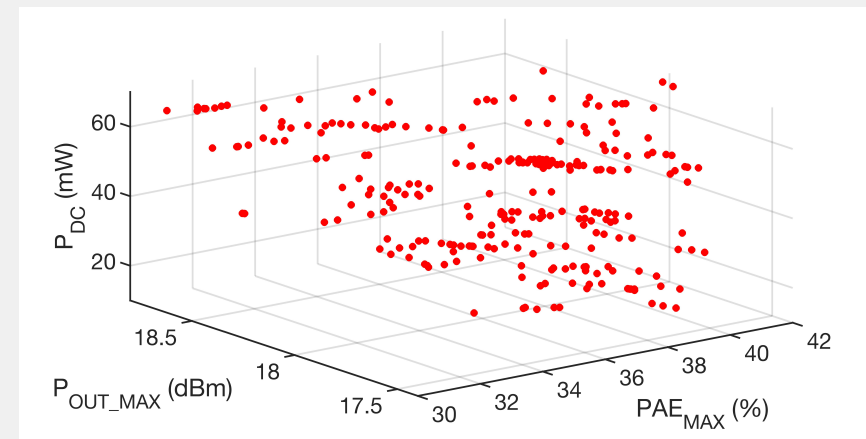
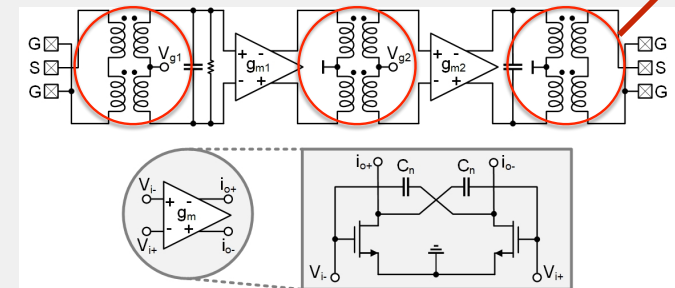
- **Better efficiency using a model !**

# CIRCUIT LEVEL SYNTHESIS

PA Performance	PA Specifications
$S_{11}$ @ 26.5-30 GHz	< -12 dB
$S_{22}$ @ 26.5-30 GHz	< -5 dB
$S_{21}$ @ 26.5-30 GHz	> 12 dB
$S_{21}$ Variation (@ 26.5-30 GHz)	< 1.7dB
Rollet Stb Factor @ 1Hz-120GHz	> 1
$P_{DC}$	Minimize (< 70 mW)
$P_{OUT\_MAX}$	Maximize (> 8 dBm)
$PAE_{MAX}$	Maximize (> 20%)
Power Gain <sub>MAX</sub>	> 12 dB
OP1dB	> 10 dBm

- Optimization performed with 400 individuals and 150 generations
- Optimization lasted ~42h

evaluated with the model

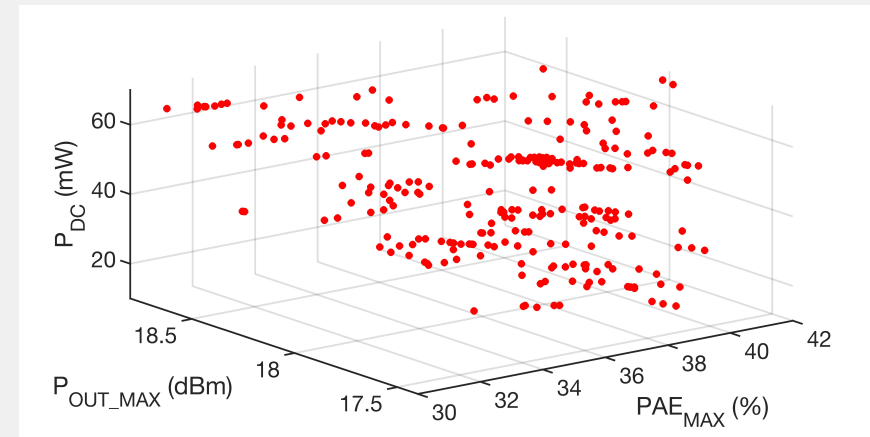
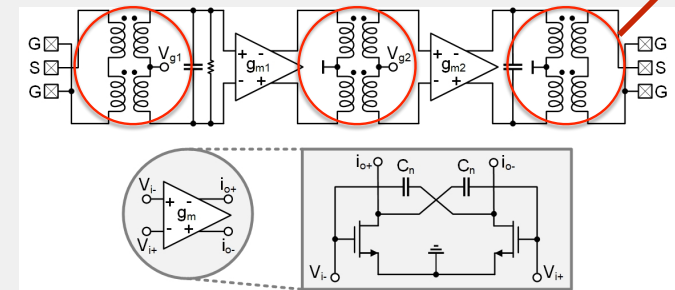


# CIRCUIT LEVEL SYNTHESIS

PA Performance	PA Specifications
$S_{11}$ @ 26.5-30 GHz	< -12 dB
$S_{22}$ @ 26.5-30 GHz	< -5 dB
$S_{21}$ @ 26.5-30 GHz	> 12 dB
$S_{21}$ Variation (@ 26.5-30 GHz)	< 1.7dB
Rollet Stb Factor @ 1Hz-120GHz	> 1
$P_{DC}$	Minimize (< 70 mW)
$P_{OUT\_MAX}$	Maximize (> 8 dBm)
$PAE_{MAX}$	Maximize (> 20%)
Power Gain <sub>MAX</sub>	> 12 dB
OP1dB	> 10 dBm

- Optimization performed with 400 individuals and 150 generations
- Optimization lasted ~42h
- 180,000 transformers evaluated
- If performed with EM simulation it would last approx. 2 years (average of 5 minutes per EM simulation)
- **Only possible using a model !!!!**

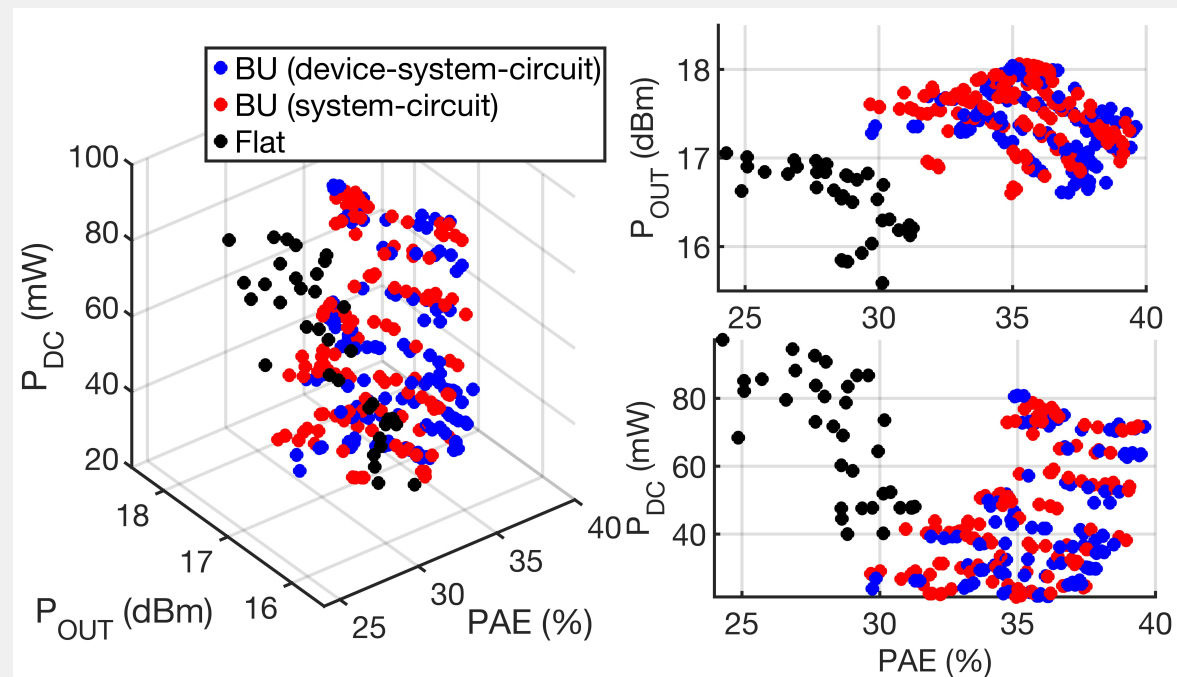
evaluated with the model



# SYSTEM LEVEL SYNTHESIS

- Three different optimization methodologies:
  1. Bottom-up (three levels, device-circuit-system)
  2. Bottom-up (two levels, system-circuit)
  3. Flat (everything optimized at once)

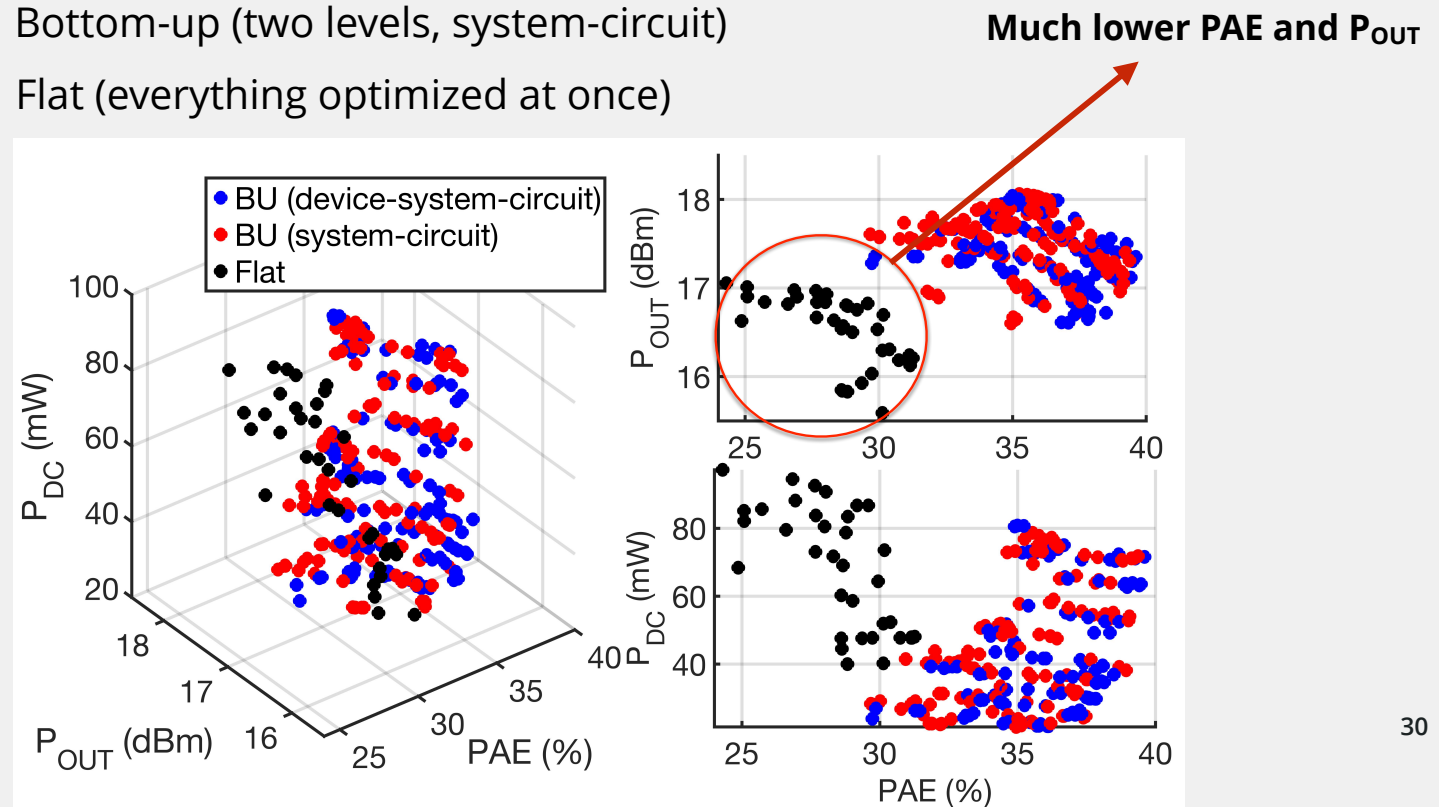
Tx Performance	Tx Specifications
<b>Conversion Gain</b>	> 20 dB
$P_{DC}$	Minimize (< 100 mW)
$P_{OUT\_MAX}$	Maximize (> 8 dBm)
$PAE_{MAX}$	Maximize (> 20%)
<b>Power Gain</b>	> 12 dB
<b>OP1dB</b>	> 2.5 dBm



# SYSTEM LEVEL SYNTHESIS

- Three different optimization methodologies:
  1. Bottom-up (three levels, device-circuit-system)
  2. Bottom-up (two levels, system-circuit)
  3. Flat (everything optimized at once)

Tx Performance	Tx Specifications
<b>Conversion Gain</b>	> 20 dB
<b><math>P_{DC}</math></b>	Minimize (< 100 mW)
<b><math>P_{OUT\_MAX}</math></b>	Maximize (> 8 dBm)
<b><math>PAE_{MAX}</math></b>	Maximize (> 20%)
<b>Power Gain</b>	> 12 dB
<b>OP1dB</b>	> 2.5 dBm

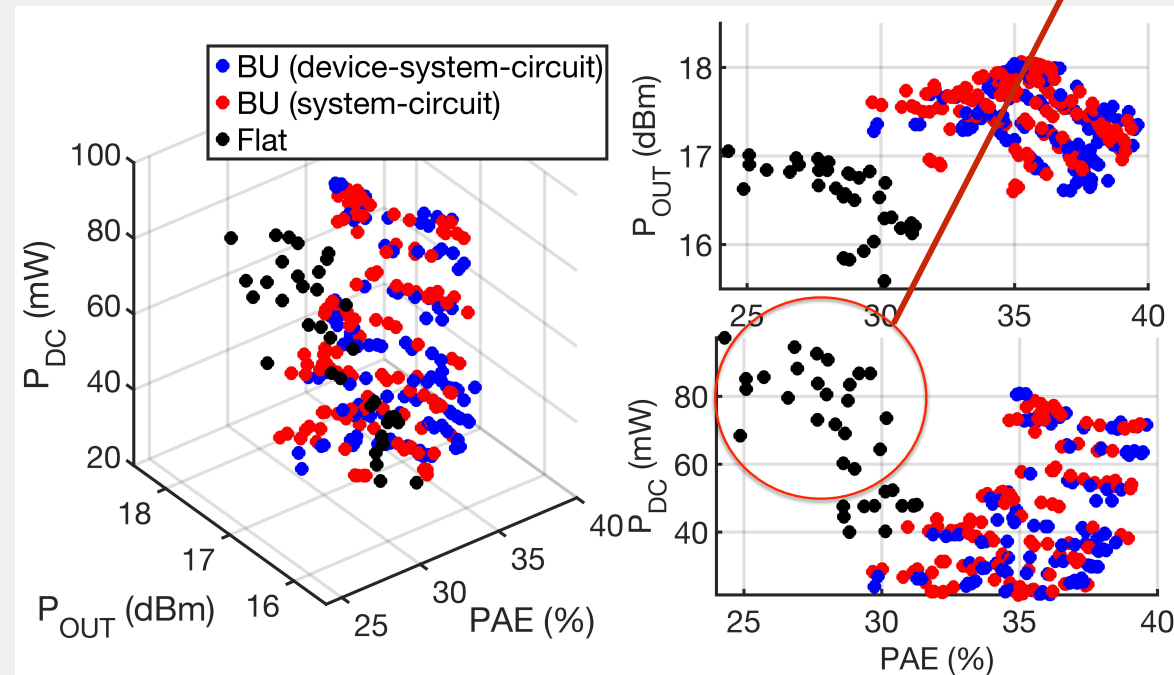


# SYSTEM LEVEL SYNTHESIS

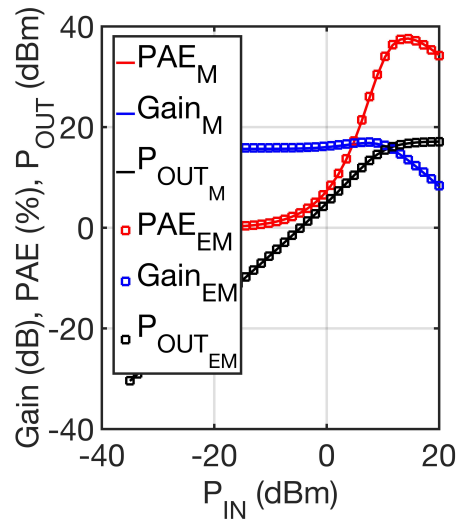
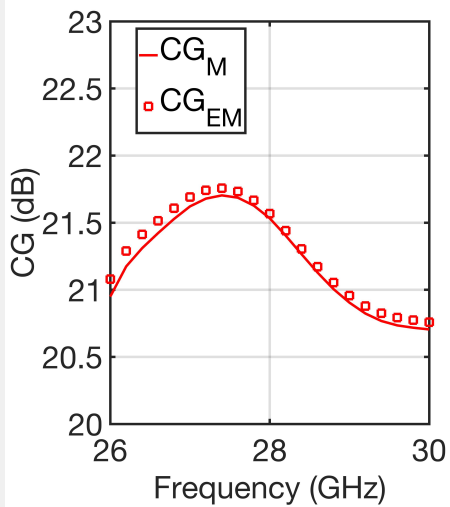
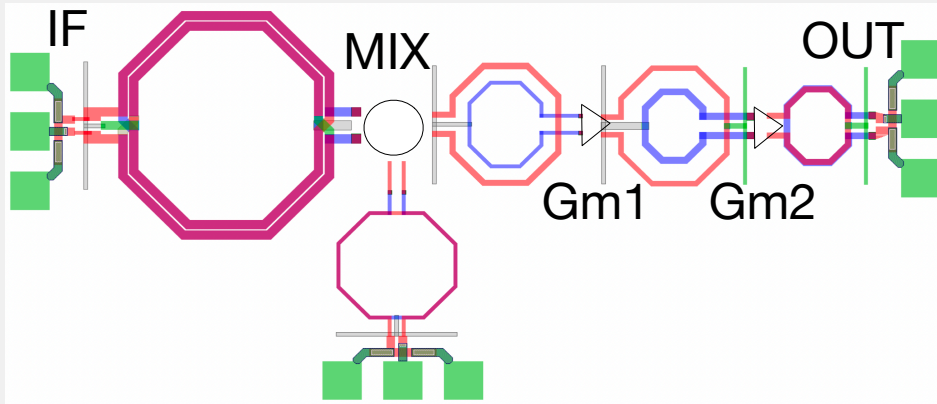
- Three different optimization methodologies:

1. Bottom-up (three levels, device-circuit-system)
2. Bottom-up (two levels, system-circuit)
3. Flat (everything optimized at once)

Tx Performance	Tx Specifications
<b>Conversion Gain</b>	> 20 dB
<b><math>P_{DC}</math></b>	Minimize (< 100 mW)
<b><math>P_{OUT\_MAX}</math></b>	Maximize (> 8 dBm)
<b><math>PAE_{MAX}</math></b>	Maximize (> 20%)
<b>Power Gain</b>	> 12 dB
<b>OP1dB</b>	> 2.5 dBm



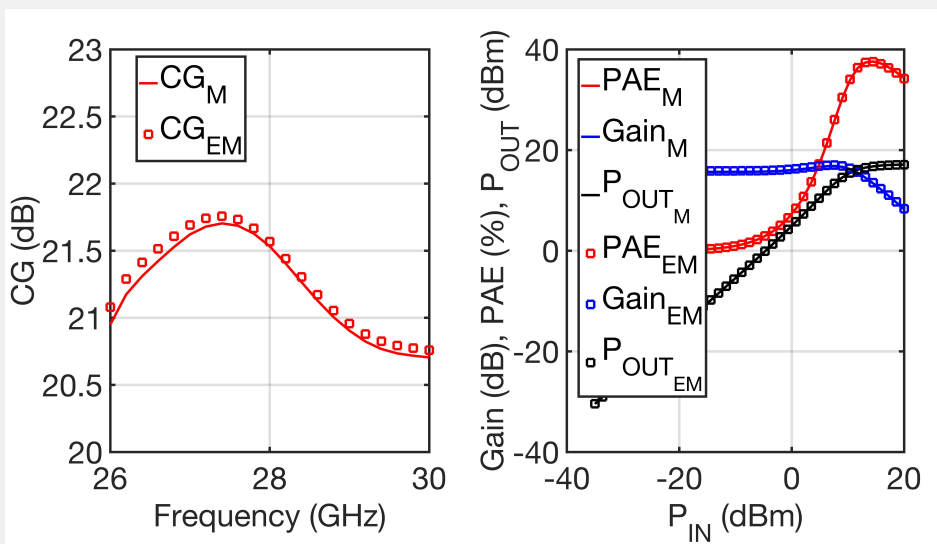
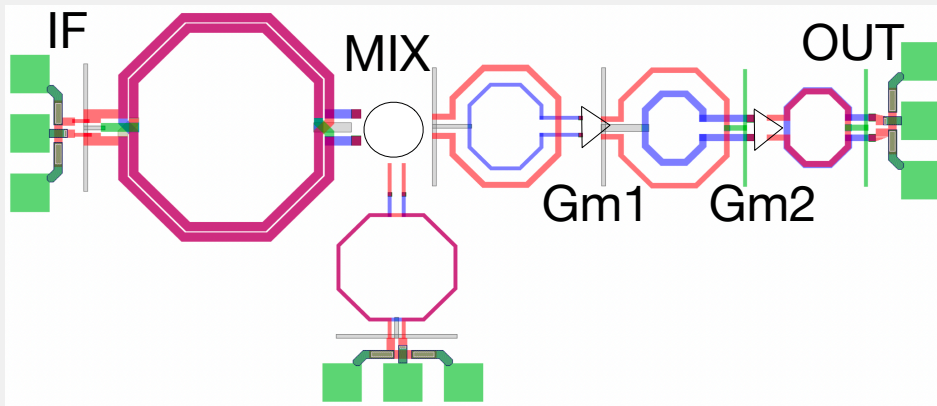
# ONE OF THE DESIGNS...



Tx Performance	Tx Performances (model)
<b>Conversion Gain</b>	21.53 dB
<b>P<sub>DC</sub></b>	21.27 mW
<b>P<sub>OUT_MAX</sub></b>	17.08 dBm
<b>PAE<sub>MAX</sub></b>	37.59 %
<b>Power Gain</b>	16.84 dB
<b>OP1dB</b>	16.44 dBm

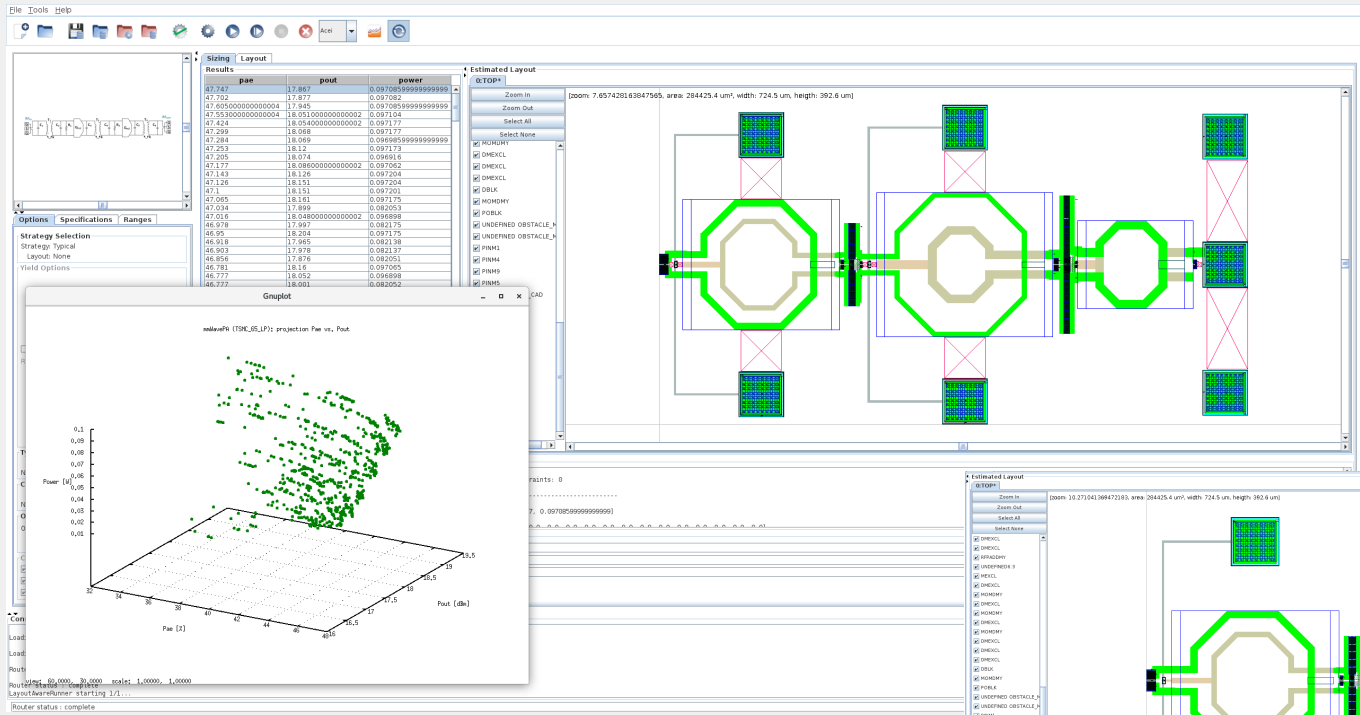


# ONE OF THE DESIGNS...



Tx Performance	Tx Performances (model)	Tx Performances (EM sim)	Error (%)
<b>Conversion Gain</b>	21.53 dB	21.57 dB	0.0019
<b>P<sub>DC</sub></b>	21.27 mW	21.27 mW	-
<b>P<sub>OUT_MAX</sub></b>	17.08 dBm	17.06 mW	0.0012
<b>PAE<sub>MAX</sub></b>	37.59 %	37.55 %	0.0011
<b>Power Gain</b>	16.84 dB	17.07 dB	0.0106
<b>OP1dB</b>	16.44 dBm	16.39 dBm	0.0031

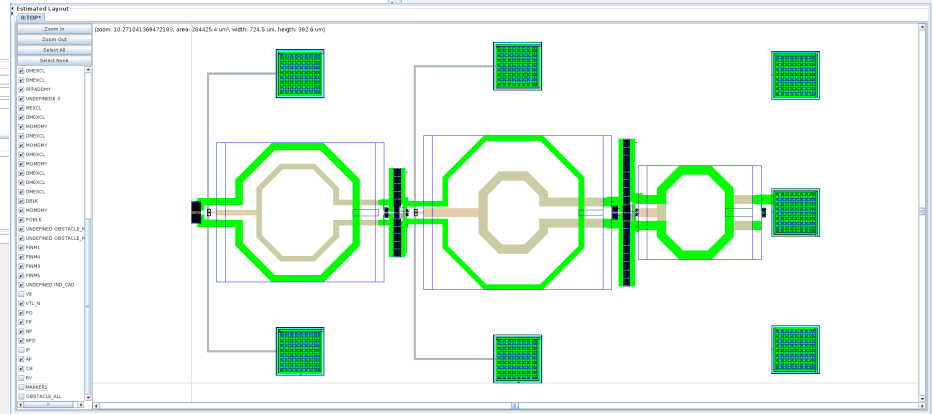
# FUTURE WORK: PVT AND LAYOUT-AWARE POF<sub>s</sub>...



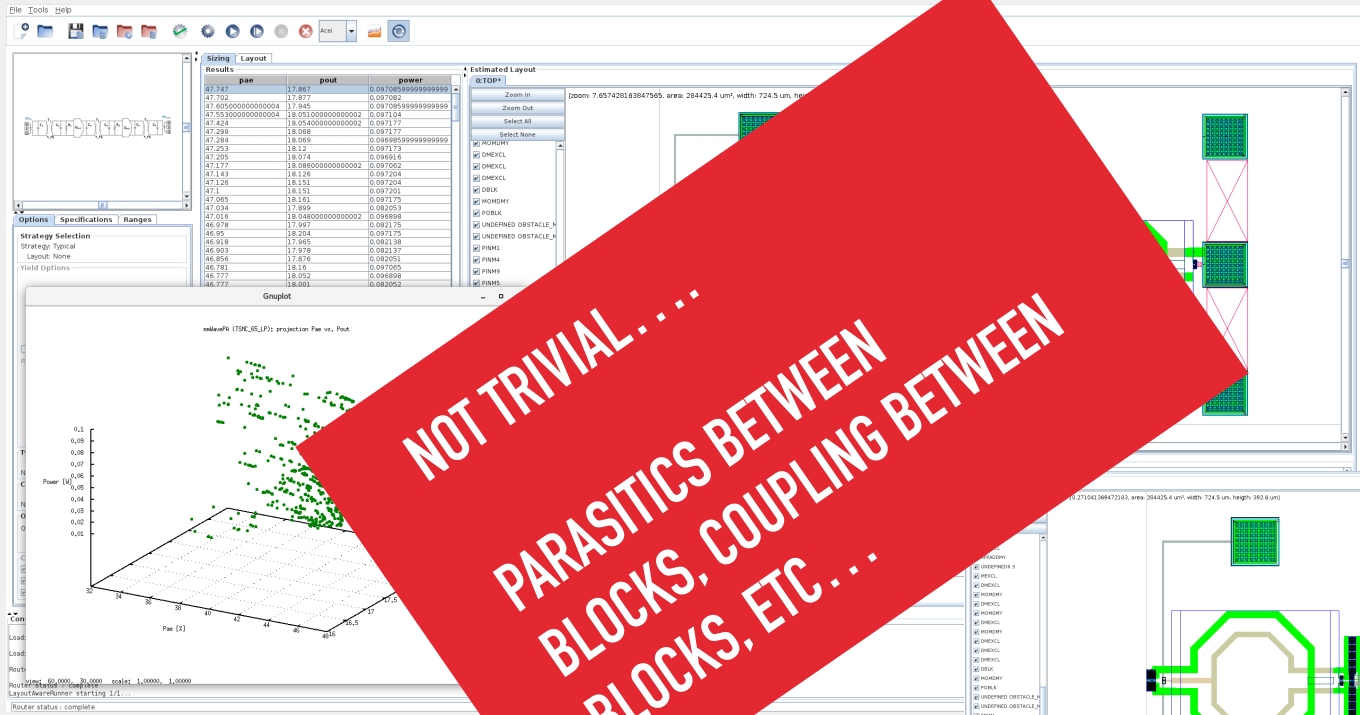
Automatic layout generation



Taking into account PVT variations

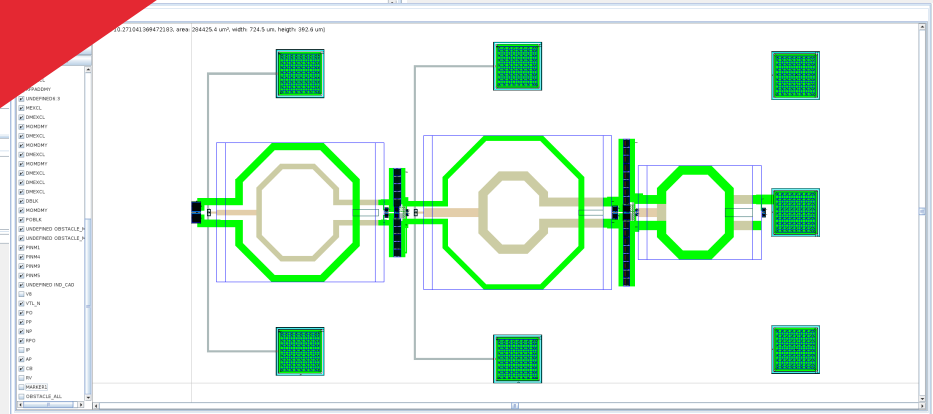


# FUTURE WORK: PVT AND LAYOUT-AWARE POF<sub>s</sub>...



**NOT TRIVIAL . . . .  
PARASITICS BETWEEN  
BLOCKS, COUPLING BETWEEN  
BLOCKS, ETC . . . .**

Automatic layout generation



Taking into account PVT variations

# CONCLUSIONS

01

## **BOTTOM-UP STRATEGY WAS APPLIED TO THE DESIGN OF A TRANSMITTER**

Baluns optimized at lower level, then the PA at circuit level and than the MIX at system level

02

## **BALUNS AND TRANSFORMERS SYNTHESIZED USING ML MODEL**

The model allows for optimal passive component design in minutes

03

## **HUNDREDS OF CIRCUITS SYNTHESIZED IN DAYS RATHER THAN WEEKS/MONTHS**

Huge improvement in efficiency

04

## **IN THE FUTURE OPTIMIZE CIRCUITS TAKING INTO ACCOUNT PVT VARIATIONS AND LAYOUT**

Enabling a fully sizing-layout automated methodology

# I invite you all to submit works to...

## 2023 SMACD Conference [WWW.SMACD-CONFERENCE.ORG](http://WWW.SMACD-CONFERENCE.ORG)

HOME Call for Papers EDA Competition IC Design Contest Conference- Sponsorship

**SMACD 2023**  
3<sup>rd</sup> - 5<sup>th</sup> of July 2023, Funchal - Madeira Island, Portugal

CALL FOR PAPERS  
CALL FOR EDA COMPETITION  
CALL FOR IC DESIGN CONTEST  
CALL FOR TUTORIALS AND SPECIAL SESSIONS  
PAPER SUBMISSION

SMACD 2023: 3 TO 5 JULY, FUNCHAL - MADEIRA ISLAND, PORTUGAL

The **2023 edition** of the International Conference on Synthesis, Modeling, Analysis and Simulation Methods, and Applications to Circuit Design (SMACD) will be held from **3 to 5 July**. It will take place at VidaMar Resort Hotel, a stunning location on Madeira island in Portugal.

SMACD is a forum devoted to modeling, simulation, and synthesis for Analog, Mixed-signal, RF (AMS/RF), and multi-domain (nanoelectronics, biological, MEMS, optoelectronics, etc.) integrated circuits and systems, as well as, emerging technologies and applications. Open-source tools and methods for IC design and experiences with modeling, simulation, and synthesis techniques in diverse application areas are also welcomed. Objective technologies include CMOS, beyond CMOS, and More-than-Moore such as MEMs, power devices, sensors, passives, etc.

## Topical Collection in ELECTRONICS MDPI

**electronics**  
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IMPACT FACTOR 2.690  
CITESCORE 3.7

Advanced Design Techniques and EDA Methodologies for Analog, RF and MM - Wave Circuit Design

**Guest Editors**  
Dr. Fábio Passos, Dr. Nuno Lourenço, Prof. Dr. Ricardo Martins

**Topical Collection**

[mdpi.com/si/101759](http://mdpi.com/si/101759) Invitation to submit

THANK YOU!

FABIO.PASSOS@LX.IT.PT



# ML TECHNIQUES

- All implemented/tested using Python libraries

## GAUSSIAN PROCESS REGRESSION

- Near parameterless technique
- internal optimization which defines its parameters

IN THE PAPER

## RADIAL BASIS FUNCTION

- Simpler than GPR and therefore require less memory

IN THE PAPER

## NEAREST NEIGHBOR

- Simplest technique available (serves as baseline for the others)

IN THE PAPER

## KERNEL RIDGE REGRESSION

- Similar to GPR but without the internal optimization

TESTED AFTERWARDS

## RANDOM FOREST REGRESSION

- Simple model which may be useful to identify multiple trends in the data

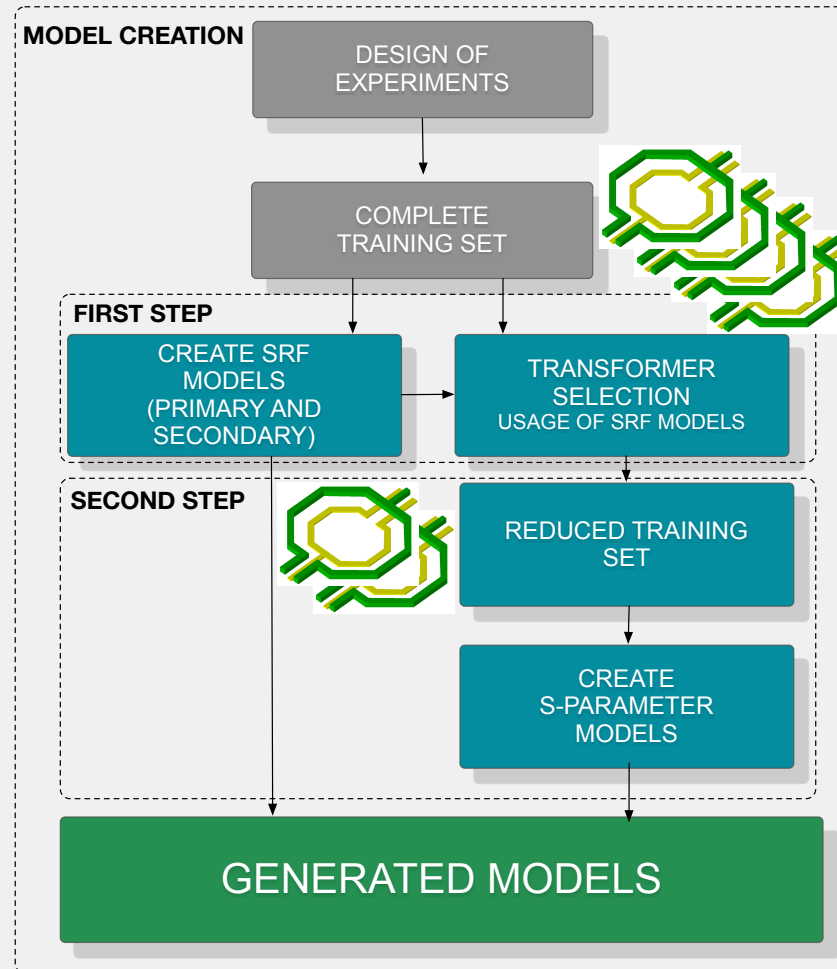
TESTED AFTERWARDS

## ARTIFICIAL NEURAL NETWORKS

- Good for big data sets and high number of variables

TESTED AFTERWARDS

# MODEL STRATEGY



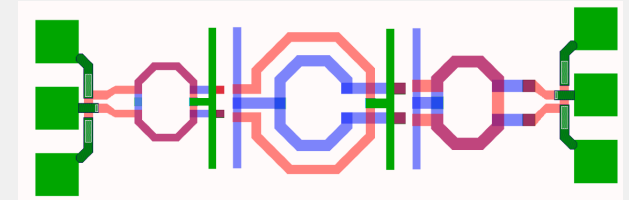
# MODEL RESULTS

		Technique												
		GPR*		KRR		RBF*		RFR		NN*		ANN		
Frequency	Performance	ME (%)	MAPE (%)	ME (%)	MAPE (%)	ME (%)	MAPE (%)	ME (%)	MAPE (%)	ME (%)	MAPE (%)	ME (%)	MAPE (%)	
28GHz	N=1:1*	L <sub>P</sub>	0.23	0.12	1.04	0.22	0.35	0.16	14.24	2.47	10.62	3.35	2.30	0.50
		Q <sub>P</sub>	3.84	1.38	4.86	1.81	3.77	1.53	22.11	9.14	22.14	4.47	139.36	7.82
		L <sub>S</sub>	0.26	0.1	1.03	0.31	0.24	0.08	13.09	4.46	16.44	5.61	2.89	0.65
		Q <sub>S</sub>	7.17	1.98	12.32	4.04	2.2	0.78	16.65	7.90	34.18	9.71	30.19	4.05
		k	0.55	0.18	0.81	0.25	0.45	0.21	28.18	6.56	25.38	8.87	5.84	1.08
	N=1:2	L <sub>P</sub>	0.57	0.14	0.48	0.15	0.53	0.17	12.03	2.94	11.92	3.88	1.63	0.66
		Q <sub>P</sub>	4.59	1.78	5.41	1.84	5.28	1.94	25.51	13.93	27.33	8.39	28.16	5.06
		L <sub>S</sub>	0.39	0.16	0.46	0.22	0.53	0.17	15.93	4.84	19.21	7.26	2.74	0.80
		Q <sub>S</sub>	4.73	1.21	3.53	1.48	4.55	1.49	16.64	7.93	19.95	5.24	18.91	4.31
		k	0.77	0.25	1.15	0.46	0.84	0.28	39.20	9.14	34.19	12.82	3.17	1.09
	N=2:1	L <sub>P</sub>	0.16	0.14	0.29	0.22	0.06	0.05	12.58	6.87	36.05	10.18	2.26	1.40
		Q <sub>P</sub>	1.63	1.13	1.54	0.9	0.71	0.36	18.37	9.83	31.87	10.65	15.53	7.34
		L <sub>S</sub>	0.62	0.44	1.09	0.96	0.1	0.07	13.04	4.87	12.96	6.08	2.64	1.01
		Q <sub>S</sub>	5.83	4.04	6.76	5.14	1.85	0.97	20.57	10.80	29.00	13.96	8.68	3.43
		k	0.5	0.43	1.1	0.82	0.4	0.25	18.07	10.56	35.74	13.40	2.69	0.89

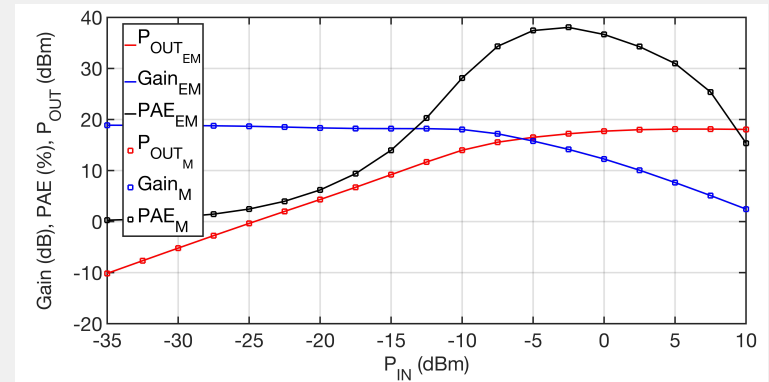
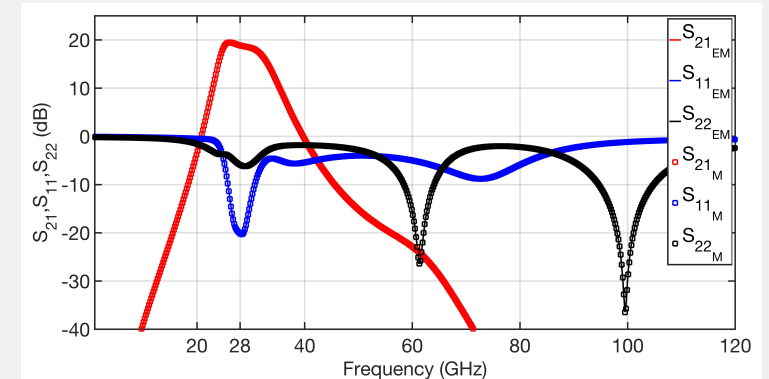
\* Present in the paper



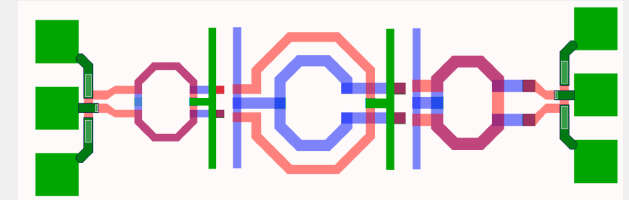
# CIRCUIT SYNTHESIS USING PACOSYT AND AIDA



PA Performance	PA Specifications	Performances of Selected PA @ 28 GHz (PACOSYT)
$S_{11}$ @ 26.5-30 GHz	< -12 dB	-20.102 dB
$S_{22}$ @ 26.5-30 GHz	< -5 dB	-5.850 dB
$S_{21}$ @ 26.5-30 GHz	> 12 dB	18.885 dB
$S_{21}$ Variation (@ 26.5-30 GHz)	< 1.7dB	Complies with spec.
<i>Rollet Stb Factor</i> @ 1Hz-120GHz	> 1	Complies with spec.
$P_{DC}$	Minimize (< 70 mW)	33.9874 mW
$P_{OUT\_MAX}$	Maximize (> 8 dBm)	18.11 dBm
$PAE_{MAX}$	Maximize (> 20%)	38.08 %
$Power\ Gain_{MAX}$	> 12 dB	18.88 dB
$P_{1dB}$	> 10 dBm	14.128 dBm



# CIRCUIT SYNTHESIS USING PACOSYT AND AIDA



PA Performance	PA Specifications	Performances of Selected PA @ 28 GHz (PACOSYT)	Performances of Selected PA @ 28 GHz (Transf. EM simulated)	Error (%)
$S_{11}$ @ 26.5-30 GHz	< -12 dB	-20.102 dB	-20.056 dB	0.087
$S_{22}$ @ 26.5-30 GHz	< -5 dB	-5.850 dB	-5.856 dB	0.230
$S_{21}$ @ 26.5-30 GHz	> 12 dB	18.885 dB	18.881 dB	0.020
$S_{21}$ Variation (@ 26.5-30 GHz)	< 1.7dB	Complies with spec.	Complies with spec.	-
<i>Rollet Stb Factor</i> @ 1Hz-120GHz	> 1	Complies with spec.	Complies with spec.	-
$P_{DC}$	Minimize (< 70 mW)	33.9874 mW	33.9877 mW	0.001
$P_{OUT\_MAX}$	Maximize (> 8 dBm)	18.11 dBm	18.12 dBm	0.055
$PAE_{MAX}$	Maximize (> 20%)	38.08 %	38.04%	0.105
$Power\ Gain_{MAX}$	> 12 dB	18.88 dB	18.89 dB	0.052
$P_{1dB}$	> 10 dBm	14.128 dBm	14.125 dBm	0.021

