EFFICIENT HIERARCHICAL MM-WAVE SYSTEM SYNTHESIS WITH EMBEDDED ACCURATE TRANSFORMER AND BALUN ML MODELS

FÁBIO PASSOS

N. LOURENÇO, R. MARTINS, L. MENDES, J. VAZ, N. HORTA

instituto de telecomunicações

DEEC
DEPARTAMENTO DE ENGENHARIA ELETROTÉCNICA E DE COMPUTADORES
TÉCNICO LISBOA

ASIA SOUTH PACIFIC DAC DESIGN AUTOMATION CONFERENCE

Overview

- MOTIVATION
- SYSTEM DESIGN METHODOLOGIES
- MODELING PASSIVE COMPONENTS
- EXPERIMENTAL RESULTS
- CONCLUSIONS

01

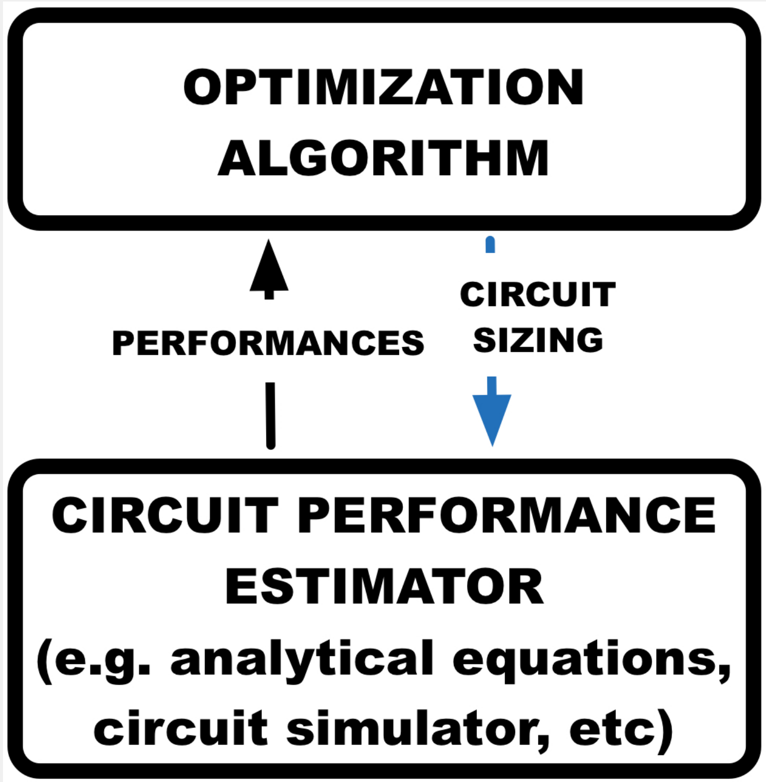
MOTIVATION

MOTIVATION

- Entering in 5G/6G era, mm-Wave circuits and systems are key technology enablers
- We need circuits with high performances, low cost (small area), power efficient, etc
- Such performances are difficult to obtain using manual/traditional design methodologies
- Therefore, there is a need for a more efficient methodology that can be used by designers

OUR APPROACH...

Usage of optimization algorithms to automatically design circuits...



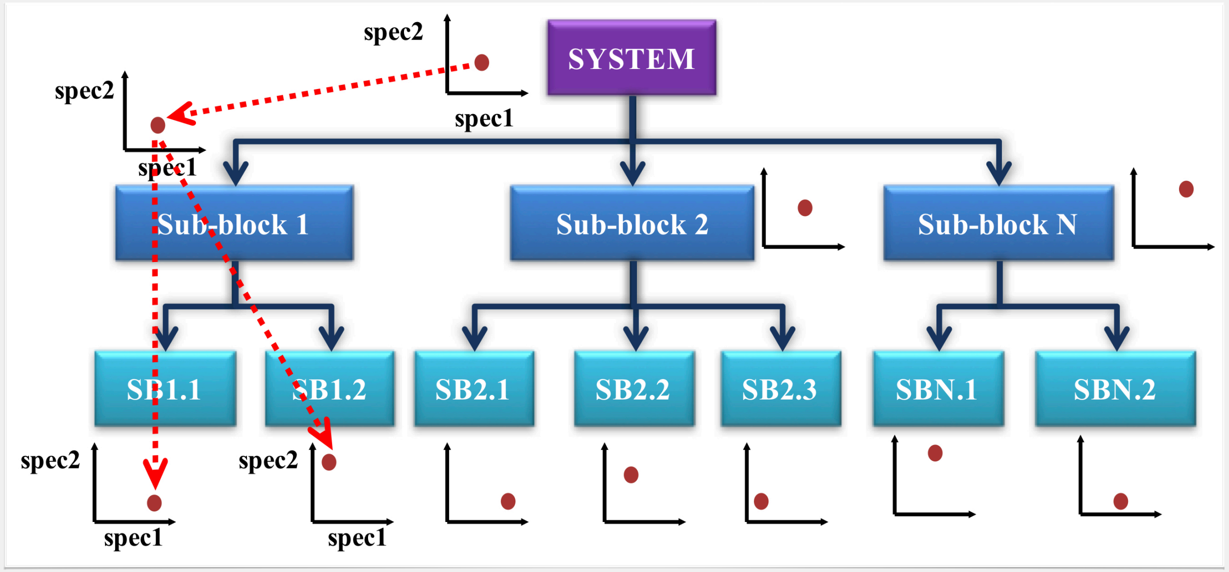
02

SYSTEM DESIGN METHODOLOGIES

(…focusing on optimization-based design methodologies)

TOP-DOWN METHODOLOGIES

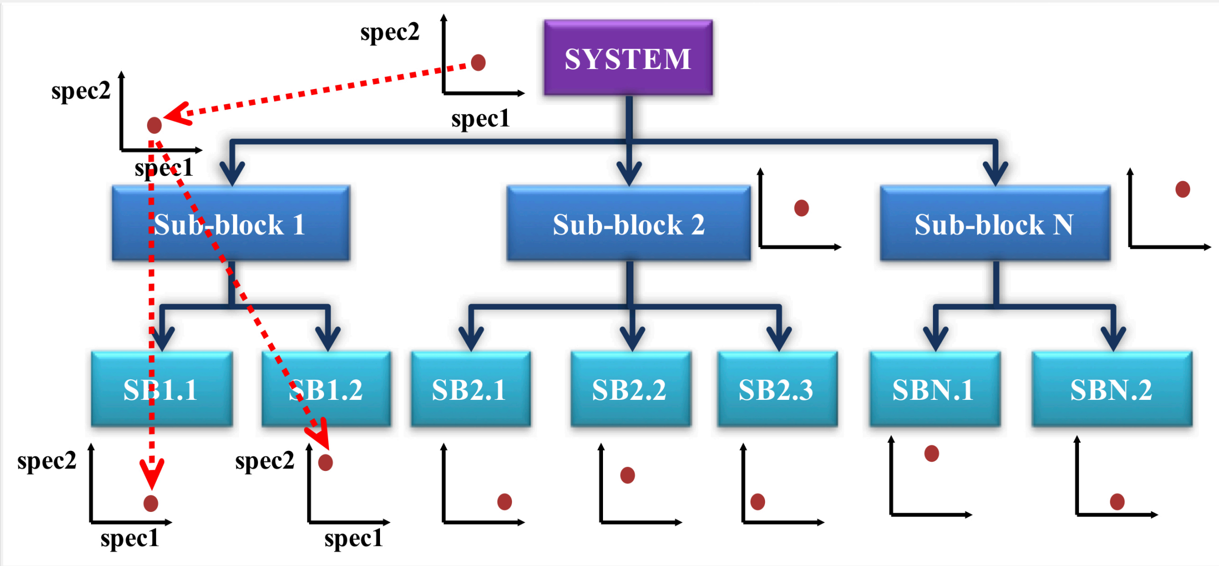
- Divide and conquer strategies, system hierarchical decomposition



- Designer starts from the system level specifications

TOP-DOWN METHODOLOGIES

- Divide and conquer strategies, system hierarchical decomposition

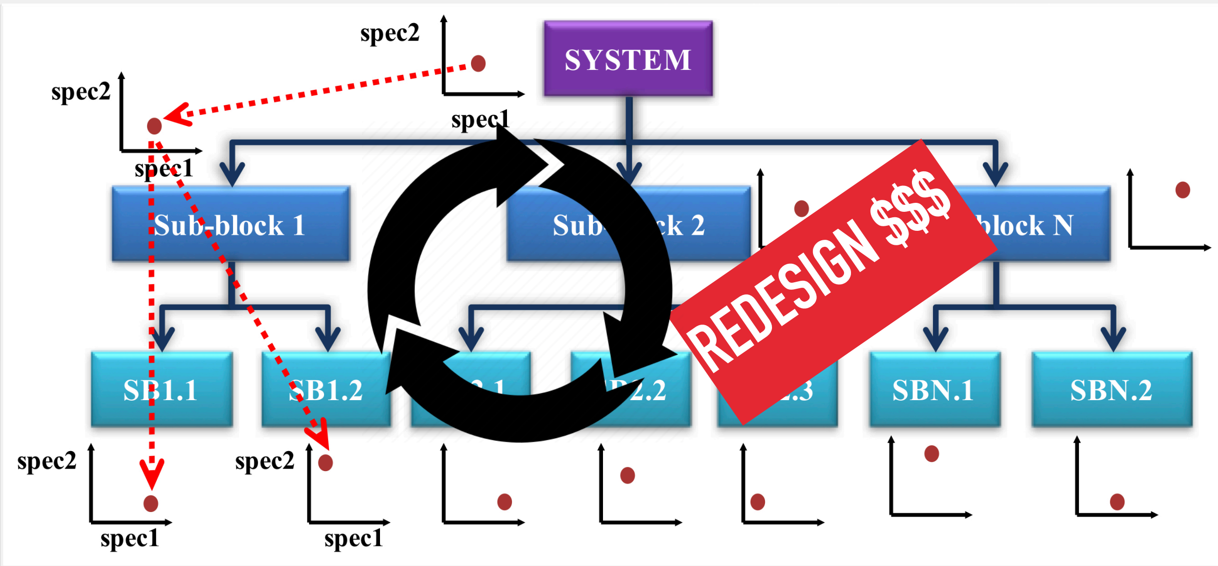


- Designer starts from the system level specifications

- Specifications transmitted down the hierarchy

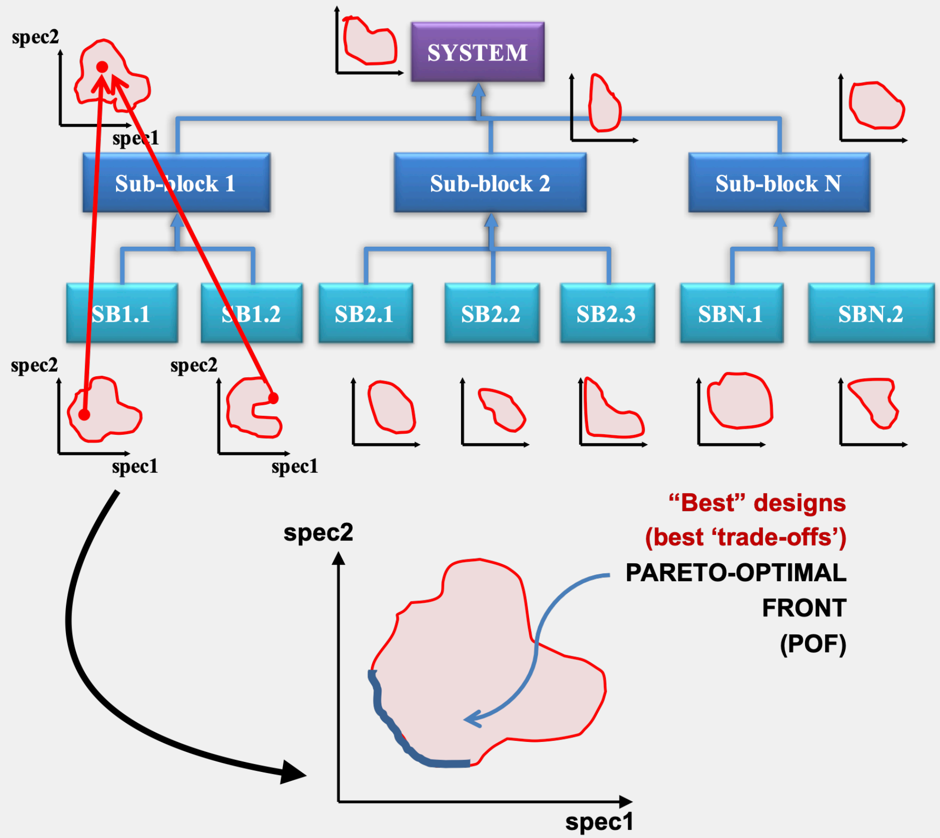
TOP-DOWN METHODOLOGIES

- Divide and conquer strategies, system hierarchical decomposition



- Designer starts from the system level specifications
- Specifications transmitted down the hierarchy
- The fact that specifications are transmitted down without knowing if they will be realizable by lower level sub-blocks may lead to costly redesign iterations…!

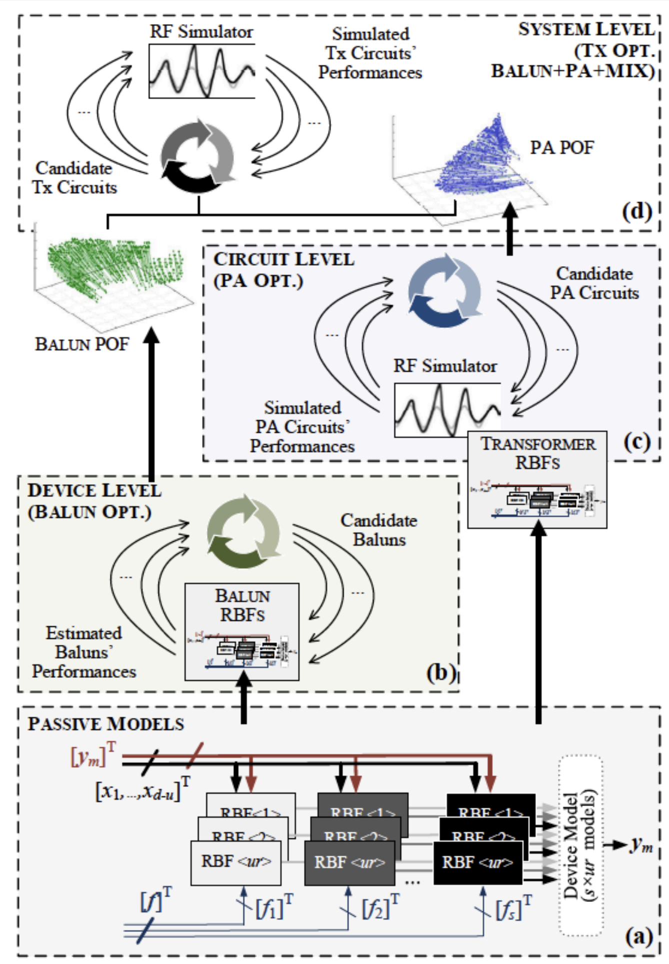
BOTTOM-UP METHODOLOGIES

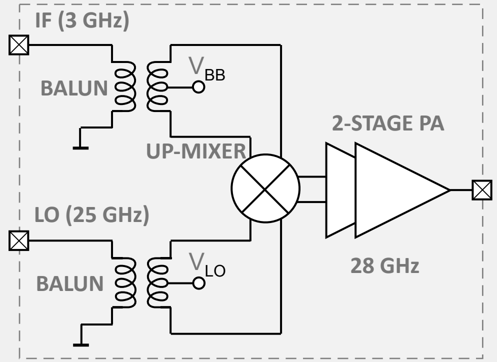


- Designer starts from the bottom level
- Ensures all levels are feasible (with the desired specifications)
- Multi-objective algorithms are used to pass POFs to the upper level

EXPERIMENTAL CASE

- 28GHz mm-Wave transmitter in 65nm CMOS technology

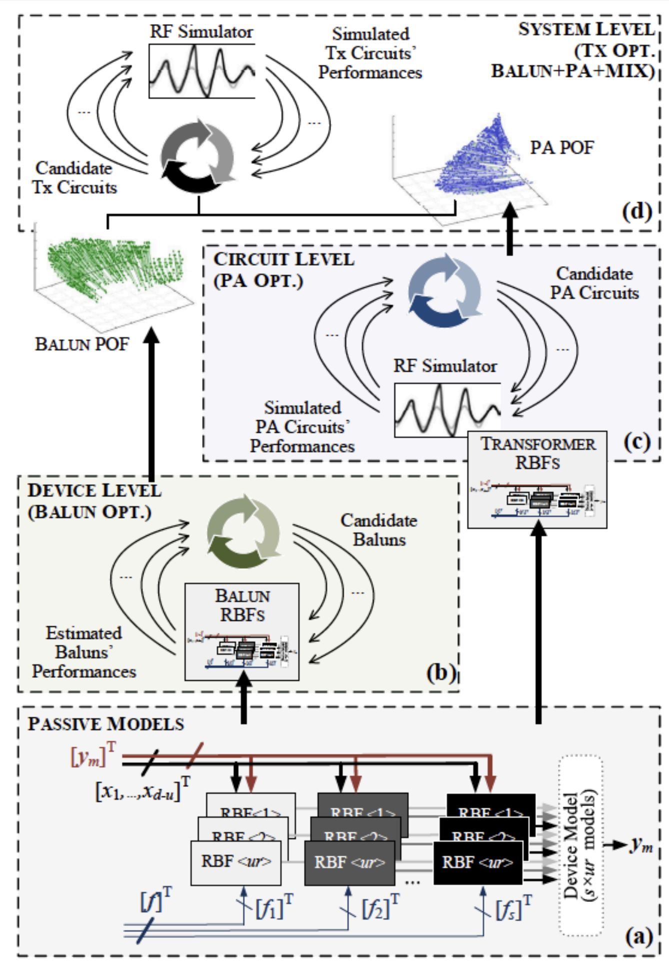


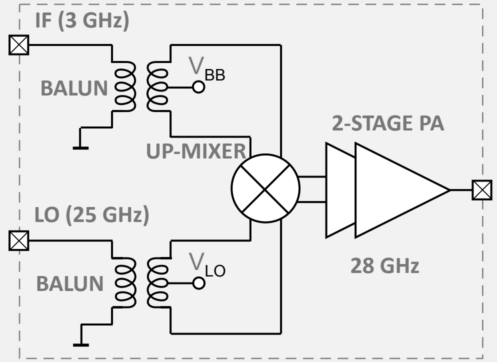


- passive component level: baluns

EXPERIMENTAL CASE

- 28GHz mm-Wave transmitter in 65nm CMOS technology

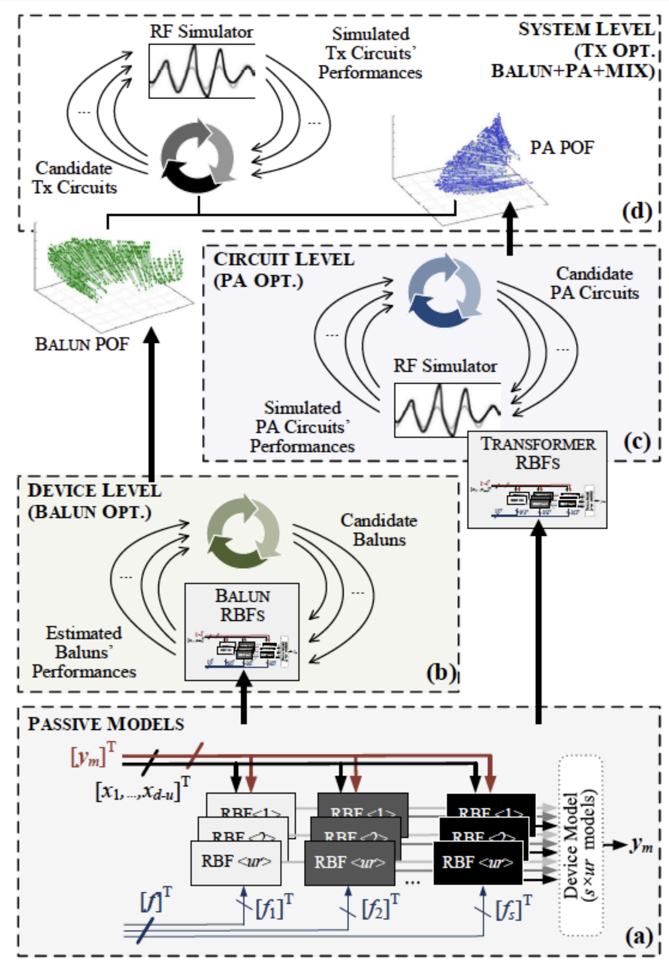


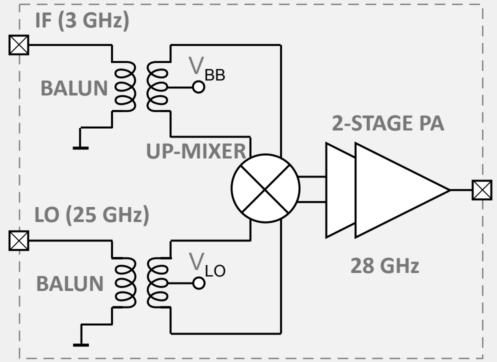


- circuit level: power amplifier (PA)
- passive component level: baluns

EXPERIMENTAL CASE

- 28GHz mm-Wave transmitter in 65nm CMOS technology

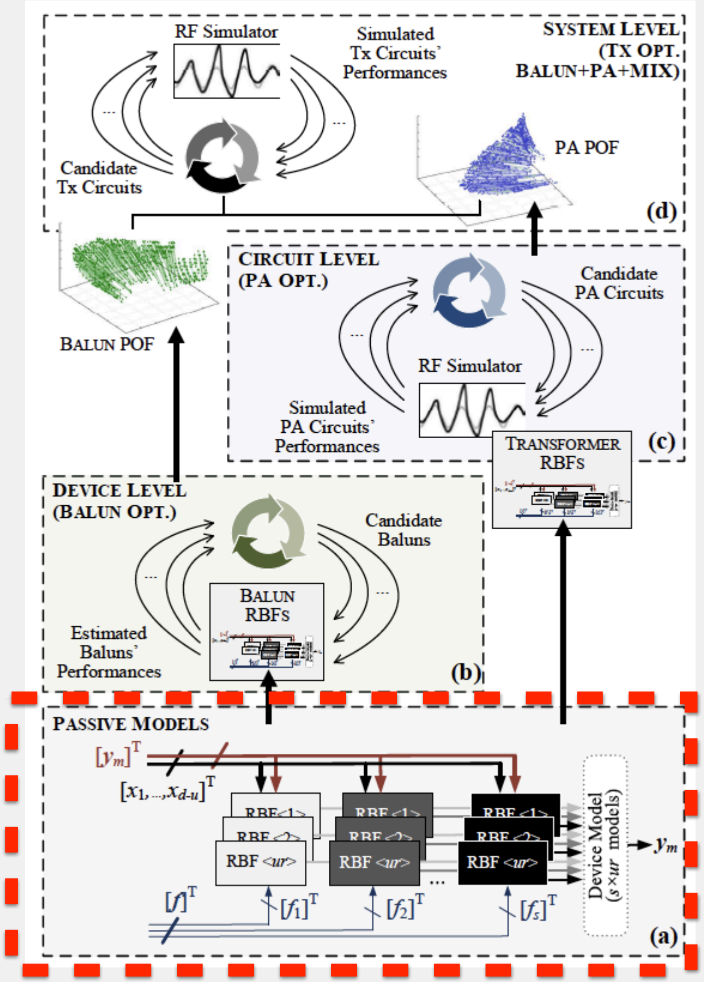




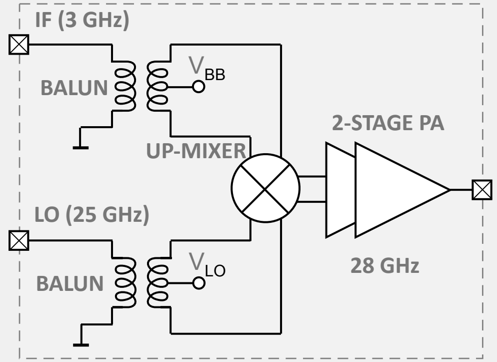
- system level optimization: complete transmitter (with mixer)
- circuit level: power amplifier (PA)
- passive component level: baluns

EXPERIMENTAL CASE

- 28GHz mm-Wave transmitter in 65nm CMOS technology



- system level optimization: complete transmitter (with mixer)



- circuit level: power amplifier (PA)
- passive component level: baluns
- Custom passive component models for transformers and baluns

03

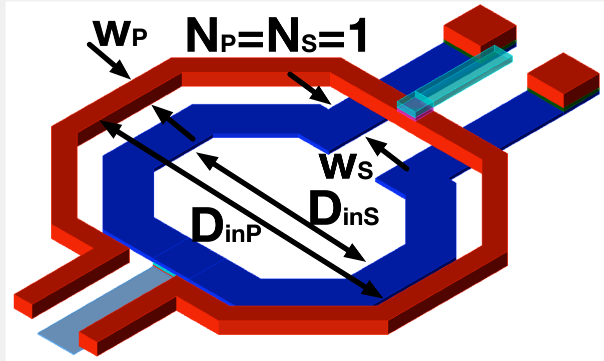
MODELING PASSIVE COMPONENTS

WHY?

- Transformers/baluns are highly used in RF/mm-Wave circuits
- Foundry’s usually do not provide models for transformers (when they do, they are not valid over 20/30GHz)
- EM simulations are time-consuming and integrating an EM simulator in optimization-based methodologies is time-prohibitive
- Therefore, there is a need for an efficient and accurate model
- Machine learning techniques have been applied successfully to the modeling of passive structures and they are proven themselves a valuable candidate solution

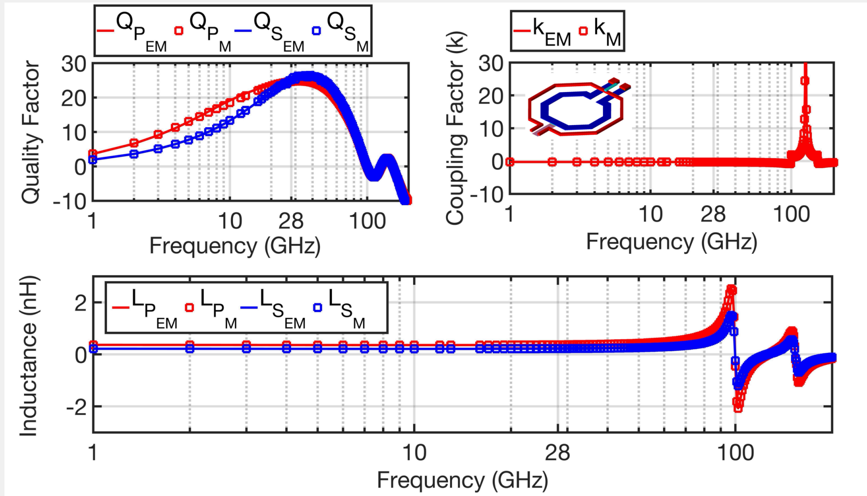
MODELING PARAMETERS

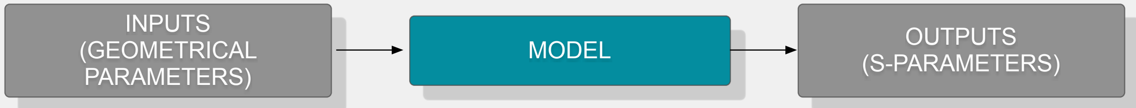
- Transformer design parameters and performances



- Design parameters
  - Number of turns of the primary (Np) and secondary (Ns) coils, their inner diameters (DinP and DinS), and their turn widths (Wp and Ws).

- Performances parameters
  - S-Parameters
  - Inductance (L) and quality factor (Q) of the primary and secondary
  - coupling factor (k)
  - SRF

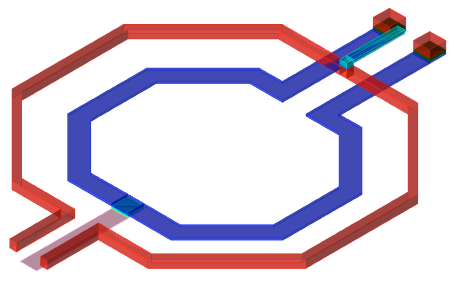




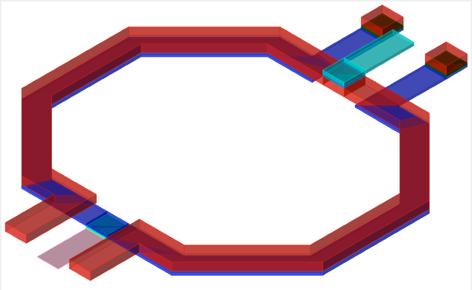
MODEL VALIDATION (EM SIM)

- Radial Basis Functions based-model with an intelligent modeling strategy
- Two types of models were built: one for transformers and another for baluns (stacked transformers)

TRANSFORMERS



BALUNS



- 1500 transformers for training and 100 for test
- 200 baluns for training and 50 for test

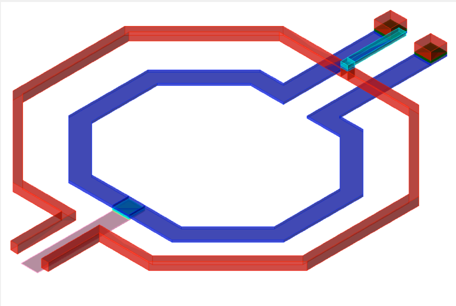
Model	Mean Square Error (%)				
	Lp	Qp	Ls	Qs	k
Transformer	0.14	1.54	0.11	1.93	0.17
Balun	0.15	2.09	0.12	1.57	0.26

[1] F. Passos *et al.*, "Machine Learning Approaches for Transformer Modeling,", *SMACD*, 2022

MODEL VALIDATION (MEAS.)

- Radial Basis Functions based-model with an intelligent modeling strategy
- Two types of models were built: one for transformers and another for baluns (stacked transformers)

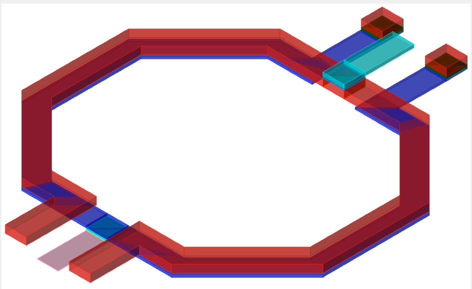
TRANSFORMERS

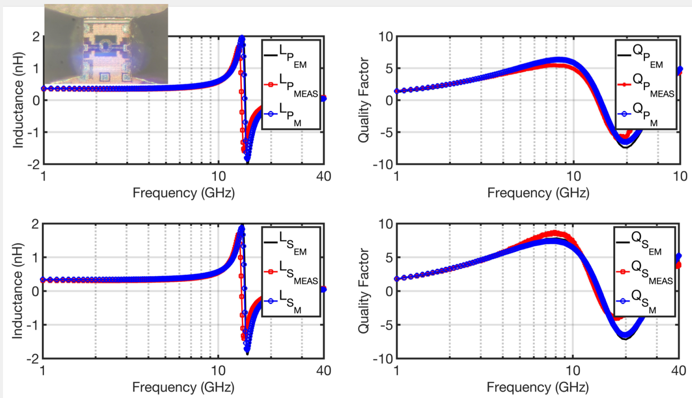


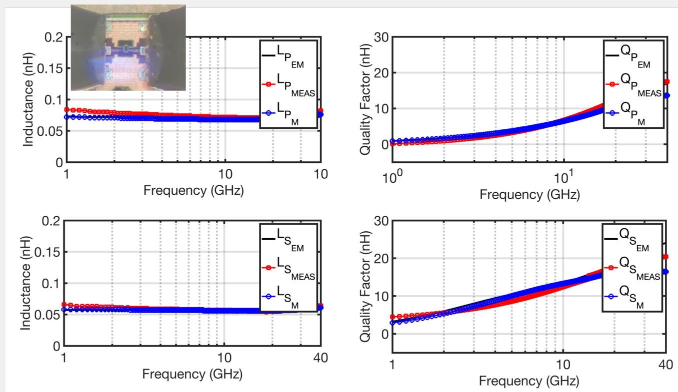
- 1500 transformers for training and 100 for test
- 200 baluns for training and 50 for test

Model	Mean Square Error (%)				
	Lp	Qp	Ls	Qs	k
Transformer	0.14	1.54	0.11	1.93	0.17
Balun	0.15	2.09	0.12	1.57	0.26

BALUNS



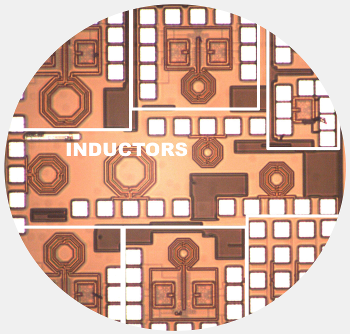




[1] F. Passos *et al.*, "Machine Learning Approaches for Transformer Modeling,", *SMACD*, 2022

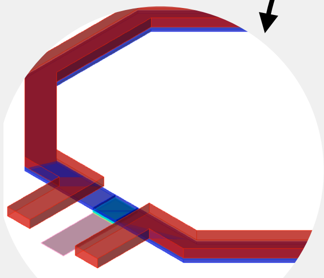
MODEL APPLICATIONS

Usage of the model as a normal PDK model inside a design framework

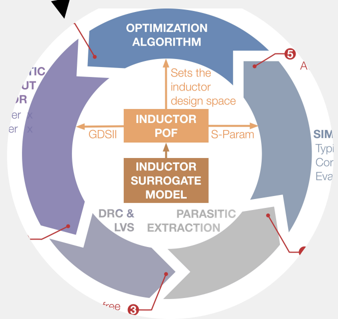


RF/MM-WAVE DESIGN

Circuit/passive component optimization using evolutionary algorithms



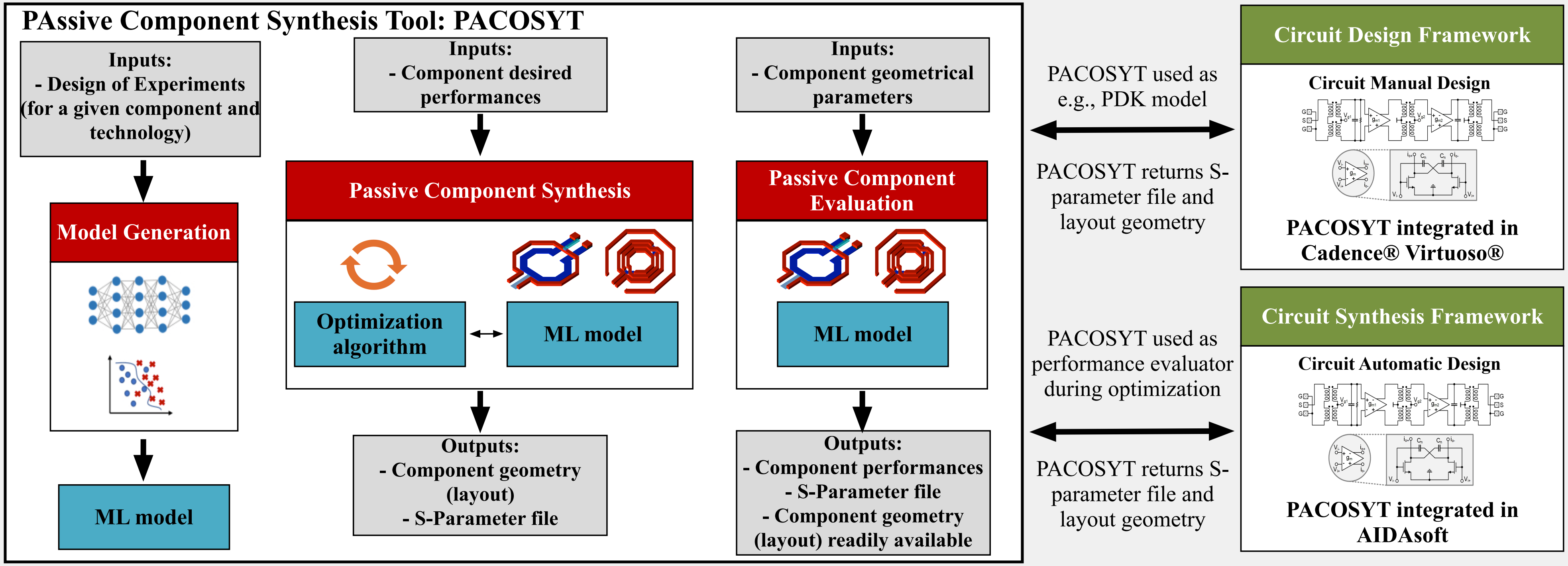
USAGE AS 'PDK' MODEL



USAGE IN OPTIMIZATION

PASSIVE COMPONENT SYNTHESIS TOOL: PACOSYT

- A tool (PACOSYT) was created to ease the model usage either as a PDK or in optimization



★ **Being tested in industrial environment**

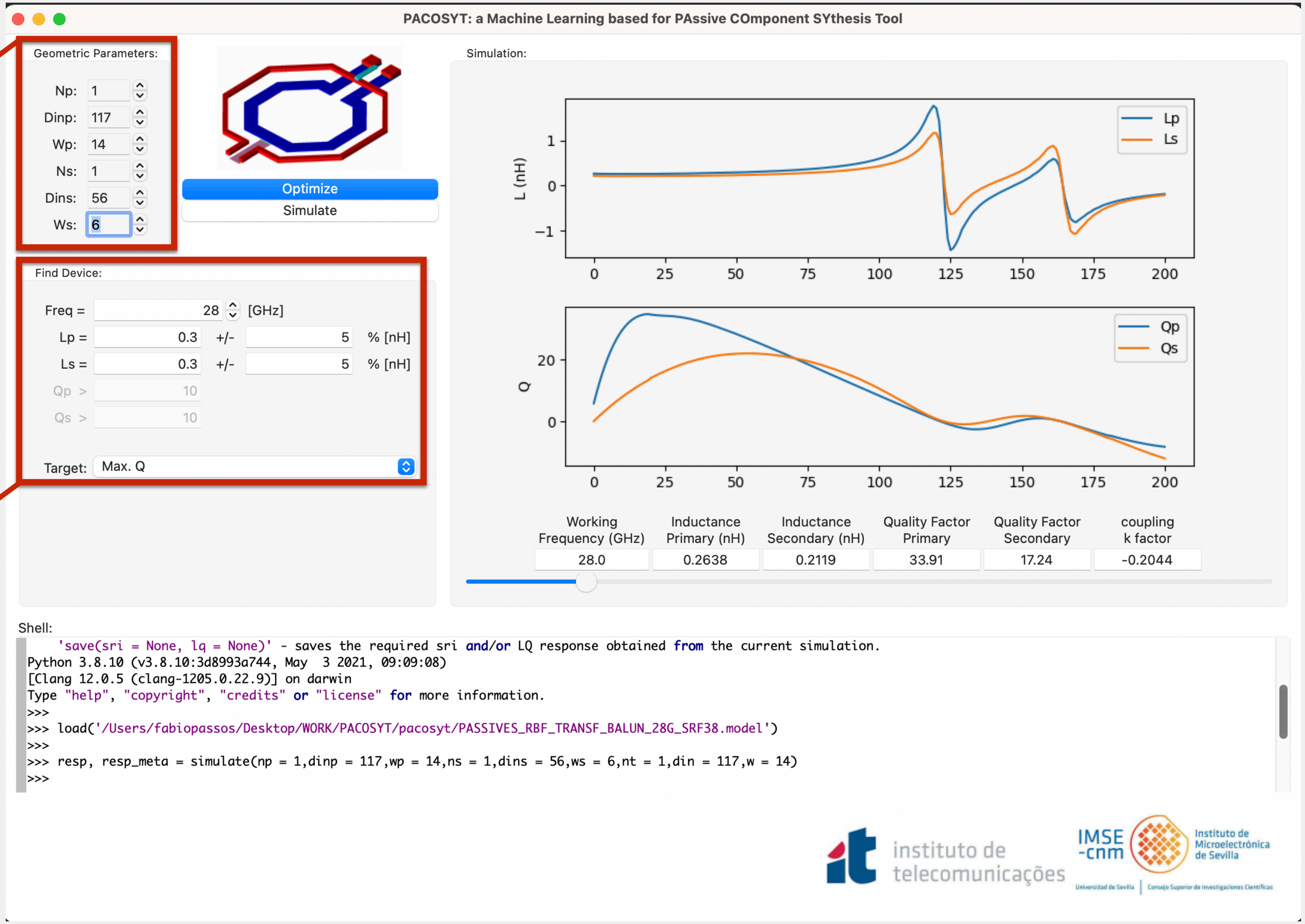
PACOSYT GUI

TRANSFORMER SIMULATION (USAGE AS 'PDK' MODEL)

Select transformer parameters and see the performances

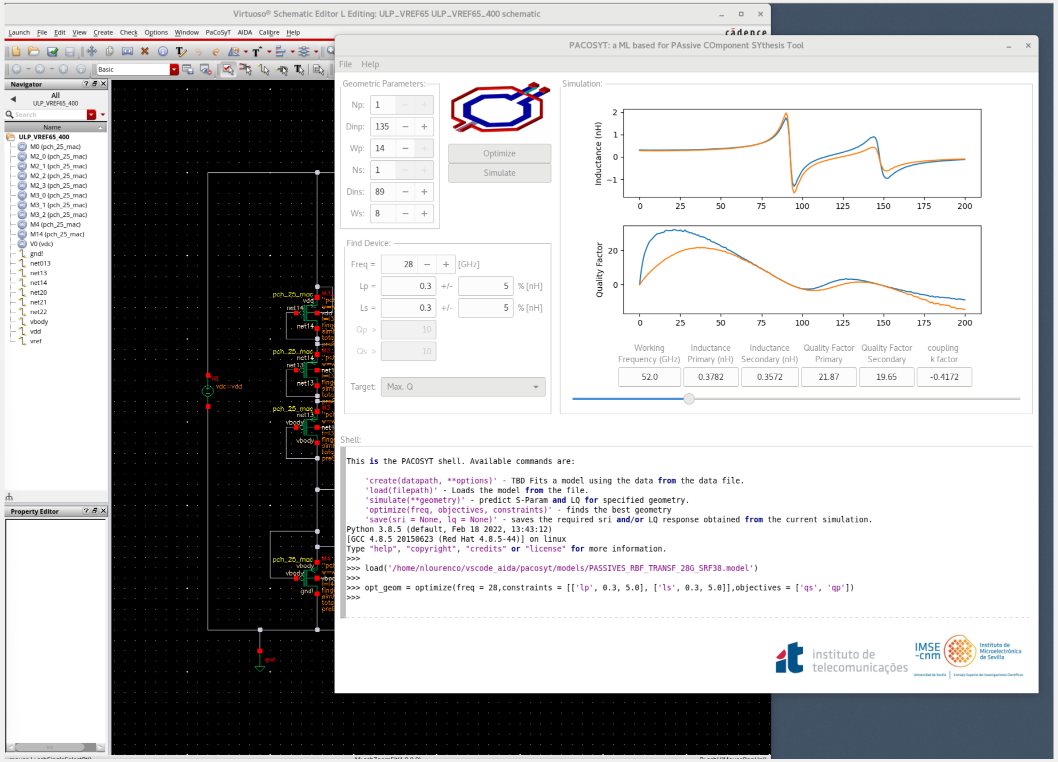
TRANSFORMER OPTIMIZATION

Select the desired transformer performances and get the geometry



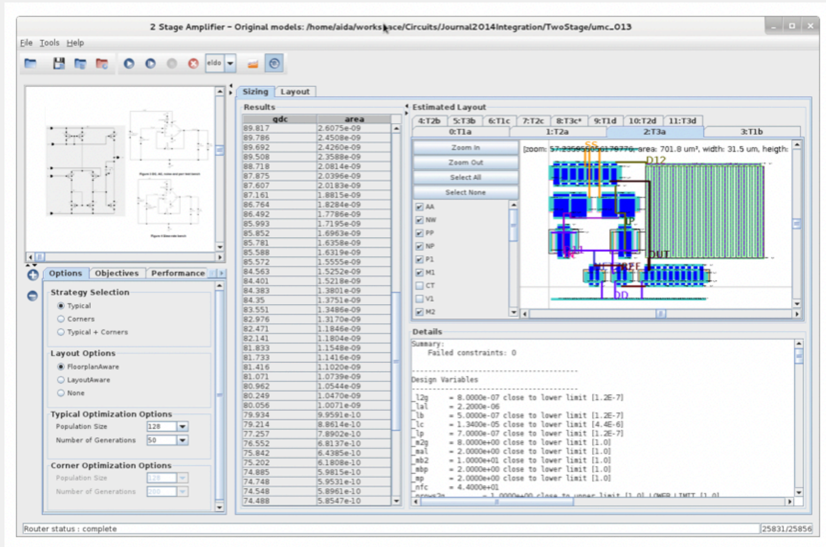
PACOSYT USABILITY

- Integrated in Cadence® Virtuoso® for usage as PDK and “inductor finder”



- Integrated in AIDASoft for circuit optimization

http://www.aidasoft.com/Home



[2] F. Passos *et al.*, "PACOSYT: A Passive Component Synthesis Tool Based on Machine Learning and Tailored Modeling Strategies Towards Optimal RF and mm-Wave Circuit Designs,", *IEEE Journal of Microwaves*, 2023

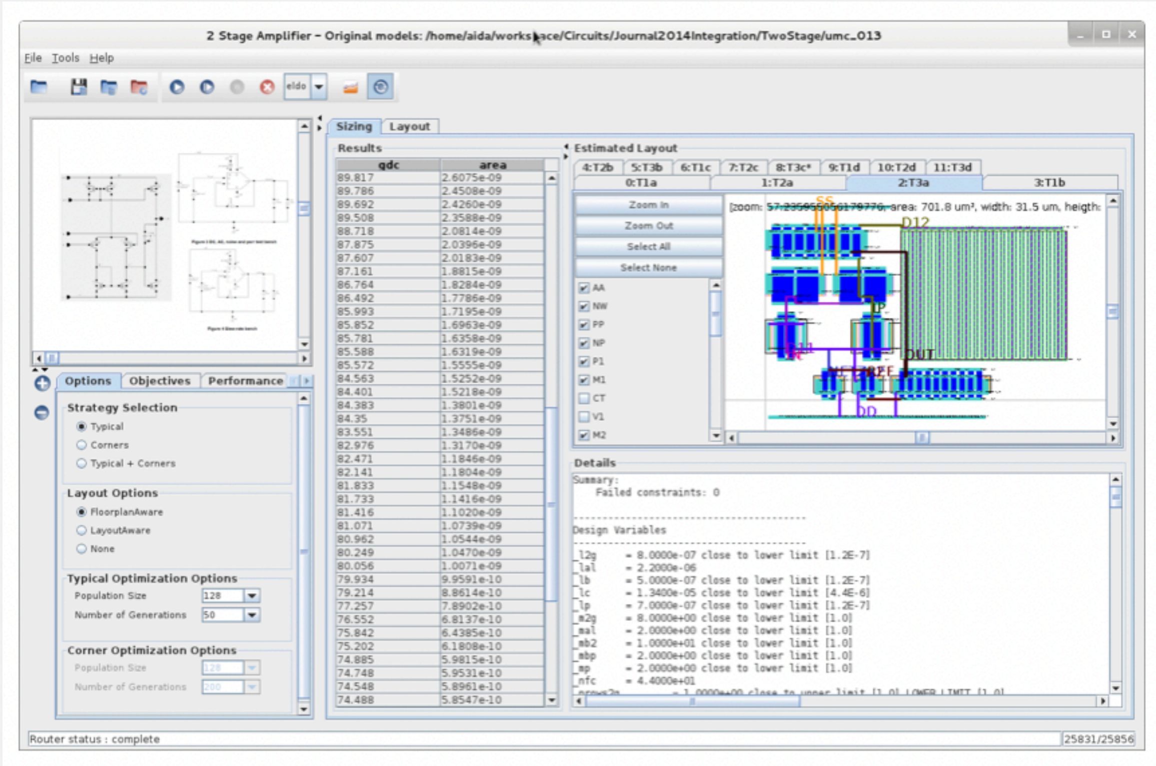
04

EXPERIMENTAL RESULTS

IN HOUSE TOOL: AIDASOFT

- In-house tool developed to optimize circuits
- AIDA uses NSGA-II evolutionary algorithm for circuit optimization
- PACOSYT is integrated and used to create the S-parameter description of passives

http://www.aidasoft.com/Home



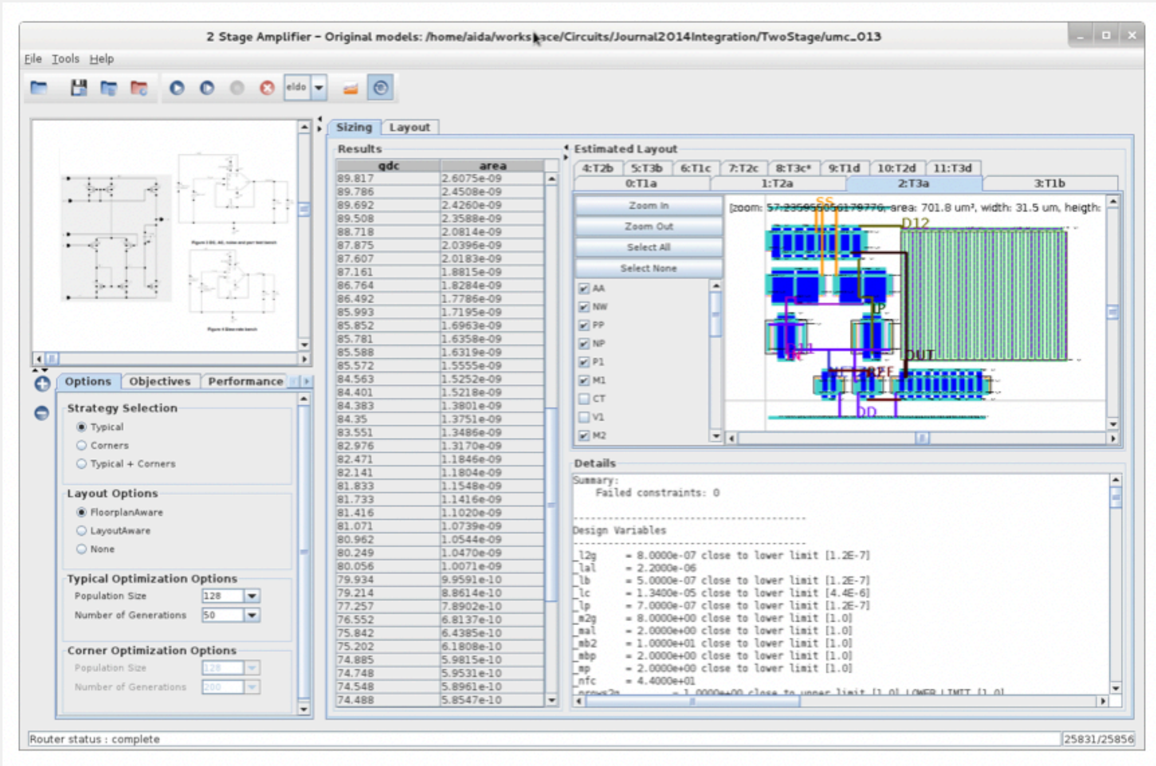
IN HOUSE TOOL: AIDASOFT

- In-house tool developed to optimize circuits
- AIDA uses NSGA-II evolutionary algorithm for circuit optimization
- PACOSYT is integrated and used to create the S-parameter description of passives

AIDAsoft Analog IC Design Automation

http://www.aidasoft.com/Home

- Tackles PVT variations
- Yield-aware optimization
- Layout-aware optimization



IN HOUSE TOOL: AIDASOFT

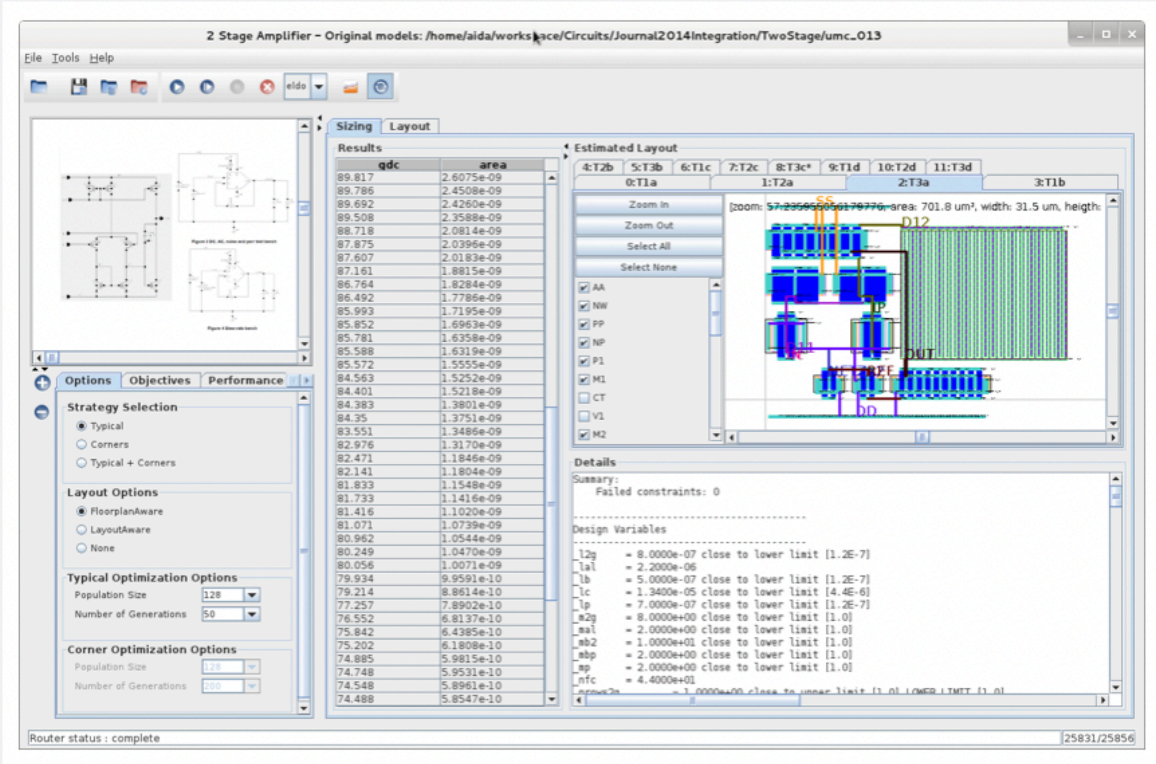
- In-house tool developed to optimize circuits
- AIDA uses NSGA-II evolutionary algorithm for circuit optimization
- PACOSYT is integrated and used to create the S-parameter description of passives

http://www.aidasoft.com/Home

- Tackles PVT variations
- Yield-aware optimization
- Layout-aware optimization

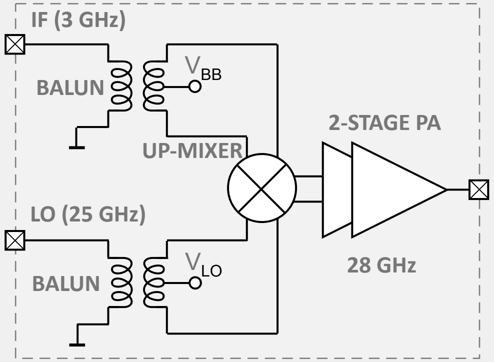
- All tested in Analog/RF circuits
- Currently being extended into mm-Wave and system-level designs

★ **Being tested in industrial environment**

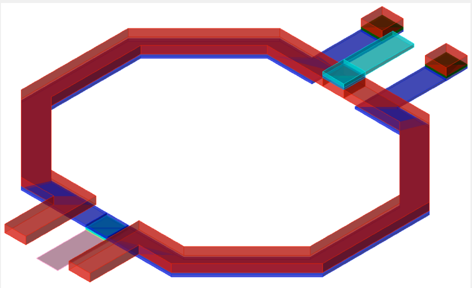


PAPER CASE STUDY

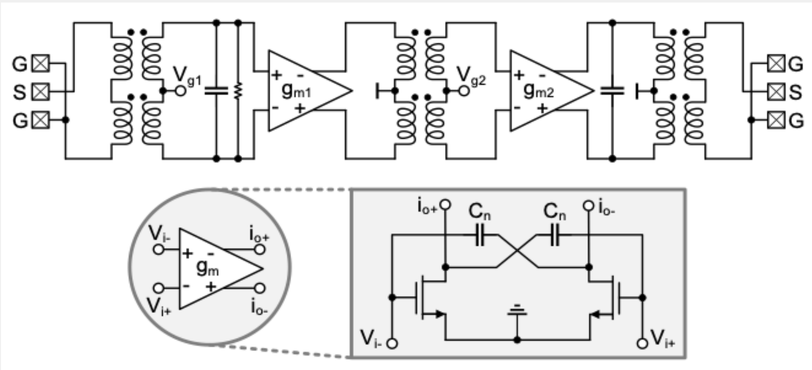
- Transmitter optimization in 65nm technology operating at 26~30GHz with a Vdd=1.2V



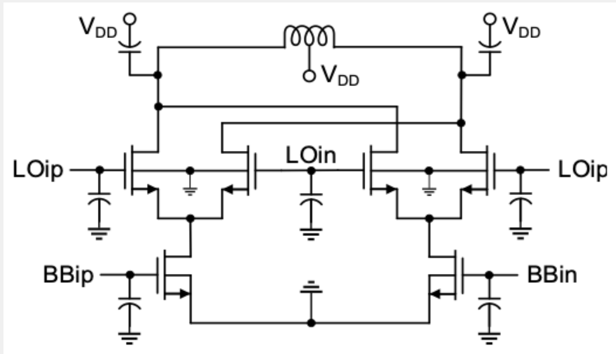
Baluns



Power Amplifier



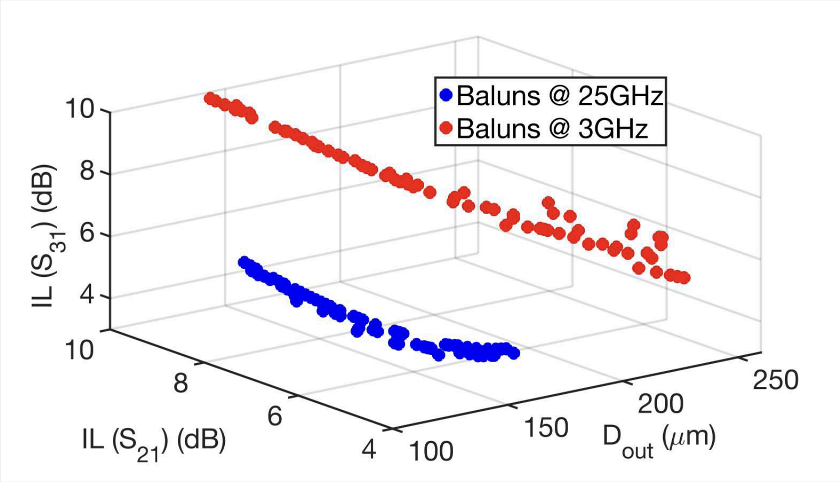
Up-Conversion Mixer



PASSIVE LEVEL SYNTHESIS

Balun Performance	Balun Specifications
Amplitude imbalance	< 1 dB
Phase Imbalance	< 10º
Insertion Loss (S_{21})	Minimize
Insertion Loss (S_{21})	Minimize
Area	Minimize

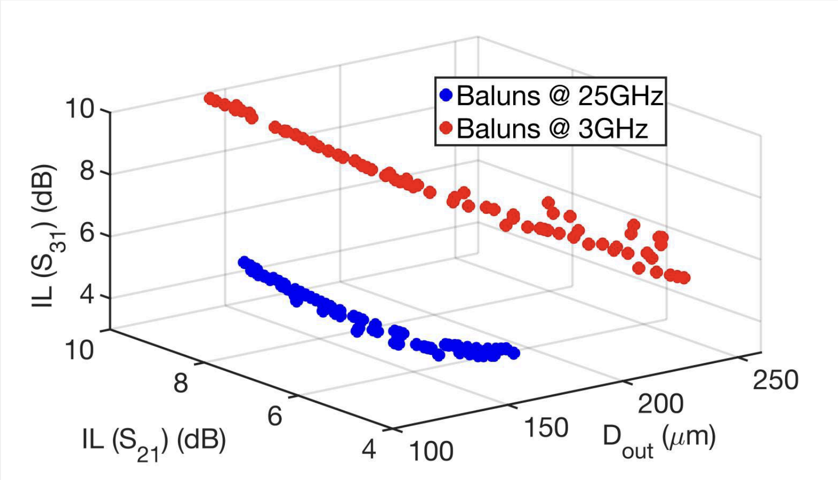
- Two optimizations performed with 64 individuals and 50 generations
- Optimization lasted 4m



PASSIVE LEVEL SYNTHESIS

Balun Performance	Balun Specifications
Amplitude imbalance	< 1 dB
Phase Imbalance	< 10º
Insertion Loss (S_{21})	Minimize
Insertion Loss (S_{21})	Minimize
Area	Minimize

- Two optimizations performed with 64 individuals and 50 generations
- Optimization lasted 4m



- 3,200 transformers evaluated
- If performed with EM simulation it would last approx. 11 days (average of 5 minutes per EM simulation)

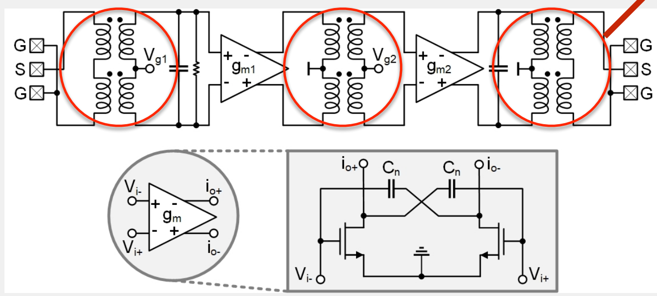
- **Better efficiency using a model !**

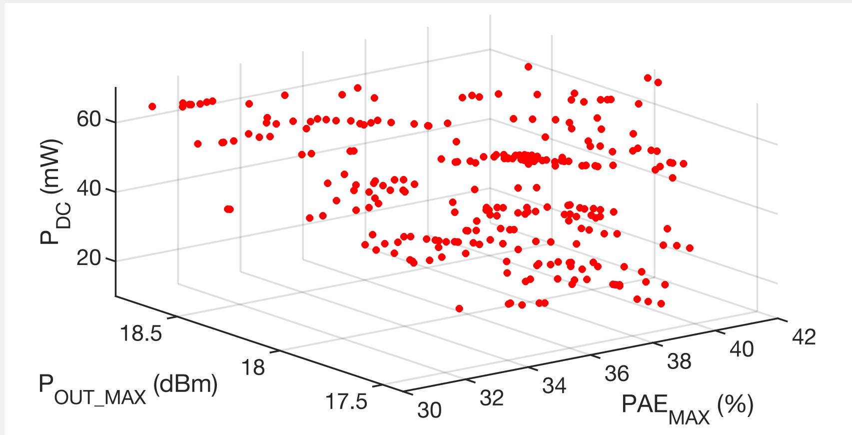
CIRCUIT LEVEL SYNTHESIS

PA Performance	PA Specifications
S_{11} @ 26.5-30 GHz	< -12 dB
S_{22} @ 26.5-30 GHz	< -5 dB
S_{21} @ 26.5-30 GHz	> 12 dB
S_{21} Variation (@ 26.5-30 GHz)	< 1.7dB
***Rollet Stb Factor* @ 1Hz-120GHz**	> 1
P_{DC}	Minimize (< 70 mW)
P_{OUT_MAX}	Maximize (> 8 dBm)
PAE_{MAX}	Maximize (> 20%)
Power $Gain_{MAX}$	> 12 dB
OP1dB	> 10 dBm

- Optimization performed with 400 individuals and 150 generations
- Optimization lasted ~42h

evaluated with the model





CIRCUIT LEVEL SYNTHESIS

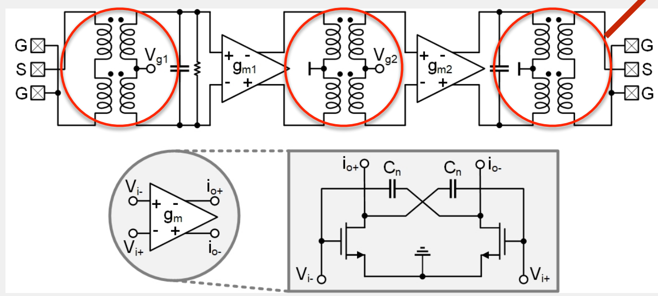
PA Performance	PA Specifications
***S*₁₁ @ 26.5-30 GHz**	< -12 dB
***S*₂₂ @ 26.5-30 GHz**	< -5 dB
***S*₂₁ @ 26.5-30 GHz**	> 12 dB
***S*₂₁ Variation (@ 26.5-30 GHz)**	< 1.7dB
***Rollet Stb Factor* @ 1Hz-120GHz**	> 1
P_{DC}	Minimize (< 70 mW)
P_{OUT_MAX}	Maximize (> 8 dBm)
PAE_{MAX}	Maximize (> 20%)
Power $Gain_{MAX}$	> 12 dB
OP1dB	> 10 dBm

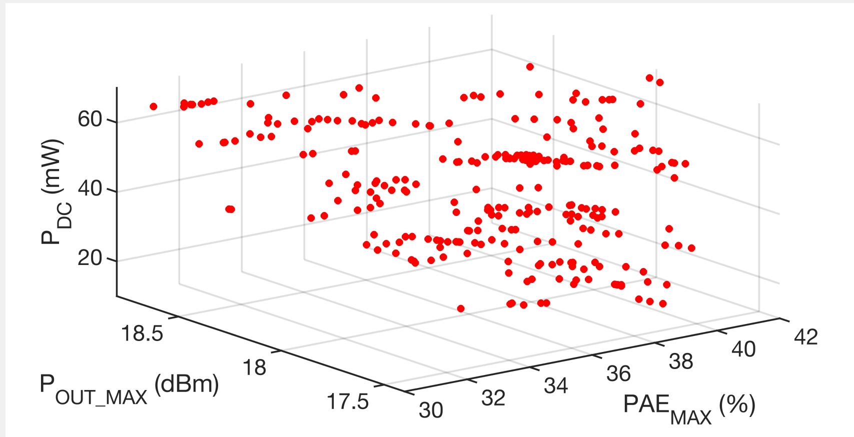
- Optimization performed with 400 individuals and 150 generations
- Optimization lasted ~42h

- 180,000 transformers evaluated
- If performed with EM simulation it would last approx. 2 years (average of 5 minutes per EM simulation)

- **Only possible using a model !!!!**

evaluated with the model

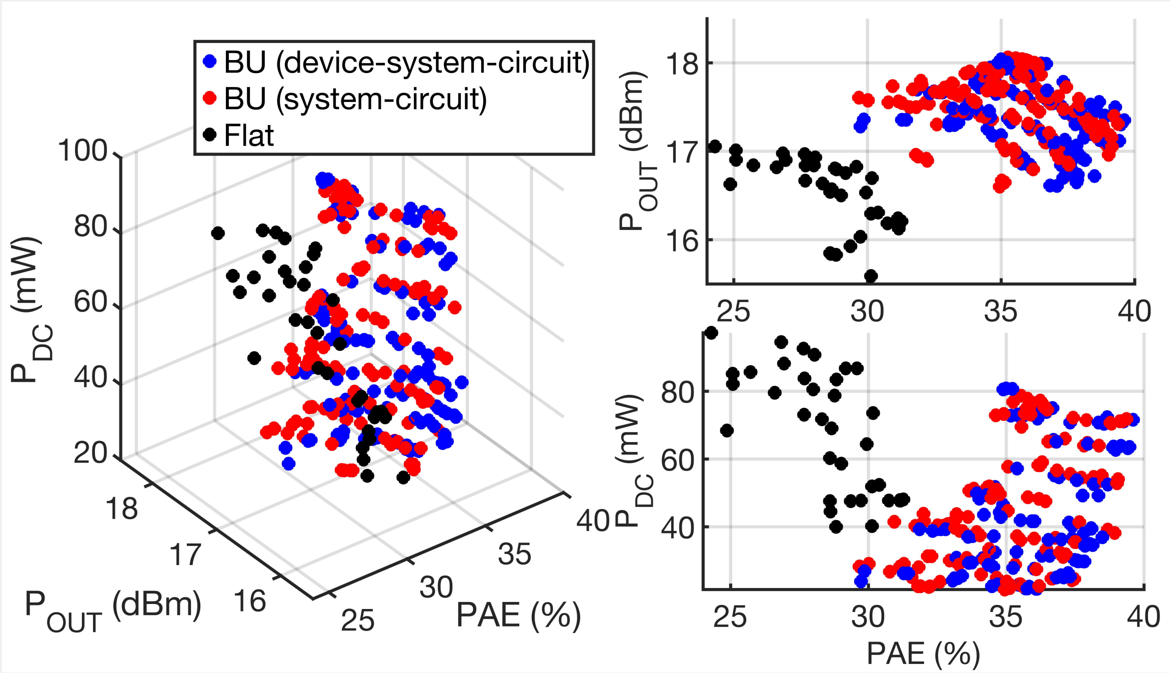




SYSTEM LEVEL SYNTHESIS

Tx Performance	Tx Specifications
Conversion Gain	> 20 dB
P_{DC}	Minimize (< 100 mW)
P_{OUT_MAX}	Maximize (> 8 dBm)
PAE_{MAX}	Maximize (> 20%)
Power Gain	> 12 dB
OP1dB	> 2.5 dBm

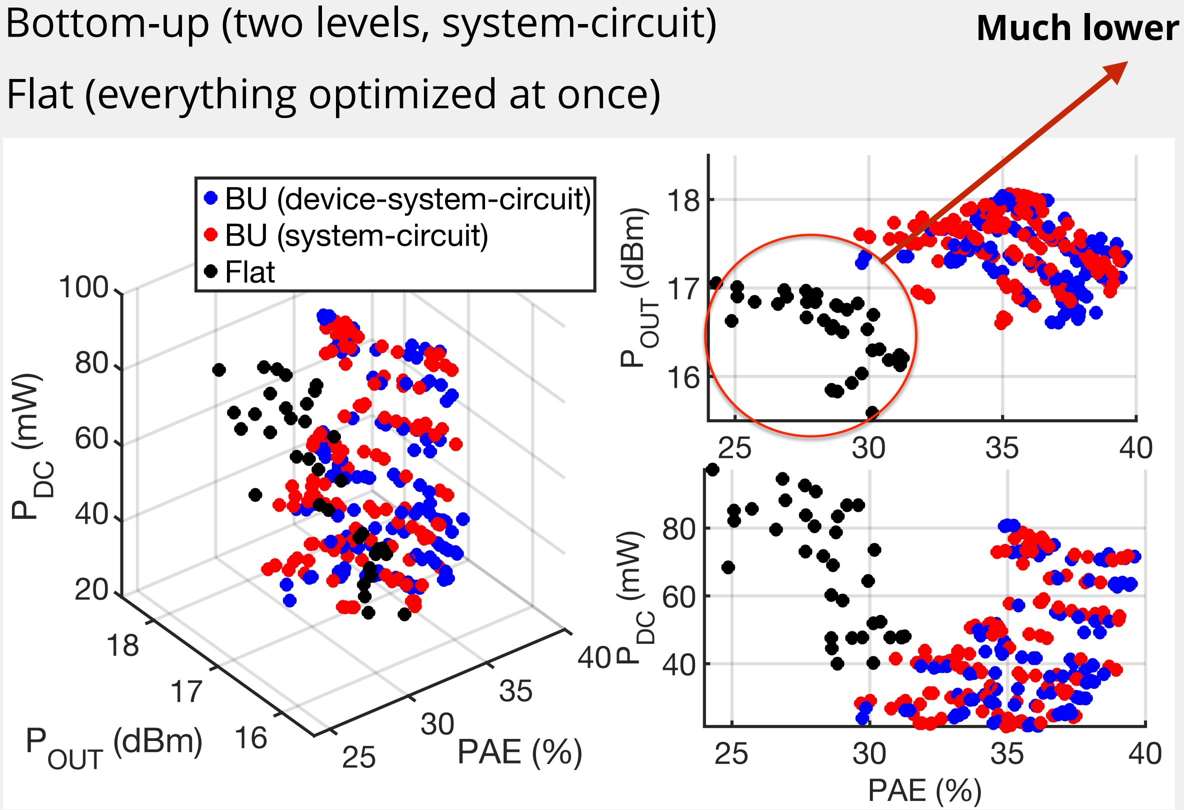
- Three different optimization methodologies:
  1. Bottom-up (three leves, device-circuit-system)
  2. Bottom-up (two levels, system-circuit)
  3. Flat (everything optimized at once)



SYSTEM LEVEL SYNTHESIS

Tx Performance	Tx Specifications
Conversion Gain	> 20 dB
P_{DC}	Minimize (< 100 mW)
P_{OUT_MAX}	Maximize (> 8 dBm)
PAE_{MAX}	Maximize (> 20%)
Power Gain	> 12 dB
OP1dB	> 2.5 dBm

- Three different optimization methodologies:
  1. Bottom-up (three leves, device-circuit-system)
  2. Bottom-up (two levels, system-circuit)
  3. Flat (everything optimized at once)

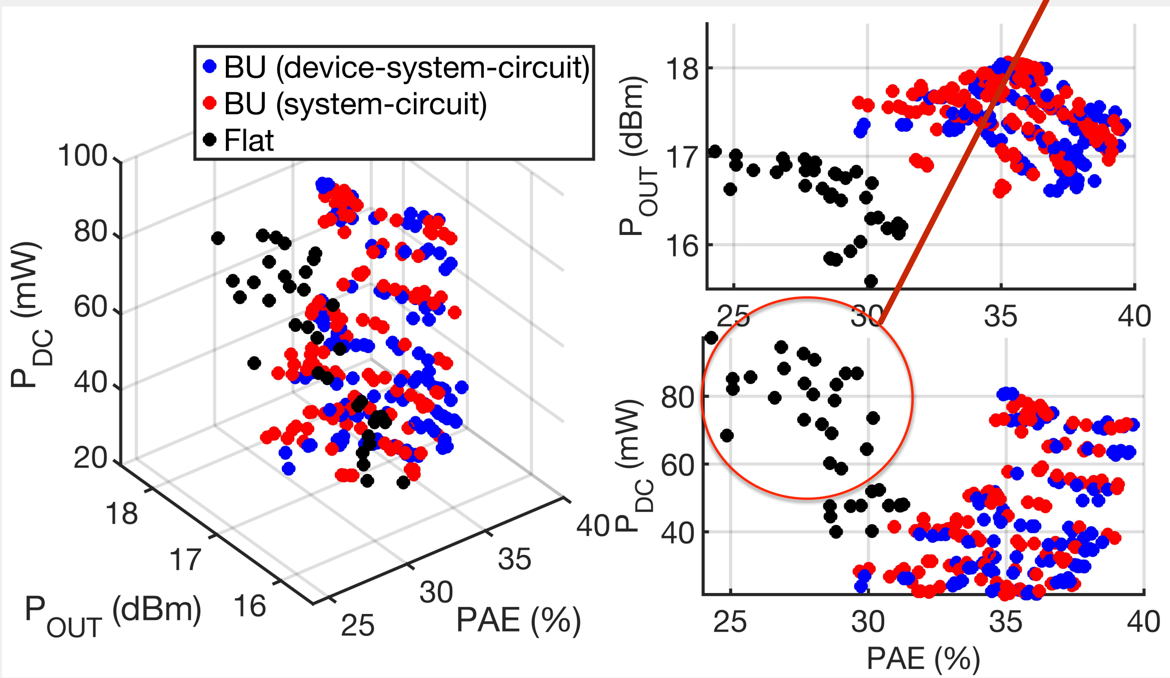


SYSTEM LEVEL SYNTHESIS

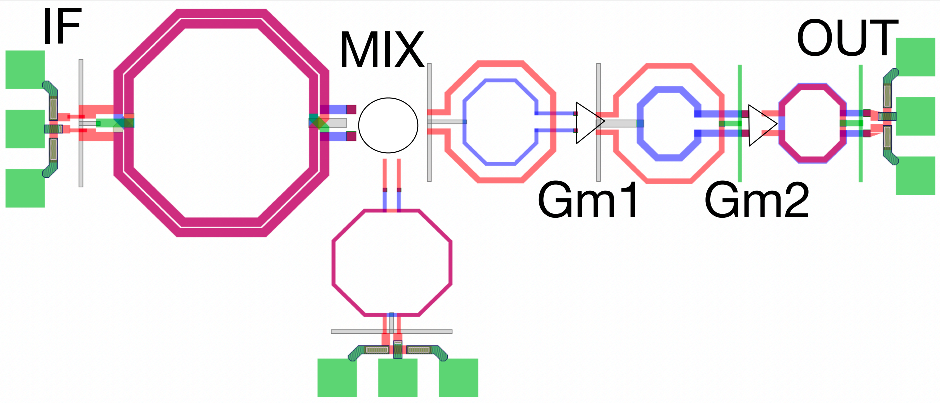
Tx Performance	Tx Specifications
Conversion Gain	> 20 dB
P_{DC}	Minimize (< 100 mW)
P_{OUT_MAX}	Maximize (> 8 dBm)
PAE_{MAX}	Maximize (> 20%)
Power Gain	> 12 dB
OP1dB	> 2.5 dBm

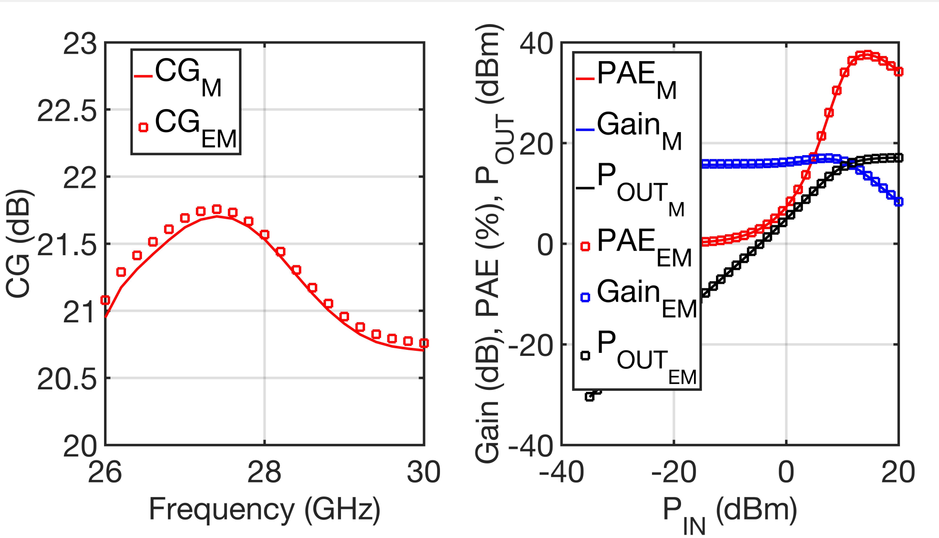
- Three different optimization methodologies:
  1. Bottom-up (three leves, device-circuit-system)
  2. Bottom-up (two levels, system-circuit)
  3. Flat (everything optimized at once)

Much lower PAE and higher P_{DC}



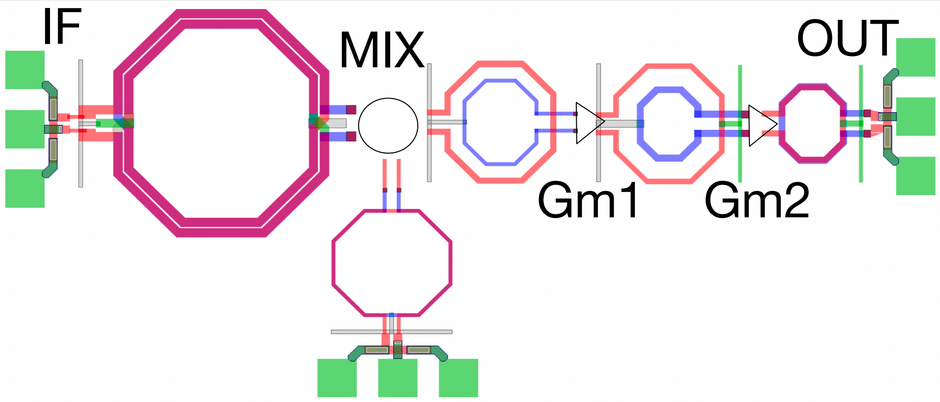
ONE OF THE DESIGNS...

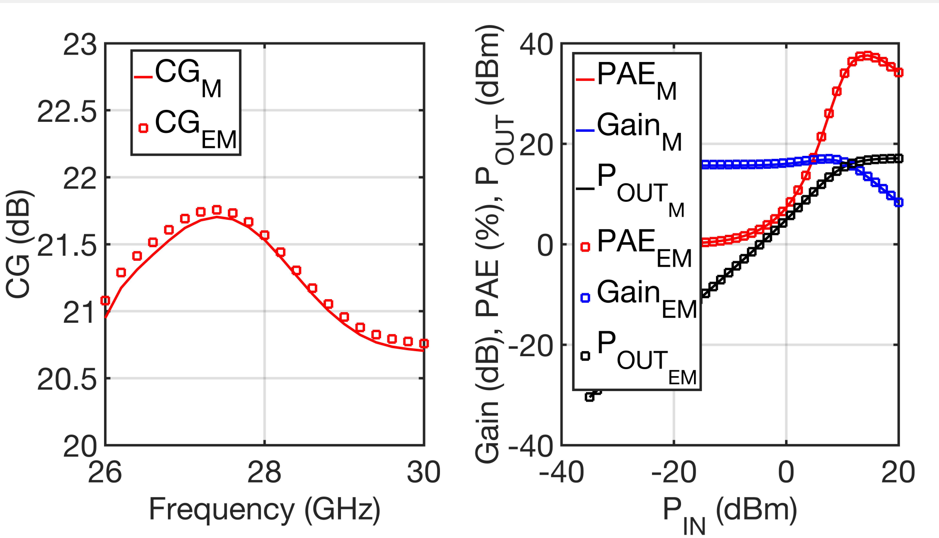




Tx Performance	Tx Performances (model)
Conversion Gain	21.53 dB
P_{DC}	21.27 mW
P_{OUT_MAX}	17.08 dBm
PAE_{MAX}	37.59 %
Power Gain	16.84 dB
OP1dB	16.44 dBm

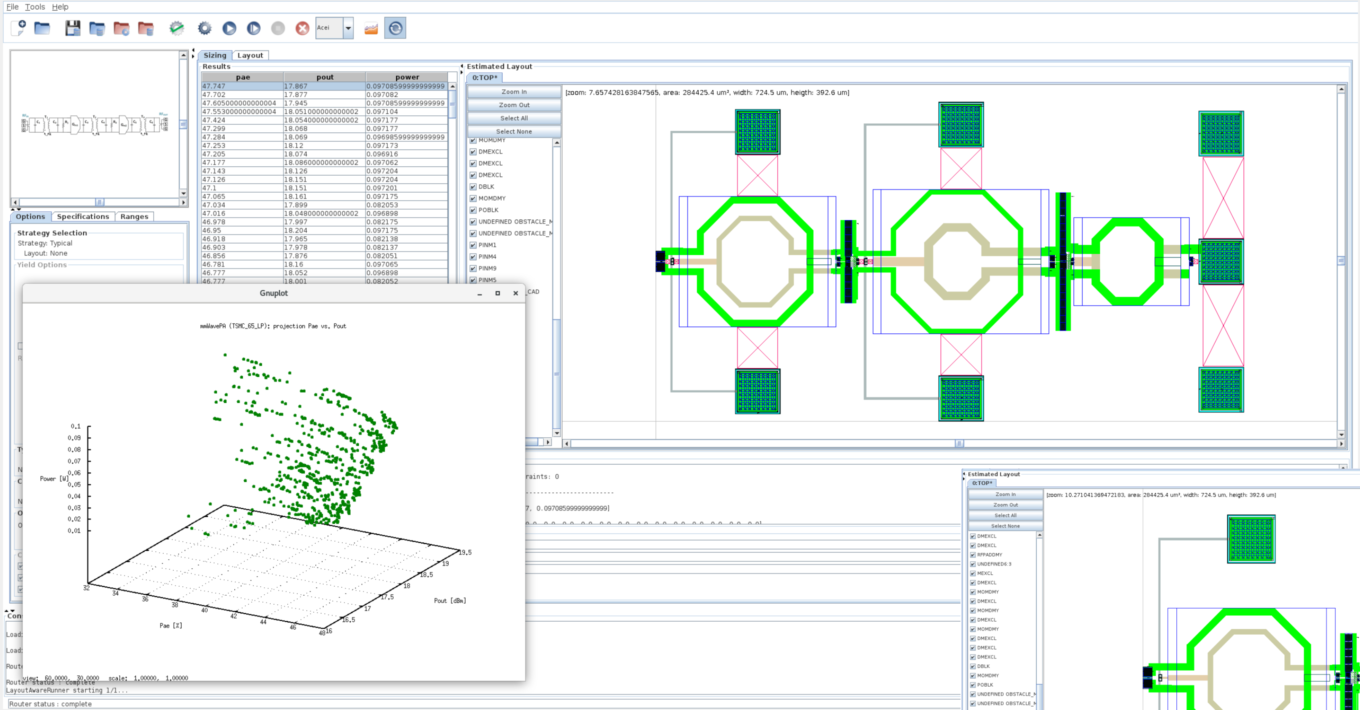
ONE OF THE DESIGNS...



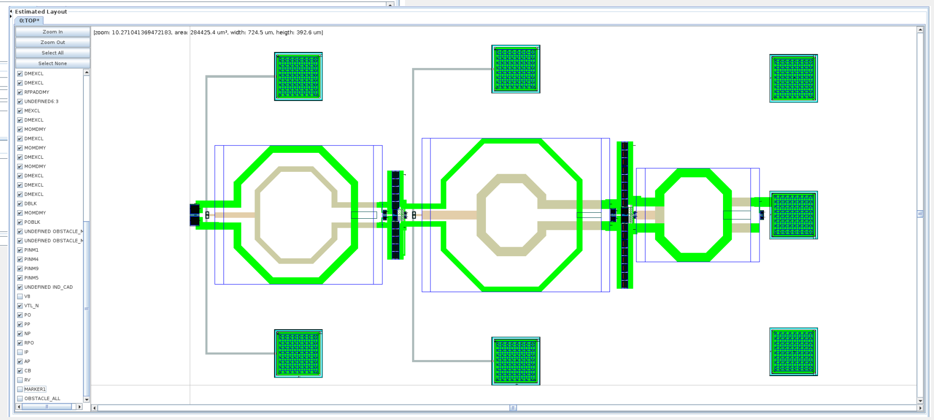


Tx Performance	Tx Performances (model)	Tx Performances (EM sim)	Error (%)
Conversion Gain	21.53 dB	21.57 dB	0.0019
P_{DC}	21.27 mW	21.27 mW	-
P_{OUT_MAX}	17.08 dBm	17.06 mW	0.0012
PAE_{MAX}	37.59 %	37.55 %	0.0011
Power Gain	16.84 dB	17.07 dB	0.0106
OP1dB	16.44 dBm	16.39 dBm	0.0031

FUTURE WORK: PVT AND LAYOUT-AWARE POFs...

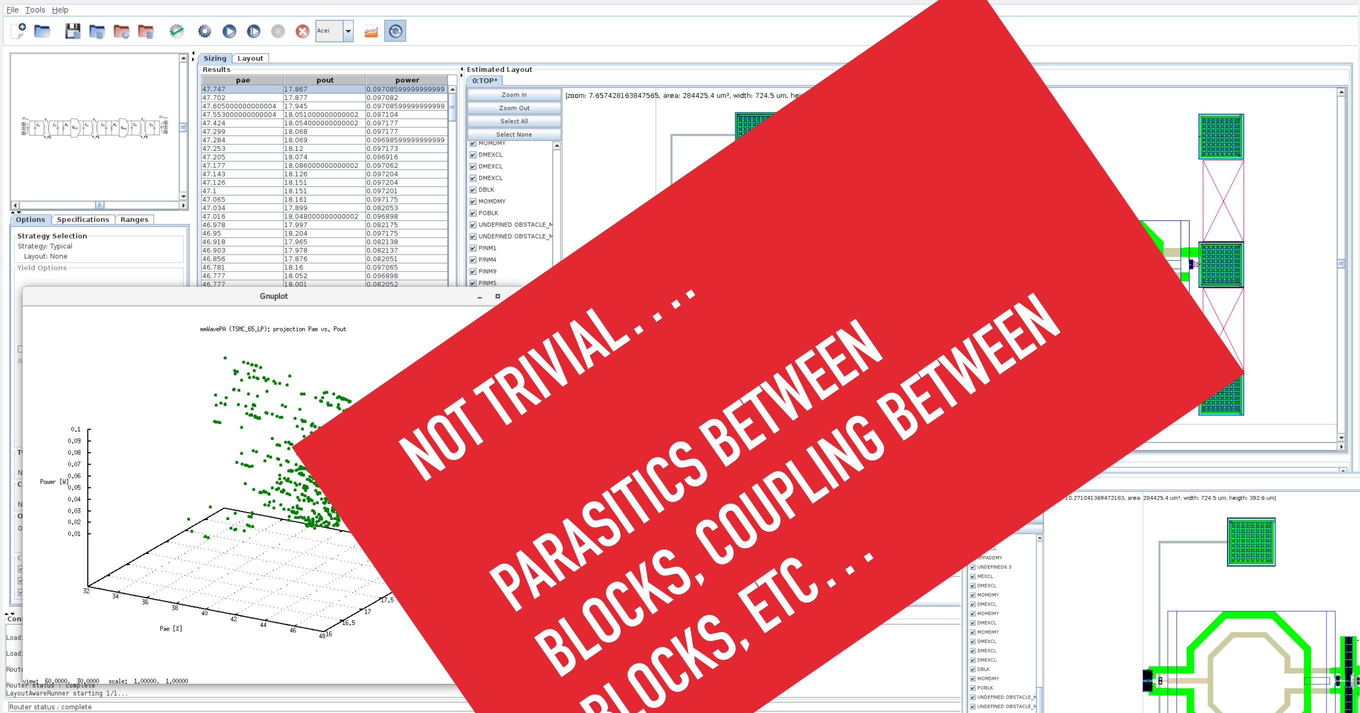


Automatic layout generation



Taking into account PVT variations

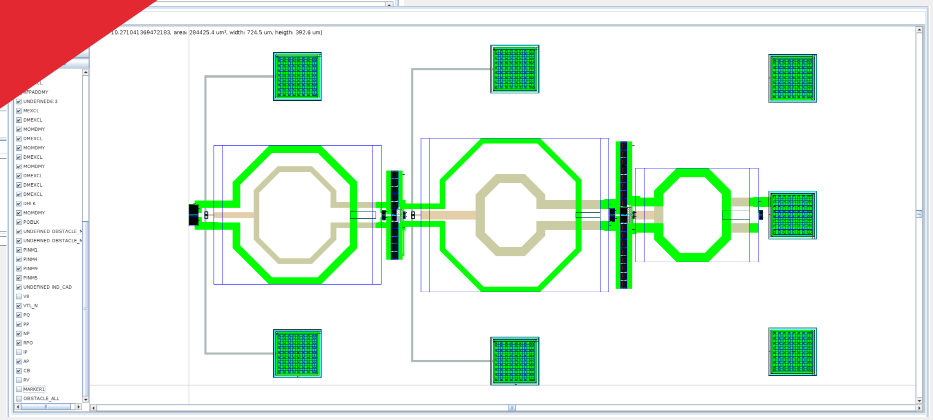
FUTURE WORK: PVT AND LAYOUT-AWARE POFs…



NOT TRIVIAL….

PARASITICS BETWEEN BLOCKS, COUPLING BETWEEN BLOCKS, ETC…

Automatic layout generation



Taking into a[illegible]ount PVT variations

CONCLUSIONS

01
BOTTOM-UP STRATEGY WAS APPLIED TO THE DESIGN OF A TRANSMITTER
Baluns optimized at lower level, then the PA at circuit level and than the MIX at system level

02
BALUNS AND TRANSFORMERS SYNTHESIZED USING ML MODEL
The model allows for optimal passive component design in minutes

03
HUNDREDS OF CIRCUITS SYNTHESIZED IN DAYS RATHER THAN WEEKS/MONTHS
Huge improvement in efficiency

04
IN THE FUTURE OPTIMIZE CIRCUITS TAKING INTO ACCOUNT PVT VARIATIONS AND LAYOUT
Enabling a fully sizing-layout automated methodology

I invite you all to submit works to...

2023 SMACD Conference

WWW.SMACD-CONFERENCE.ORG

Topical Collection in ELECTRONICS MDPI

THANK YOU!

FABIO.PASSOS@LX.IT.PT

instituto de telecomunicações

DEEC
DEPARTAMENTO DE ENGENHARIA ELETROTÉCNICA E DE COMPUTADORES
TÉCNICO LISBOA

ASIA SOUTH PACIFIC DAC DESIGN AUTOMATION CONFERENCE

ML TECHNIQUES

- All implemented/tested using Python libraries

GAUSSIAN PROCESS REGRESSION

- Near parameterless technique
- internal optimization which defines its parameters

IN THE PAPER

RADIAL BASIS FUNCTION

- Simpler than GPR and therefore require less memory

IN THE PAPER

NEAREST NEIGHBOR

- Simplest technique available (serves as baseline for the others)

IN THE PAPER

KERNEL RIDGE REGRESSION

- Similar to GPR but without the internal optimization

TESTED AFTERWARDS

RANDOM FOREST REGRESSION

- Simple model which may be useful to identify multiple trends in the data

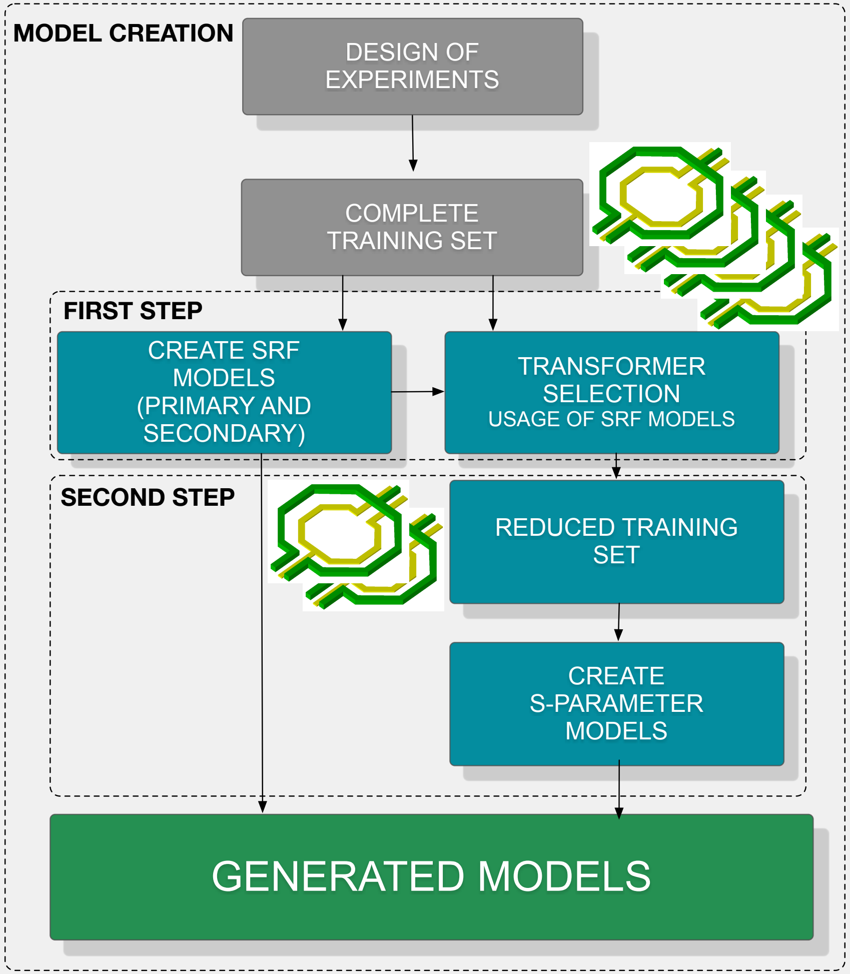
TESTED AFTERWARDS

ARTIFICIAL NEURAL NETWORKS

- Good for big data sets and high number of variables

TESTED AFTERWARDS

MODEL STRATEGY



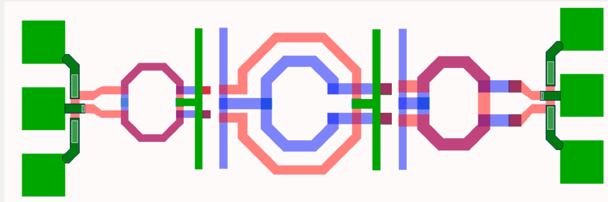
MODEL RESULTS

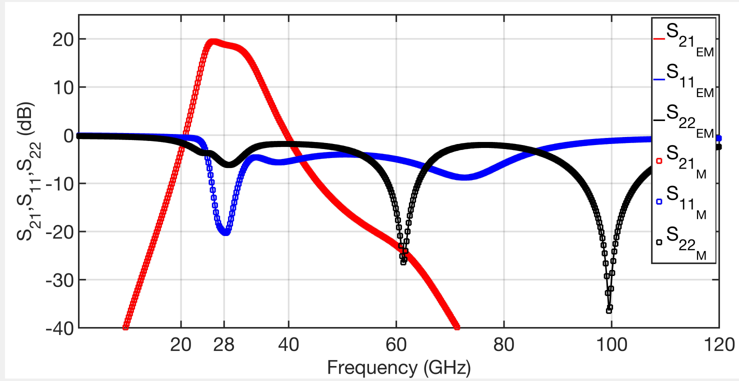
			Technique											
			GPR*		KRR		RBF*		RFR		NN*		ANN	
Frequency	Performance		ME (%)	MAPE (%)	ME (%)	MAPE (%)	ME (%)	MAPE (%)	ME (%)	MAPE (%)	ME (%)	MAPE (%)	ME (%)	MAPE (%)
28GHz	N=1:1*	L_P	0.23	0.12	1.04	0.22	0.35	0.16	14.24	2.47	10.62	3.35	2.30	0.50
		Q_P	3.84	1.38	4.86	1.81	3.77	1.53	22.11	9.14	22.14	4.47	139.36	7.82
		L_S	0.26	0.1	1.03	0.31	0.24	0.08	13.09	4.46	16.44	5.61	2.89	0.65
		Q_S	7.17	1.98	12.32	4.04	2.2	0.78	16.65	7.90	34.18	9.71	30.19	4.05
		k	0.55	0.18	0.81	0.25	0.45	0.21	28.18	6.56	25.38	8.87	5.84	1.08
	N=1:2	L_P	0.57	0.14	0.48	0.15	0.53	0.17	12.03	2.94	11.92	3.88	1.63	0.66
		Q_P	4.59	1.78	5.41	1.84	5.28	1.94	25.51	13.93	27.33	8.39	28.16	5.06
		L_S	0.39	0.16	0.46	0.22	0.53	0.17	15.93	4.84	19.21	7.26	2.74	0.80
		Q_S	4.73	1.21	3.53	1.48	4.55	1.49	16.64	7.93	19.95	5.24	18.91	4.31
		k	0.77	0.25	1.15	0.46	0.84	0.28	39.20	9.14	34.19	12.82	3.17	1.09
	N=2:1	L_P	0.16	0.14	0.29	0.22	0.06	0.05	12.58	6.87	36.05	10.18	2.26	1.40
		Q_P	1.63	1.13	1.54	0.9	0.71	0.36	18.37	9.83	31.87	10.65	15.53	7.34
		L_S	0.62	0.44	1.09	0.96	0.1	0.07	13.04	4.87	12.96	6.08	2.64	1.01
		Q_S	5.83	4.04	6.76	5.14	1.85	0.97	20.57	10.80	29.00	13.96	8.68	3.43
		k	0.5	0.43	1.1	0.82	0.4	0.25	18.07	10.56	35.74	13.40	2.69	0.89

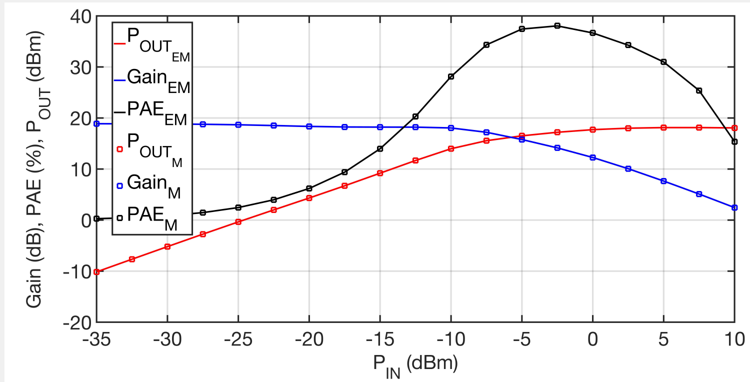
* Present in the paper

CIRCUIT SYNTHESIS USING PACOSYT AND AIDA

PA Performance	PA Specifications	Performances of Selected PA @ 28 GHz (PACOSYT)
***S_{11}* @ 26.5-30 GHz**	< -12 dB	-20.102 dB
***S_{22}* @ 26.5-30 GHz**	< -5 dB	-5.850 dB
***S_{21}* @ 26.5-30 GHz**	> 12 dB	18.885 dB
***S_{21}* Variation (@ 26.5-30 GHz)**	< 1.7dB	Complies with spec.
***Rollet Stb Factor* @ 1Hz-120GHz**	> 1	Complies with spec.
PDC	Minimize (< 70 mW)	33.9874 mW
POUT_MAX	Maximize (> 8 dBm)	18.11 dBm
PAE_{MAX}	Maximize (> 20%)	38.08 %
Power $Gain_{MAX}$	> 12 dB	18.88 dB
P1dB	> 10 dBm	14.128 dBm







CIRCUIT SYNTHESIS USING PACOSYT AND AIDA

PA Performance	PA Specifications	Performances of Selected PA @ 28 GHz (PACOSYT)	Performances of Selected PA @ 28 GHz (Transf. EM simulated)	Error (%)
S_{11} @ 26.5-30 GHz	< -12 dB	-20.102 dB	-20.056 dB	0.087
S_{22} @ 26.5-30 GHz	< -5 dB	-5.850 dB	-5.856 dB	0.230
S_{21} @ 26.5-30 GHz	> 12 dB	18.885 dB	18.881 dB	0.020
S_{21} Variation (@ 26.5-30 GHz)	< 1.7dB	Complies with spec.	Complies with spec.	-
Rollet Stb Factor @ 1Hz-120GHz	> 1	Complies with spec.	Complies with spec.	-
PDC	Minimize (< 70 mW)	33.9874 mW	33.9877 mW	0.001
POUT_MAX	Maximize (> 8 dBm)	18.11 dBm	18.12 dBm	0.055
PAE_{MAX}	Maximize (> 20%)	38.08 %	38.04%	0.105
Power $Gain_{MAX}$	> 12 dB	18.88 dB	18.89 dB	0.052
P1dB	> 10 dBm	14.128 dBm	14.125 dBm	0.021