DECC: Differential ECC for Read Performance Optimization on High-Density NAND Flash Memory

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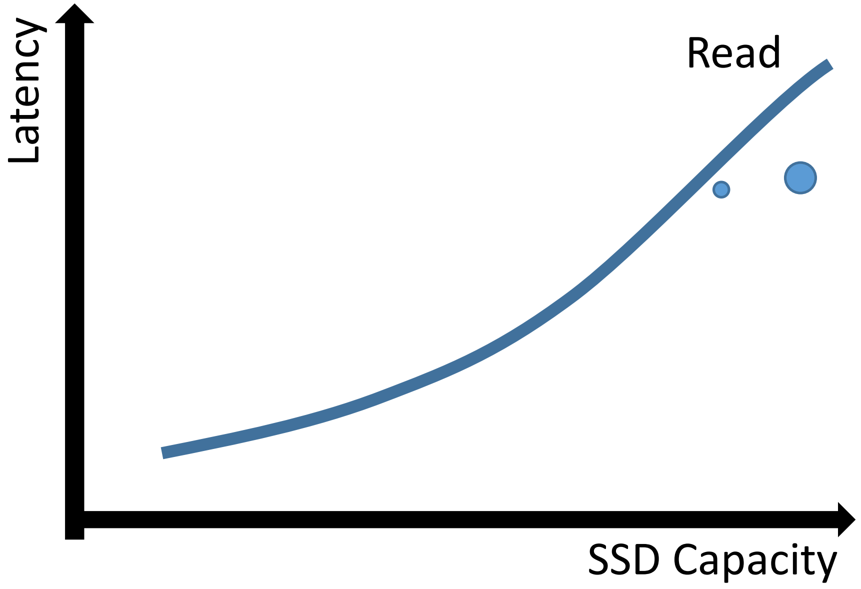
Background

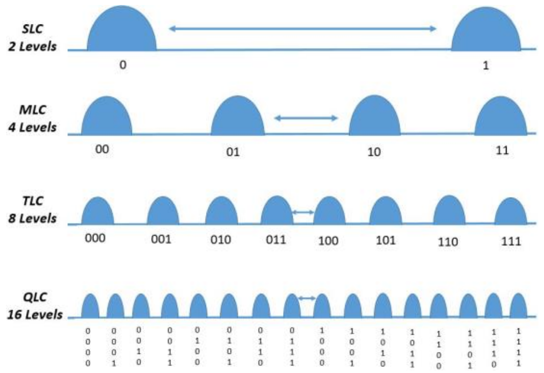
- Solid state drivers(SSDs) are now widely deployed due to the development of high-density and low-cost NAND flash memories.

Background

- Latency of reads is gradually increasing in Solid State Drives

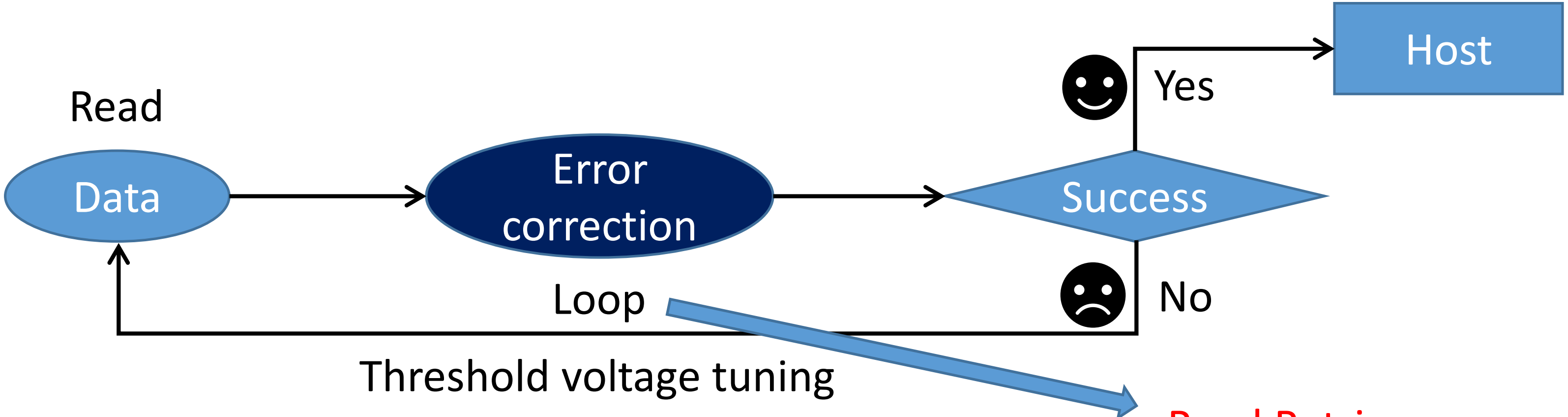


The read latency of flash memory is increasing rapidly.



Background

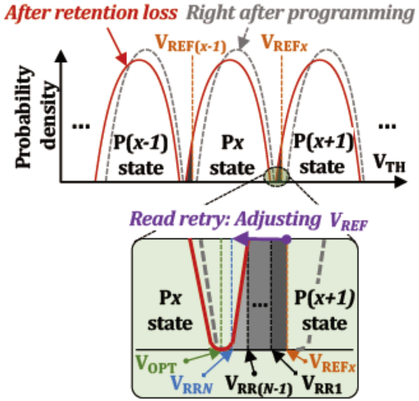
- Error correction overhead due to reduced data reliability



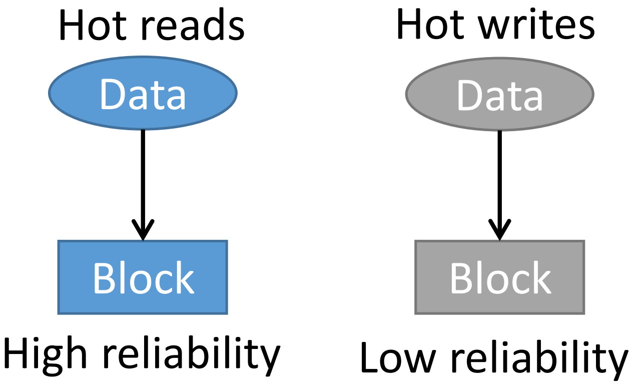
Read Retries

State-of-the-art works

- Reduce error correction overhead
- Threshold voltage tuning
- Optimal threshold voltage prediction



- Data placement
- Placement of data based on access characteristics



Hot reads

Data

Block

High reliability

Hot writes

Data

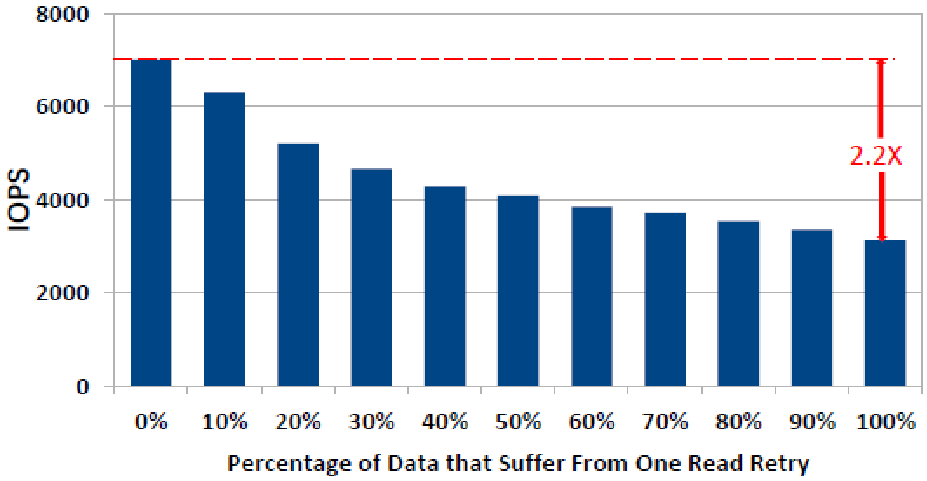
Block

Low reliability

None of these works take the effect of different strengths of ECC on performance into consideration!

Motivation

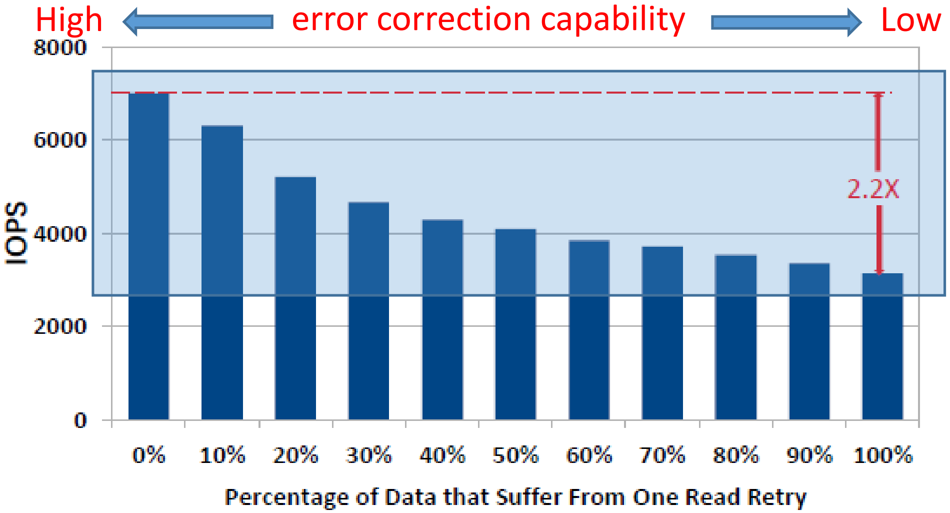
- The influence of ECC's error correction capability on the read performance of high-density flash memory.



Under the single error correction capability of ECC

Motivation

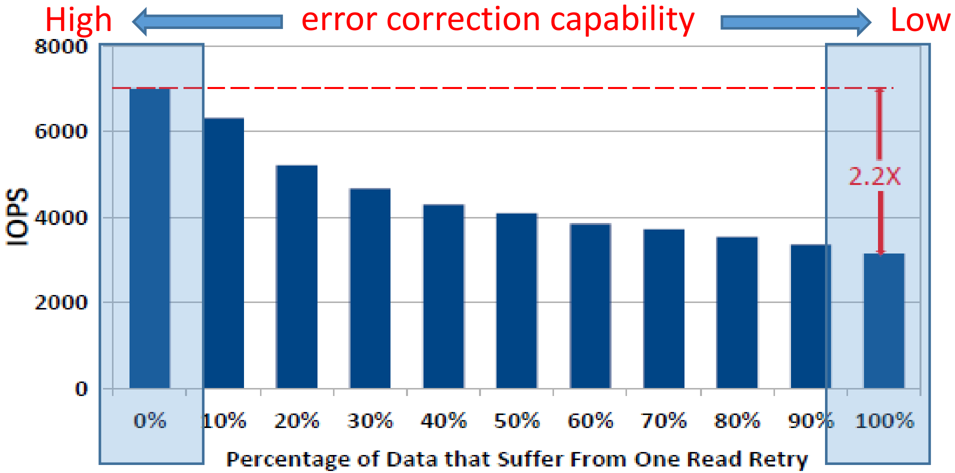
- The influence of ECC's error correction capability on the read performance of high-density flash memory.



Observation: Read performance will decrease as the error correction capability of the ECC decreases.

Motivation

- The influence of ECC's error correction capability on the read performance of high-density flash memory.



Observation: ECC with high error correction capability reduces the number of read retries, but requires more storage space and vice versa.

Our Contribution

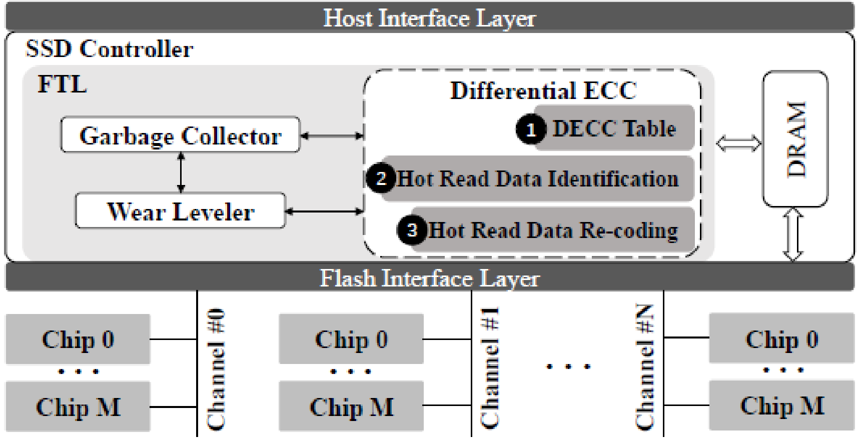
--Differential ECC for High-Density NAND Flash Memory

- Propose a construction and selection for DECC
- Propose a hot read data identification scheme for DECC
- A hot read data aware re-coding scheme is proposed to adopt different strengths of ECC

Architecture

Basic idea:

- Selecting and constructing DECC based on the characteristics of the data
- Recode data that is hot read and read retries occur with strong ECC

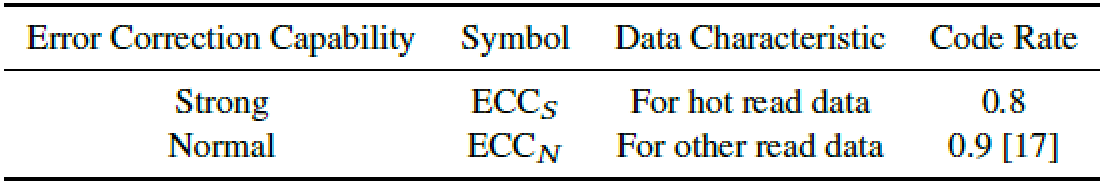


Architecture

Construction and Selection for DECC

- Strong ECC
  - Strong ECC services hot read data
- Normal ECC
  - Normal ECC services other read data

Table 1: Differential ECC Table



Error Correction Capability	Symbol	Data Characteristic	Code Rate
Strong	ECC_S	For hot read data	0.8
Normal	ECC_N	For other read data	0.9 [17]

Architecture

Construction and Selection for DECC

- Strong ECC
  - Strong ECC services hot read data
- Normal ECC
  - Normal ECC services other read data

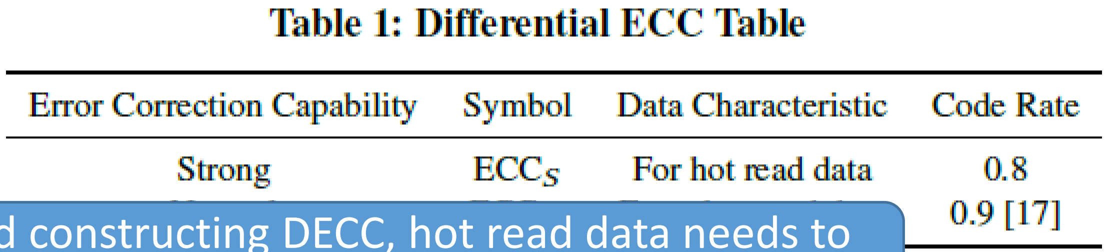


Table 1: Differential ECC Table

Error Correction Capability	Symbol	Data Characteristic	Code Rate
Strong	ECC_S	For hot read data	0.8
			0.9 [17]

After selecting and constructing DECC, hot read data needs to be identified in preparation for re-encoding!

Architecture

A hot read data identification scheme for DECC

- Overhead Analysis
  - Hot read data identification needs to be adapted to DECC's needs
  - The more complex the hot read data identification method is, the higher the overhead will be.
- Hot read data identification based on the number of reads
  - Low overhead and meets DECC requirements

Architecture

A hot read data identification scheme for DECC

- Overhead Analysis
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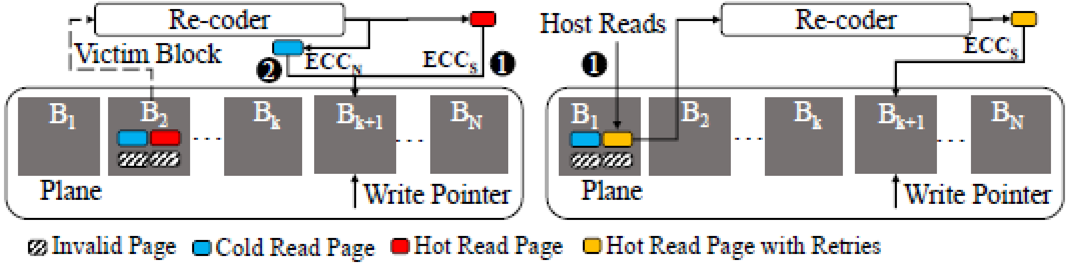
- Hot read data identification based on the number of reads
  - Low overhead and meets DECC requirements

After identifying the hot read data, the hot read data where read retries occur needs to be recoded with strong ECC!

Architecture

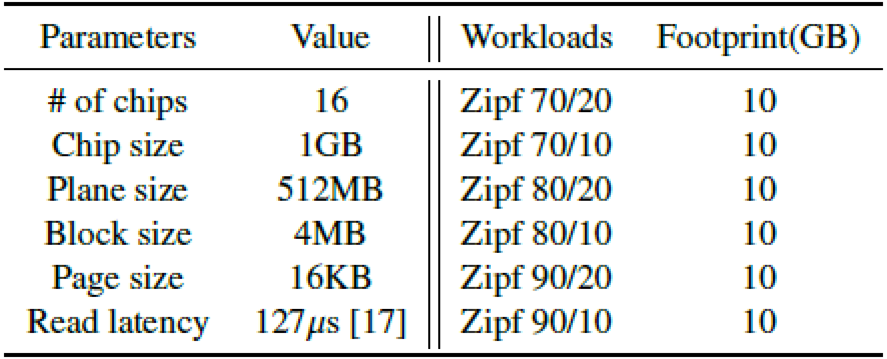
A hot read data aware re-coding scheme

- SSD internal management mechanism
  - Internal management mechanisms such as garbage collection and out-of-place updates will perform data re-coding
- Active re-coding
  - Identified hot reads are recoded if read retries occur



Evaluation

- **Parameters:**
  - Simulator: FEMU
  - 8 channels, 2 chips per channel
- **Workloads:**
  - 6 traces from FIO are simulated
- **Comparative Experiment:**
- **UECC:** a uniform code rate LDPC for the data
- **Refresh:** hot read data encoded using normal ECC after refresh when retry happens
- **MECC:** LDPCs with different code rates are selected according to the P/E cycles

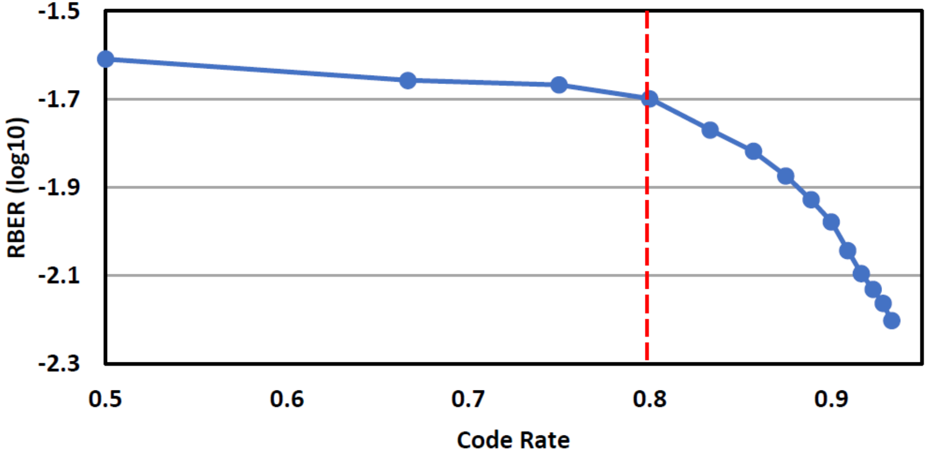


Parameters	Value	Workloads	Footprint(GB)
# of chips	16	Zipf 70/20	10
Chip size	1GB	Zipf 70/10	10
Plane size	512MB	Zipf 80/20	10
Block size	4MB	Zipf 80/10	10
Page size	16KB	Zipf 90/20	10
Read latency	127μs [17]	Zipf 90/10	10

Evaluation

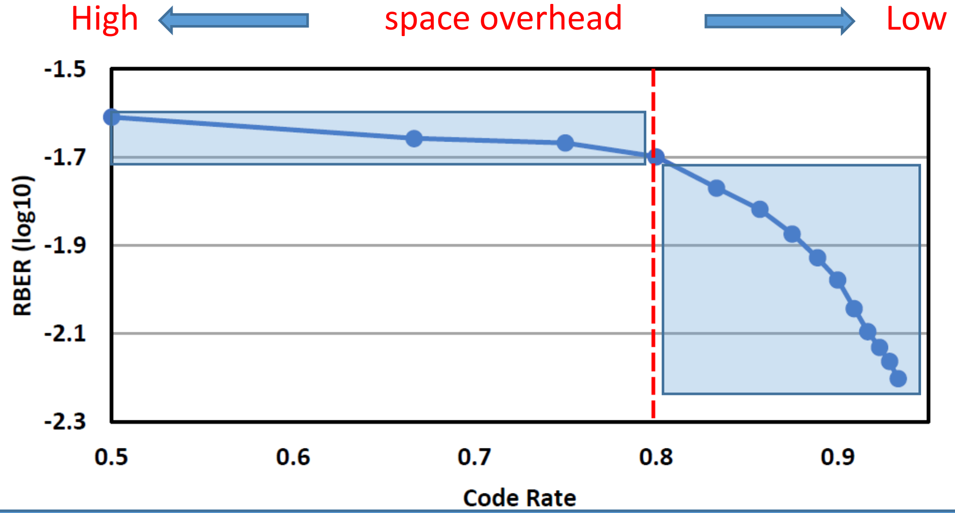
- **The relationship between error correction capability and code rate of ECC**

High ← space overhead → Low



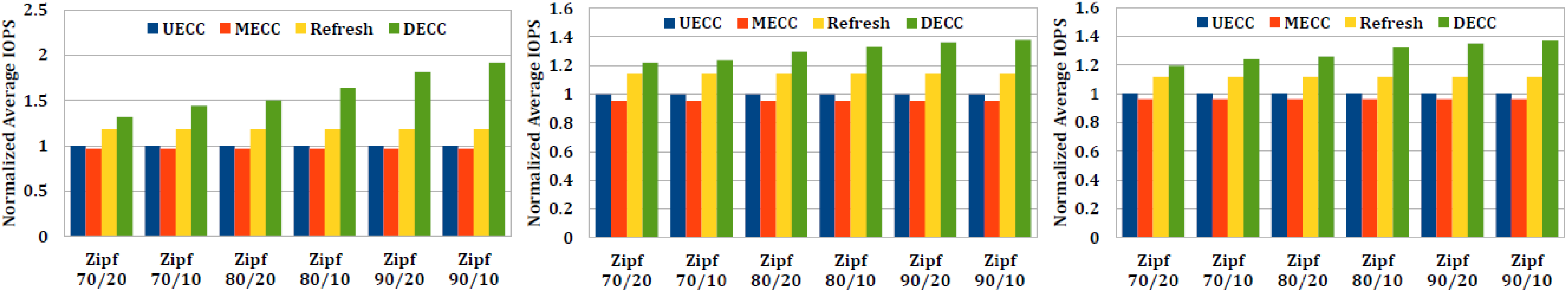
Evaluation

- **The relationship between error correction capability and code rate of ECC**



There is a logarithmic relationship between the error correction capability of ECC and the code rate, and the gain will decrease when the code rate exceeds 0.8.

Evaluation



(a) Retry model 20/80/0

(b) Retry model 10/40/50

(c) Retry model 0/20/80

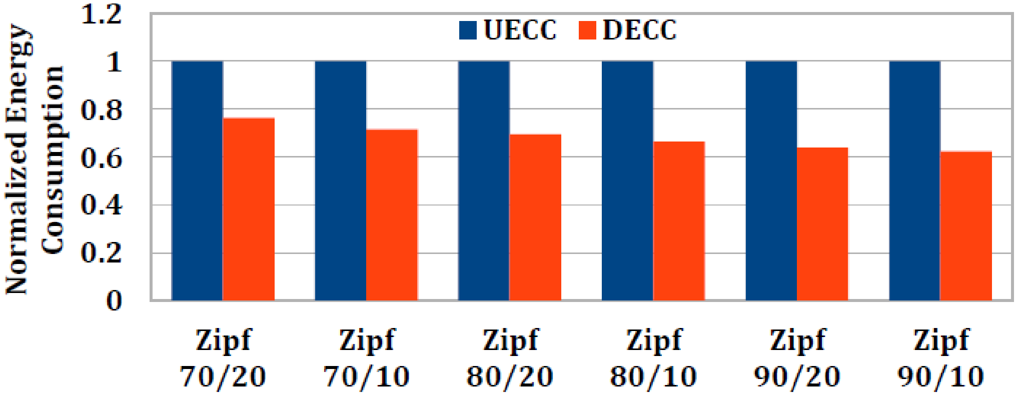
Compared to the UECC:

MECC: cannot optimize read performance

Refresh: achieves 14.8% read performance optimization

DECC: achieves 39.3% read performance optimization

Evaluation



DECC is able to reduce the number of read retries, thus reducing power consumption!

Conclusion

- SSDs are now widely deployed but the read performance is degraded due to the low reliability of state-of-the-art high-density and low-cost SSD.
- We propose differential ECC to optimize high-density NAND flash read performance.
    - Construction and Selection for DECC
    - Hot Read Data Identification for DECC
    - Hot Read Data Aware Re-Coding
- Experimental results show that the proposed method can significantly improve read performance.

DECC: Differential ECC for Read Performance Optimization on High-Density NAND Flash Memory

Thank you!

Questions?

If any questions, please contact us!

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