Demonstration of Order Statistics Based Flash ADC in a 65nm Process

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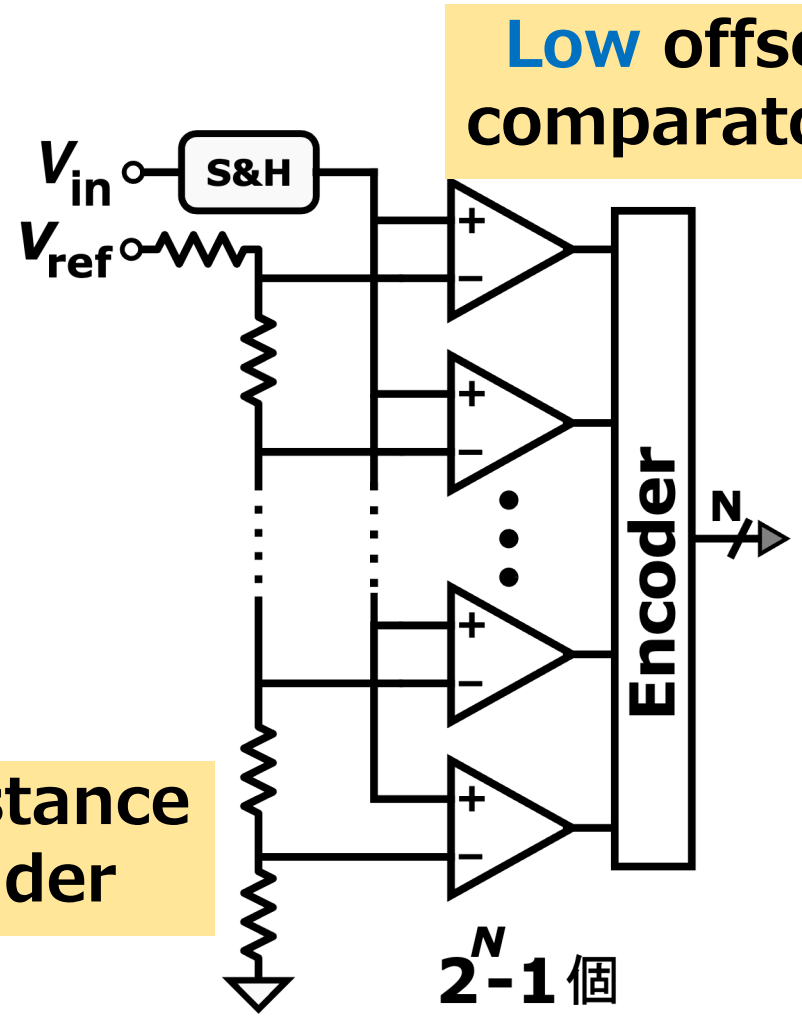
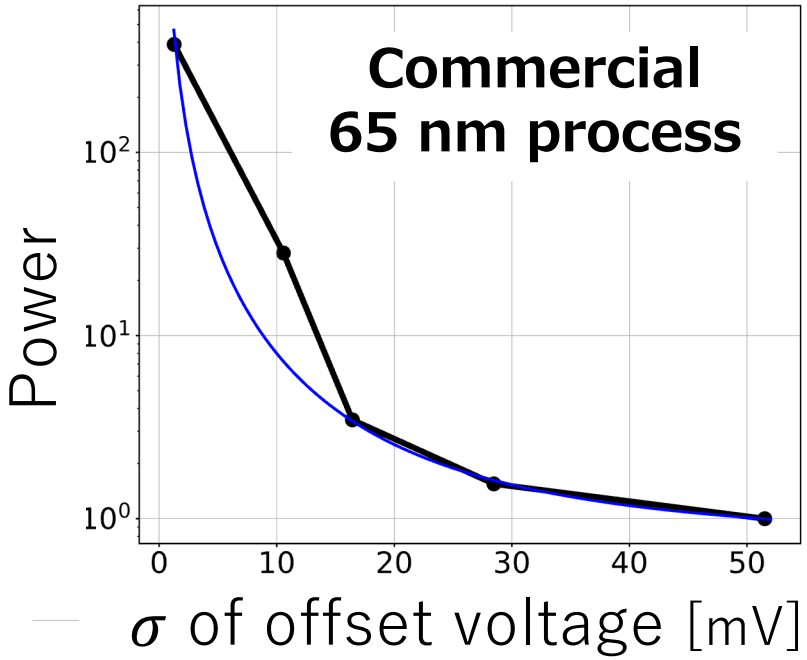
General flash ADC

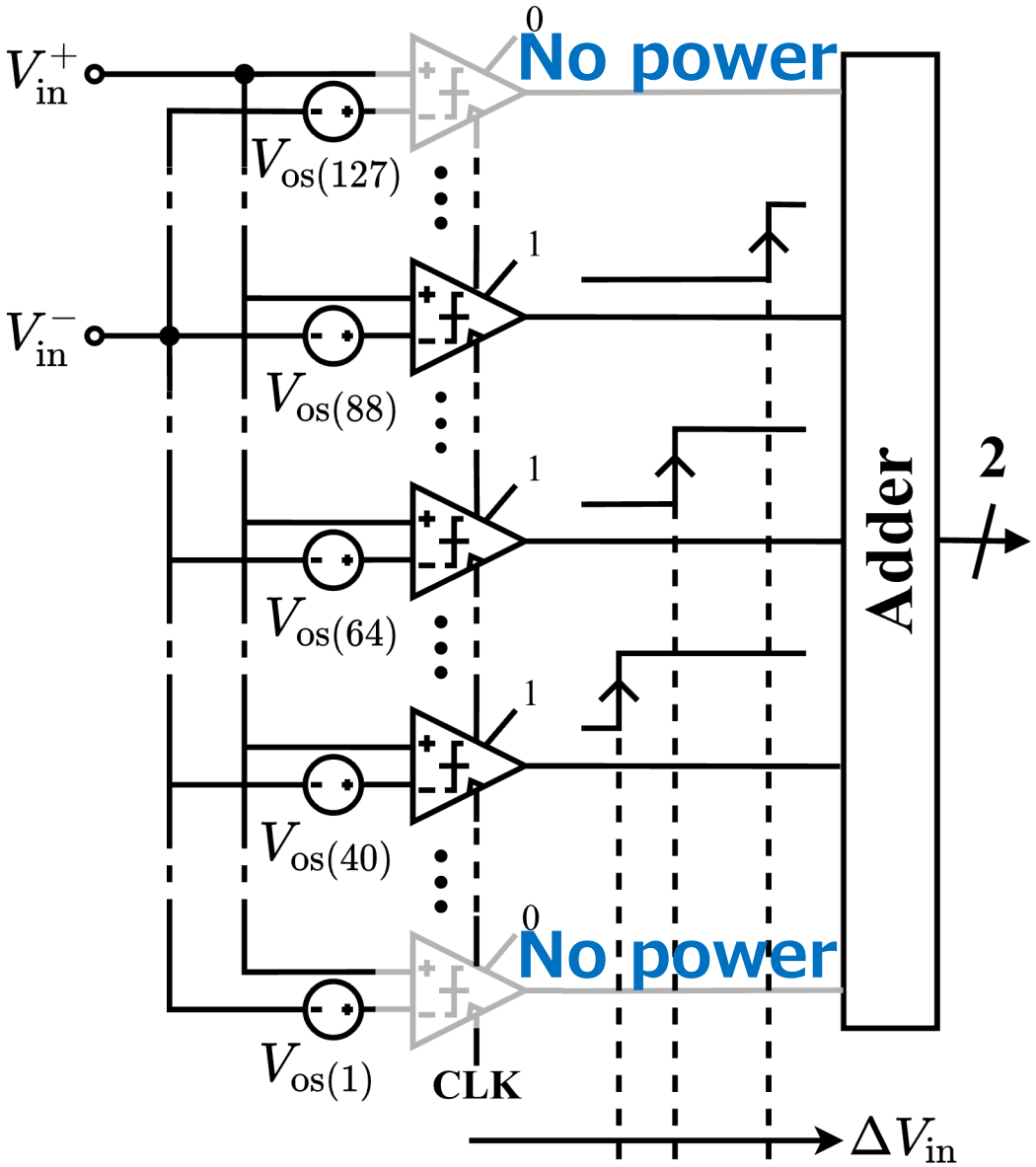


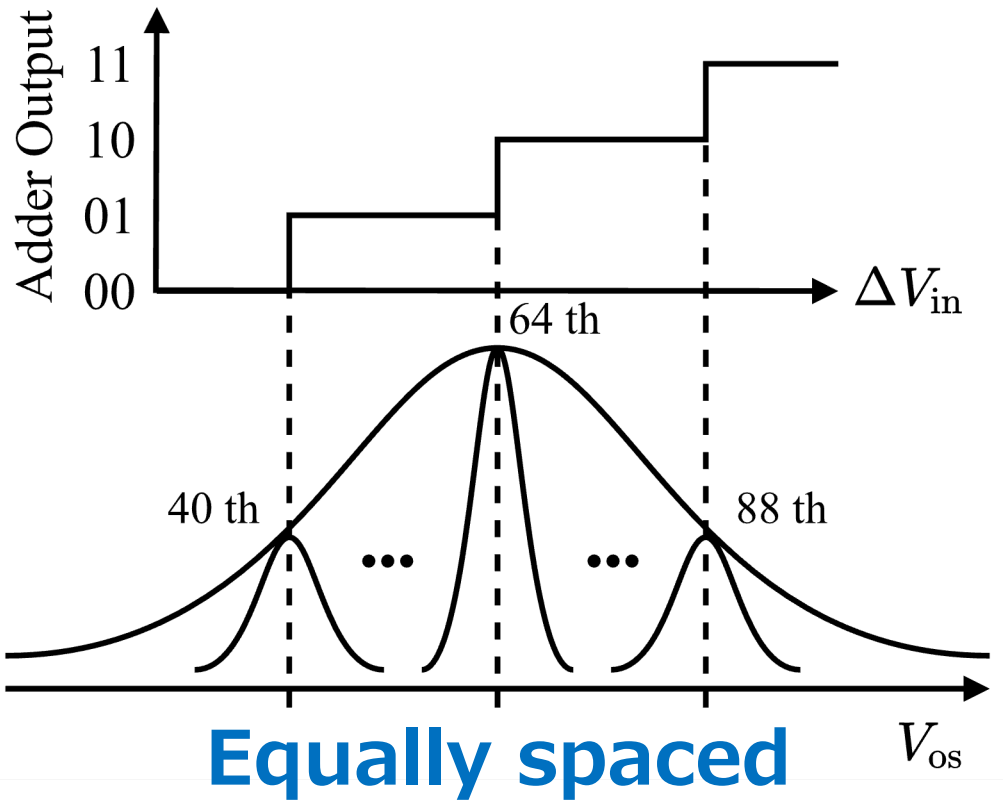
Large process variation

- **Up-size MOSFETs**
- **Large parasitic capacitance**
- **High power consumption**



Order statistics-based flash ADC



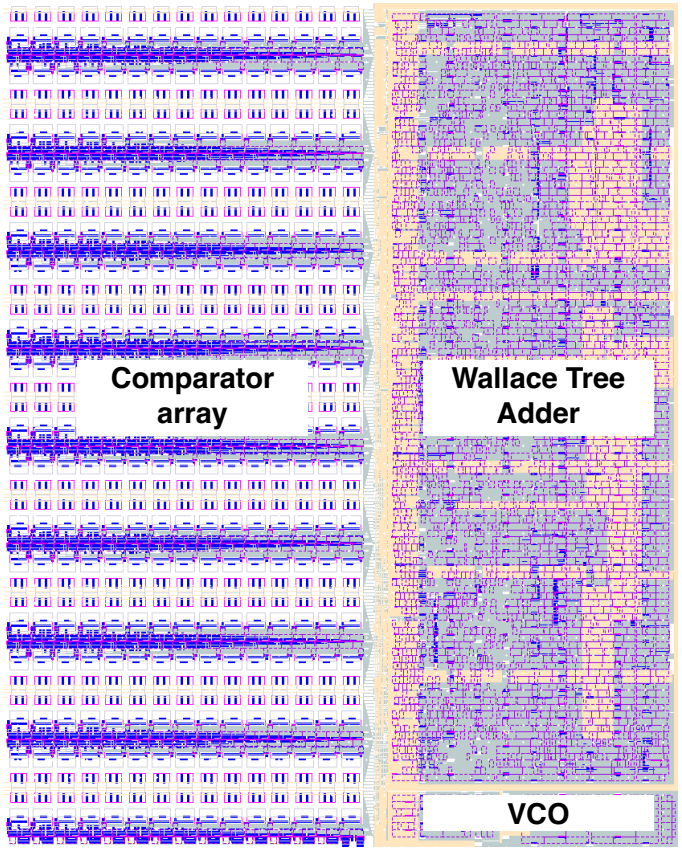


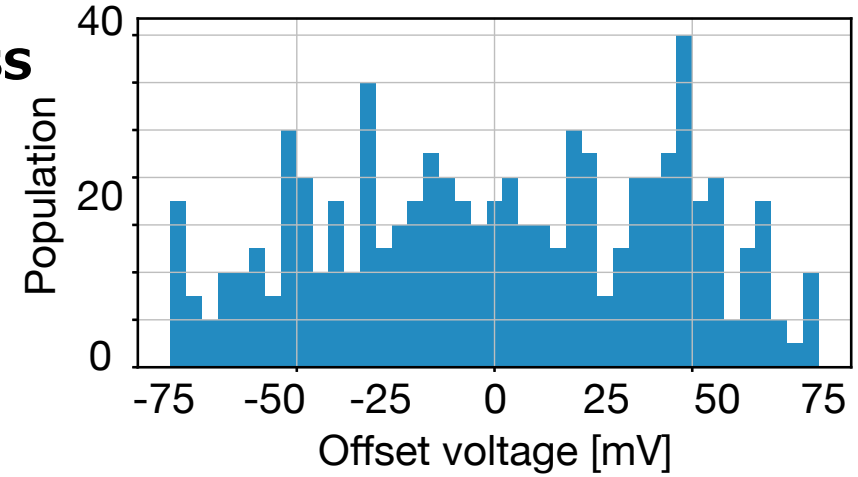
Equally spaced

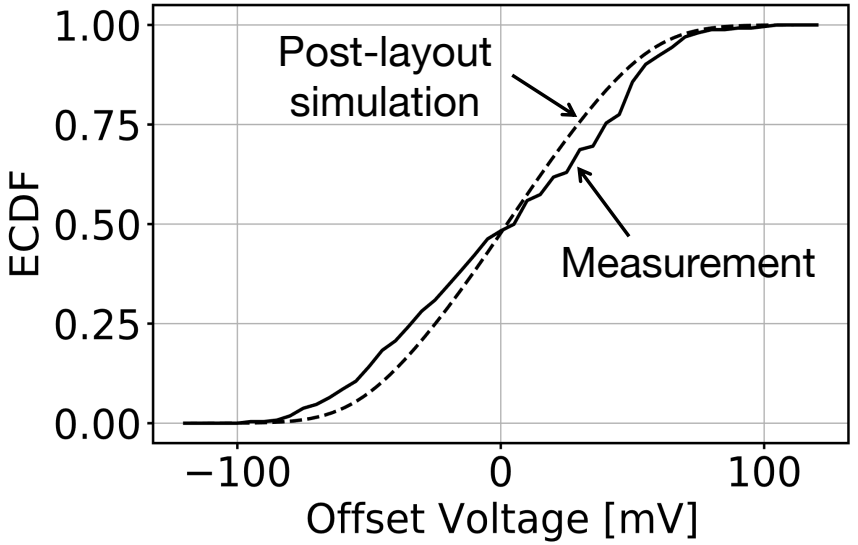
How to estimate rankings of offset voltages?

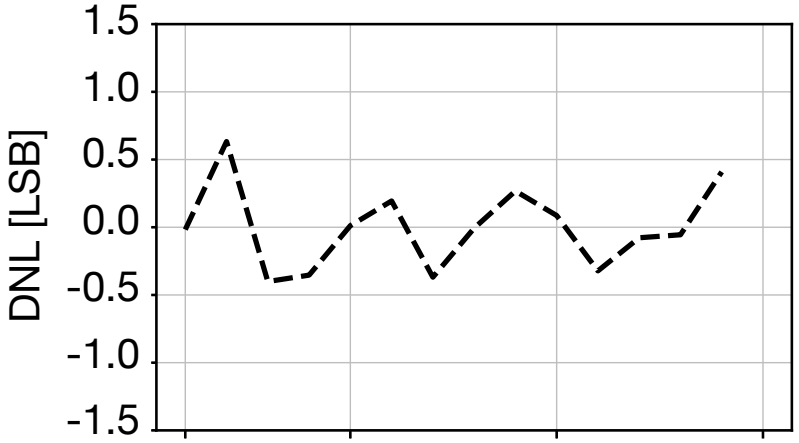
Demonstration

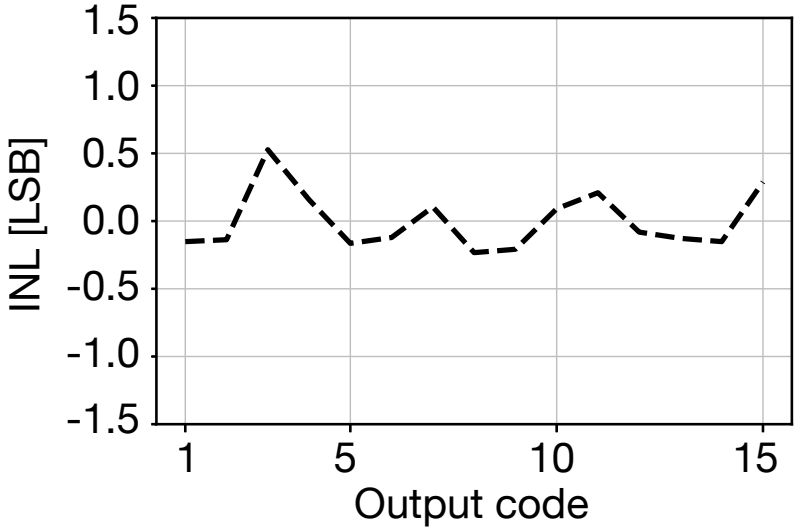
65 nm low-power bulk process











- Successful ADC at 1 GS/s
- Semi-automated design
- Higher performance by distribution tuning
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