On Automating Finger-Cap Array Synthesis with Optimal Parasitic Matching for Custom SAR ADC

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Outline

- Introduction
- Problem Formulation
- Proposed Method
- Experiments
- Conclusion

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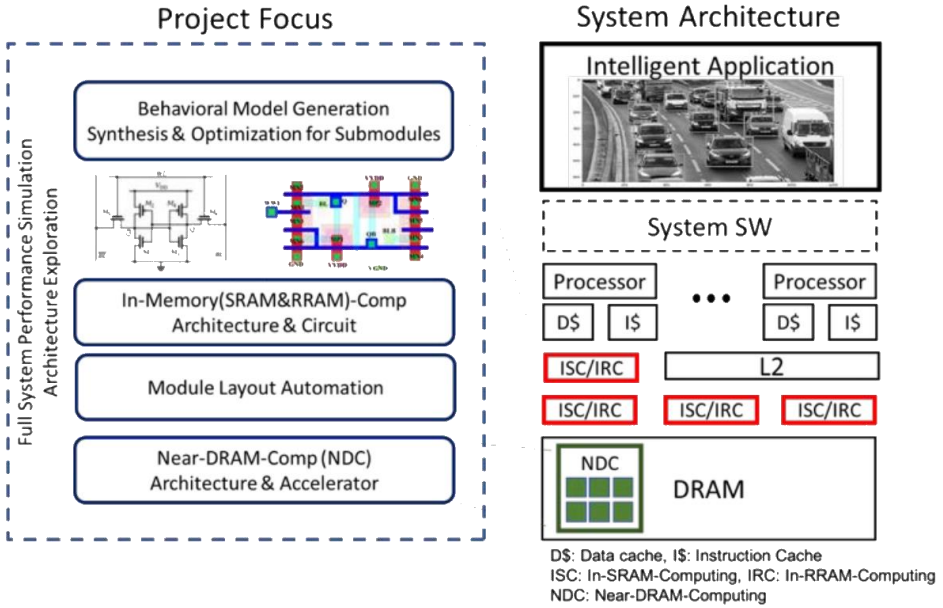
The Requirement of Low-Power

- **AI Edge Applications**
  - Sensor, Smart-phone, watch, Automotive electronics, glasses … etc.
  - Edge computing will be commonly used in the 5G era
  - Challenges: privacy, security, reliability, **power consumption** and other factors.

In-Memory Computation (IMC)

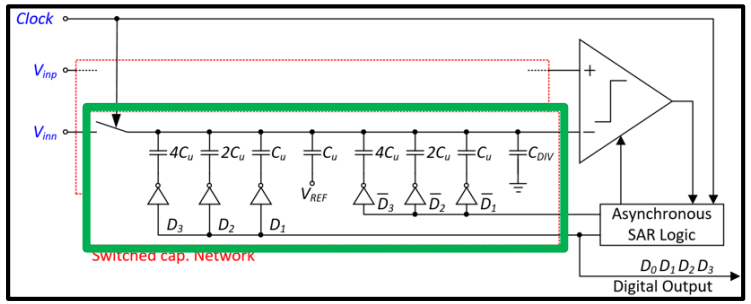
- **Memory-Centric design**
  - AI algorithm needs a lot of computing units to implement a neural network.
  - Replacing the fully digital computing unit to mixed memory computing unit to **reduce the power consumption and huge I/O bandwidth requirement.**
  - Deploying computation to storage and enabling efficient IMC while avoiding massive amount of data movement.

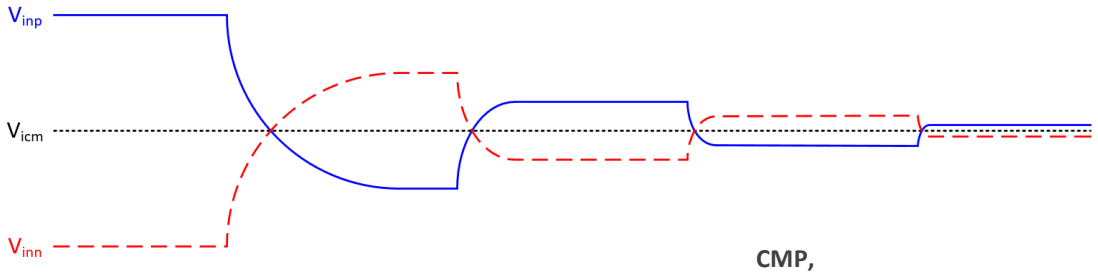


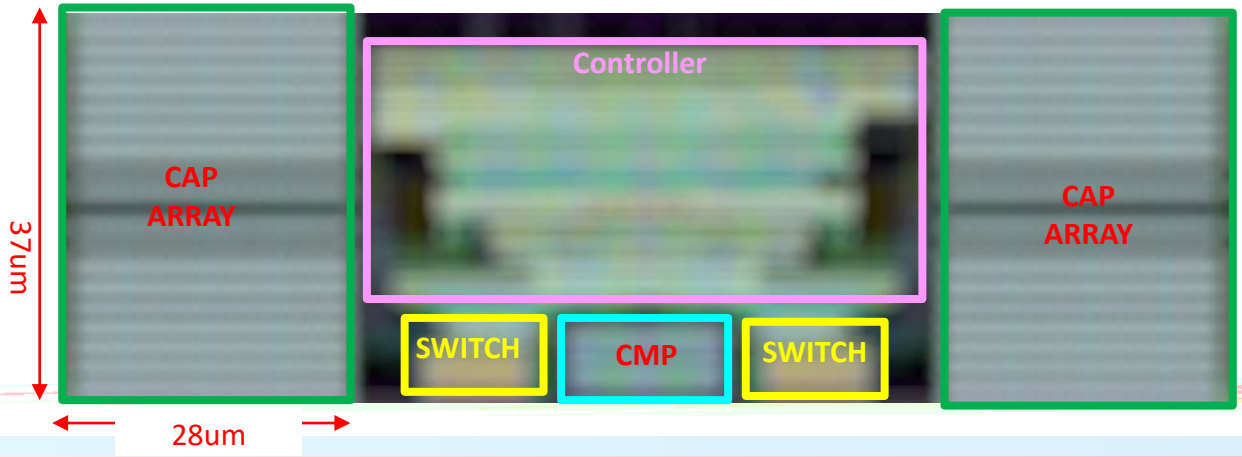
[2] H.-M. Chen, C.-L. Hu, K.-Y. Chang, A. Küster, Y.-H. Lin, P.-S. Kuo, W.-T. Chao, B.-C. Lai, C.-N. Liu, and S.-J. Jou, "On eda solutions for reconfigurable memorycentric ai edge applications," in 2020 IEEE/ACM International Conference On Computer Aided Design (ICCAD), 2020, pp. 1–8.

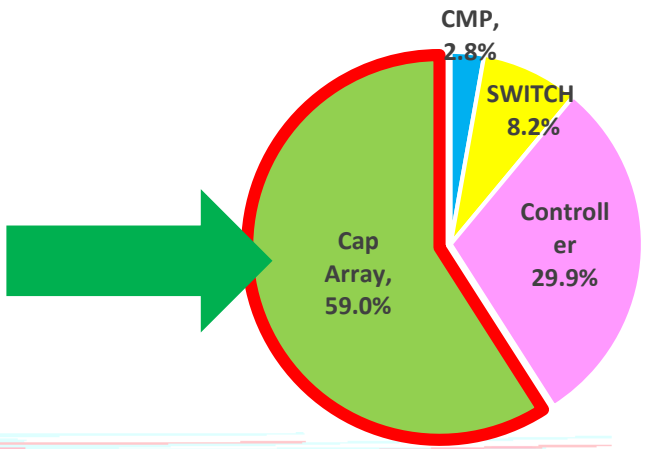
SAR ADC

- **Successive-Approximation-Register (SAR) Analog-to-Digital Converter (ADC)**
  - Excellent power efficiency
  - Consists of individually switched binary-weighted capacitors, a comparator, and SAR logic.
  - Many works try to reduce the capacitance of Cap Array to achieve better power efficiency.



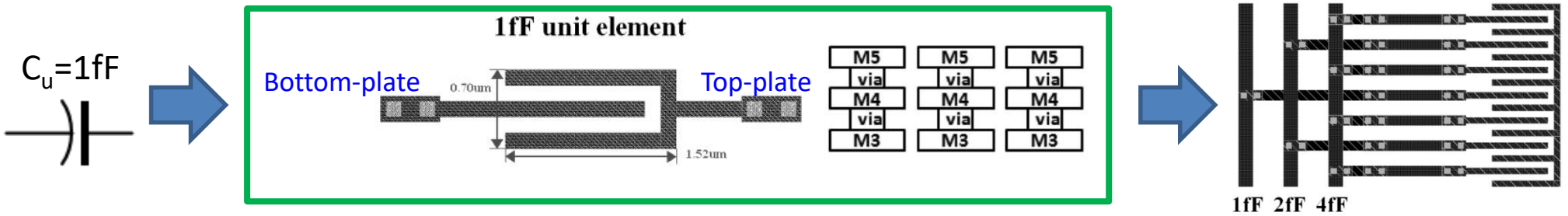




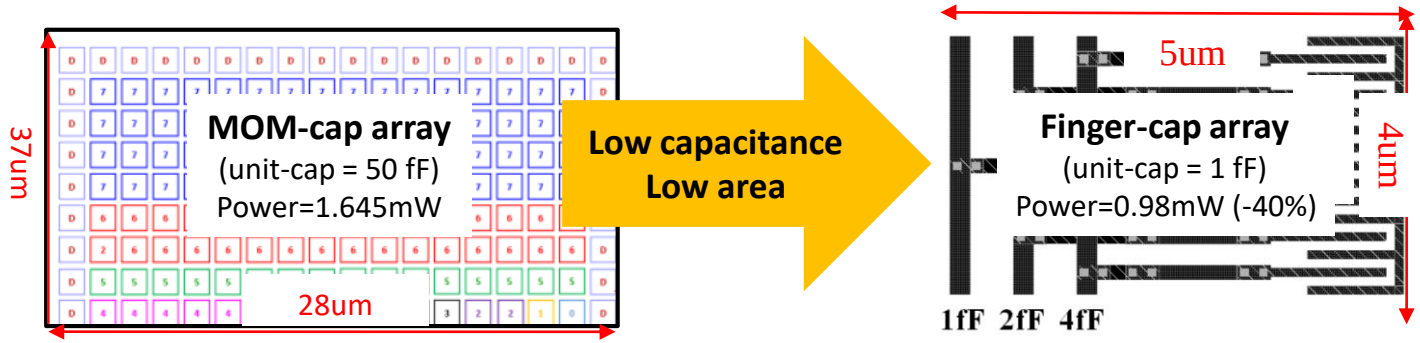


Low-Parasitic Binary-Weighted Capacitors

- Very small finger unit cap [6] (90nm CMOS Process, M4-M7 stacked)



- Some works [6-10] have replaced the traditional MOM CAP Array with this structure of cap array (Finger Cap Array) to further reduce the power consumption.



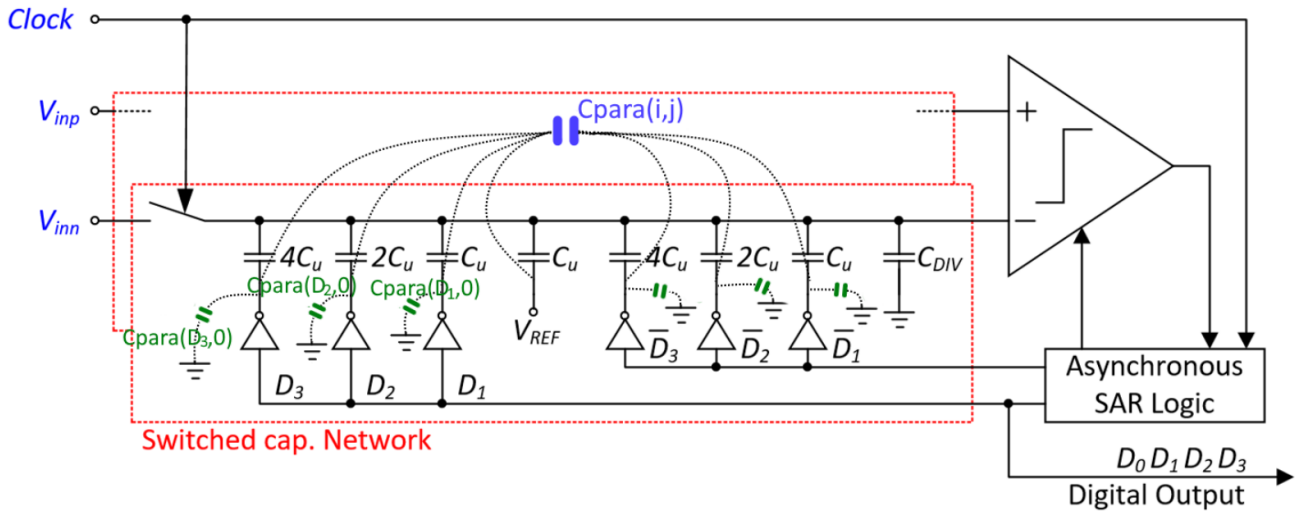
[6] P. Harpe, C. Zhou, X. Wang, G. Dolmans, and H. de Groot, "A 30fj/conversion-step 8b 0-to-10ms/s asynchronous sar adc in 90nm cmos," in 2010 IEEE International Solid-State Circuits Conference (ISSCC), 2010, pp. pp. 388–389.

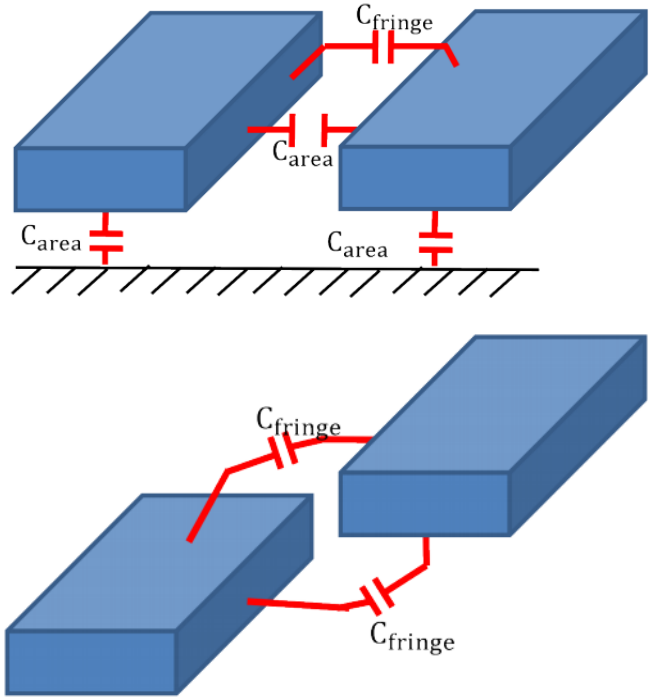
[10] D. Janke, A. Monk, E. Swindlehurst, K. Layton, and S.-H. W. Chiang, "A 9-bit 10-mhz 28- µ w sar adc using tapered bit periods and a partially interdigitated dac," IEEE Transactions on Circuits and Systems II: Express Briefs, pp. pp. 187–191, 2019.

[7] P. J. A. Harpe, C. Zhou, Y. Bi, N. P. van der Meijs, X. Wang, K. Philips, G. Dolmans, and H. de Groot, "A 26 µ w 8 bit 10 ms/s asynchronous sar adc for low energy radios," IEEE Journal of Solid-State Circuits (JSSC), pp. 1585–1595, 2011.

Motivation --- Parasitic Impact on SAR-ADC

- The accuracy and performance of a SAR-ADC are highly correlated with the accuracy of capacitance ratio of binary-weighted capacitors, while the power consumption and setting time depends on the absolute capacitance values.

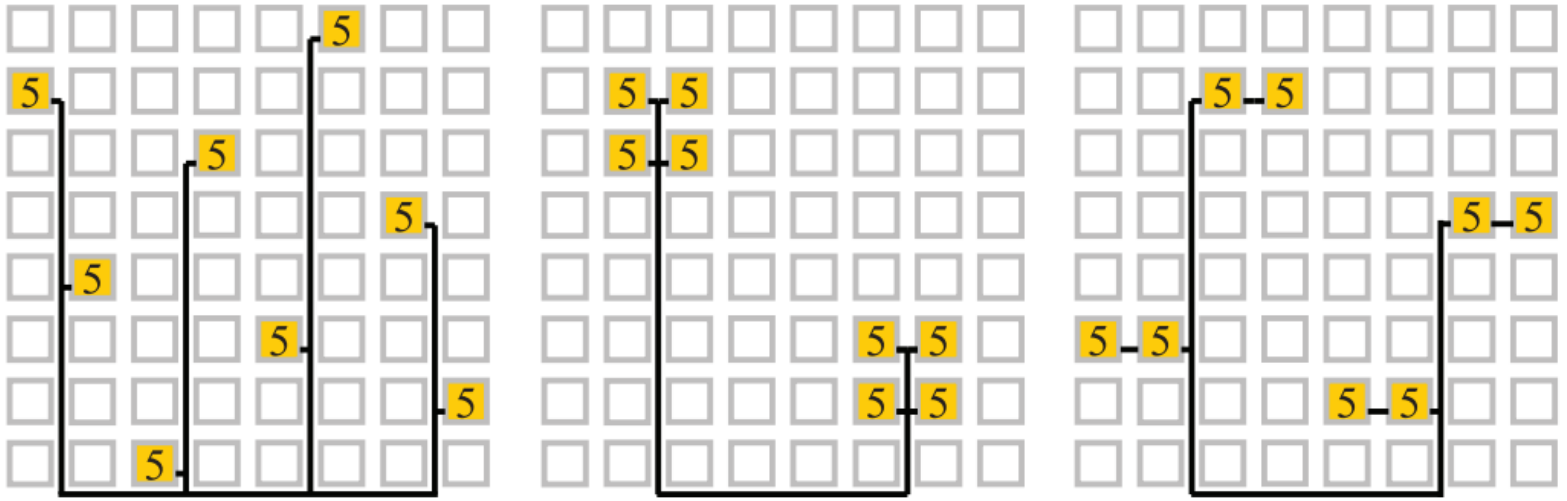




$$\widetilde{C}_i = 2^{i-1} * C_u + Cpara_i$$

Previous Works --- Binary-Weighted Capacitors

- Most of the previous works focus on the placement and/or routing in the **MOM/MIM-Cap** structure.
  - [5, 16] emphasized the matching properties of common-centroid placement.
  - [9, 11] proposed some methods or guidelines for routing to minimize the parasitic capacitance and/or the mismatch of the capacitance ratio.



[11] M. P.-H. Lin, V. W.-H. Hsiao, C.-Y. Lin, and N.-C. Chen, "Parasitic-aware common-centroid binary-weighted capacitor layout generation integrating placement, routing, and unit capacitor sizing," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 36, no. 8, pp. 1274–1286, 2017.
[9] K.-H. Ho, H.-C. Ou, Y.-W. Chang, and H.-F. Tsao, "Coupling-aware length-ratiomatching routing for capacitor arrays in analog integrated circuits," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 34, no. 2, pp. 161–172, 2015.

Previous Works

- None of the previous works optimizes the matching properties automatically in the structure of Finger-Cap-Array.
- The impact from routing parasitics becomes enormous with such small unit capacitor.

Contribution

- We presents a new framework to synthesize a Finger-Cap-Array layout for low-power SAR ADC
  - We first adopt the common-centroid placement style, “partially interdigitated” (PI), in [10] to generate an optimal binary-weighted capacitors placement result in SAR-ADC with balanced parasitic capacitance and mismatch.
  - In the routing stage, we present the parasitic-aware ILP-based weight-dynamic network routing algorithm to generate the optimal layout.
  - Our approach helps designers save much time when designing the switched binary-weighted capacitors.

[10] D. Sayed and M. Dessouky, “Automatic generation of commoncentroid capacitor arrays with arbitrary capacitor ratio,” in Proc. IEEE/ACM Design Autom. Test Europe Conf., Paris, France, 2002, pp. 576–580.

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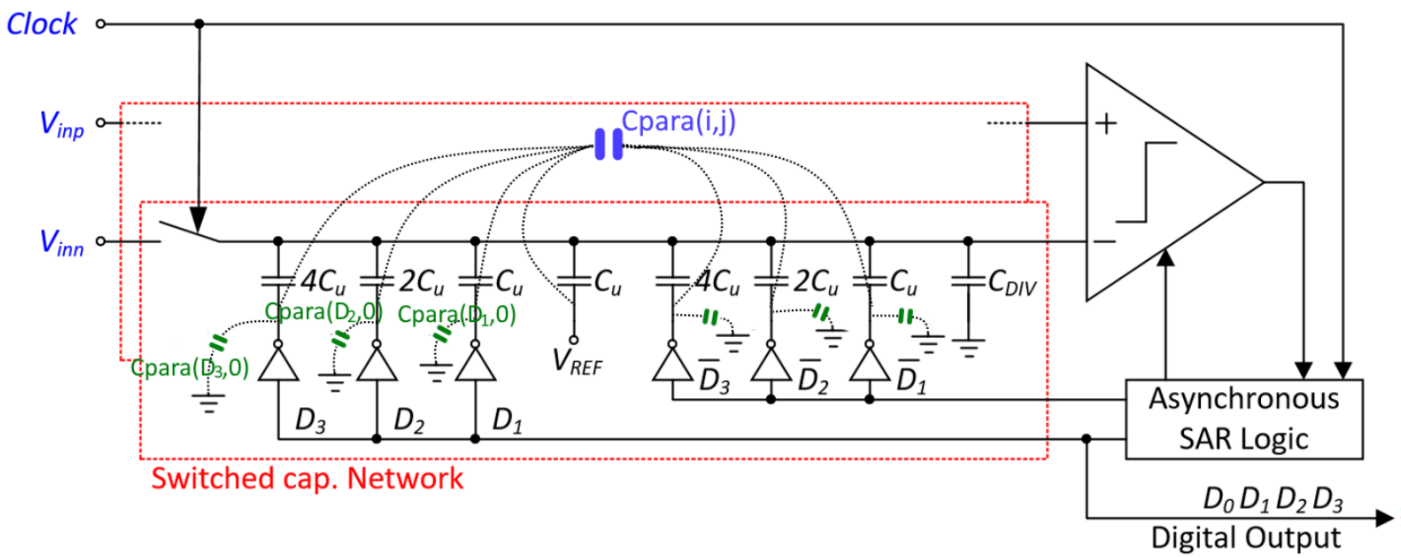
Problem Formulation

- Objective: To generate the capacitor-array layout with the minimized total parasitic capacitance and capacitance ratio mismatch for optimal Effect Number of Bit (ENOB) result
- Cost function:

$$\varphi = \sum_{i}^{N} \alpha * \widetilde{C}_i + \beta * \left| \widehat{C}_i - \widetilde{C}_i \right|$$

where $\widehat{C}_i$ and $\widetilde{C}_i$ is the target and real capacitance.



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  - Common-Centroid Placement
  - Parasitic-Aware ILP-based Routing
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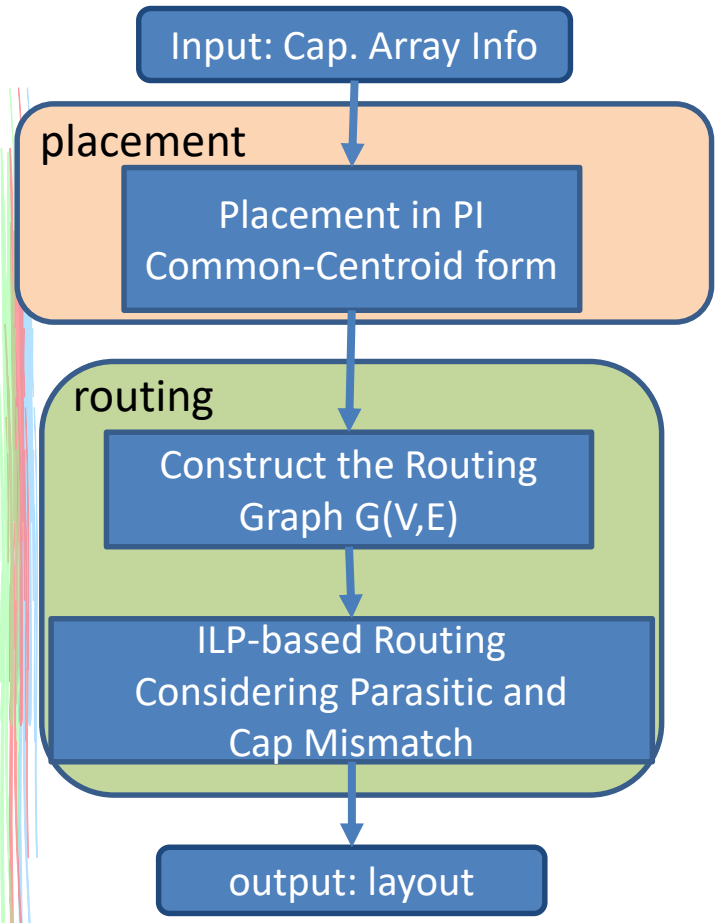
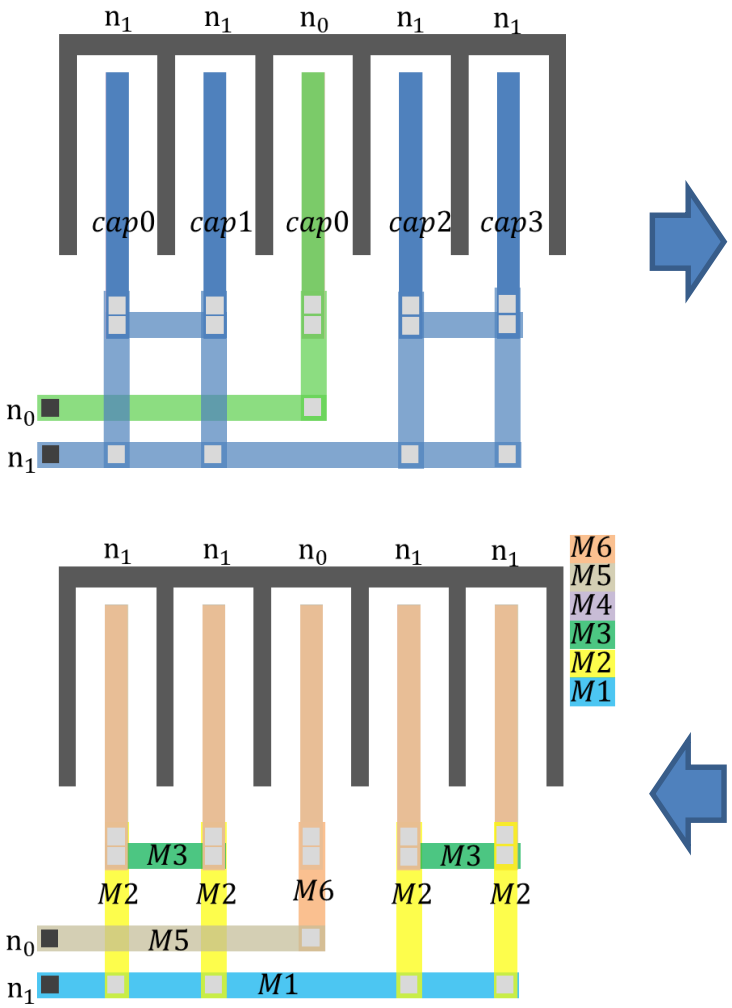
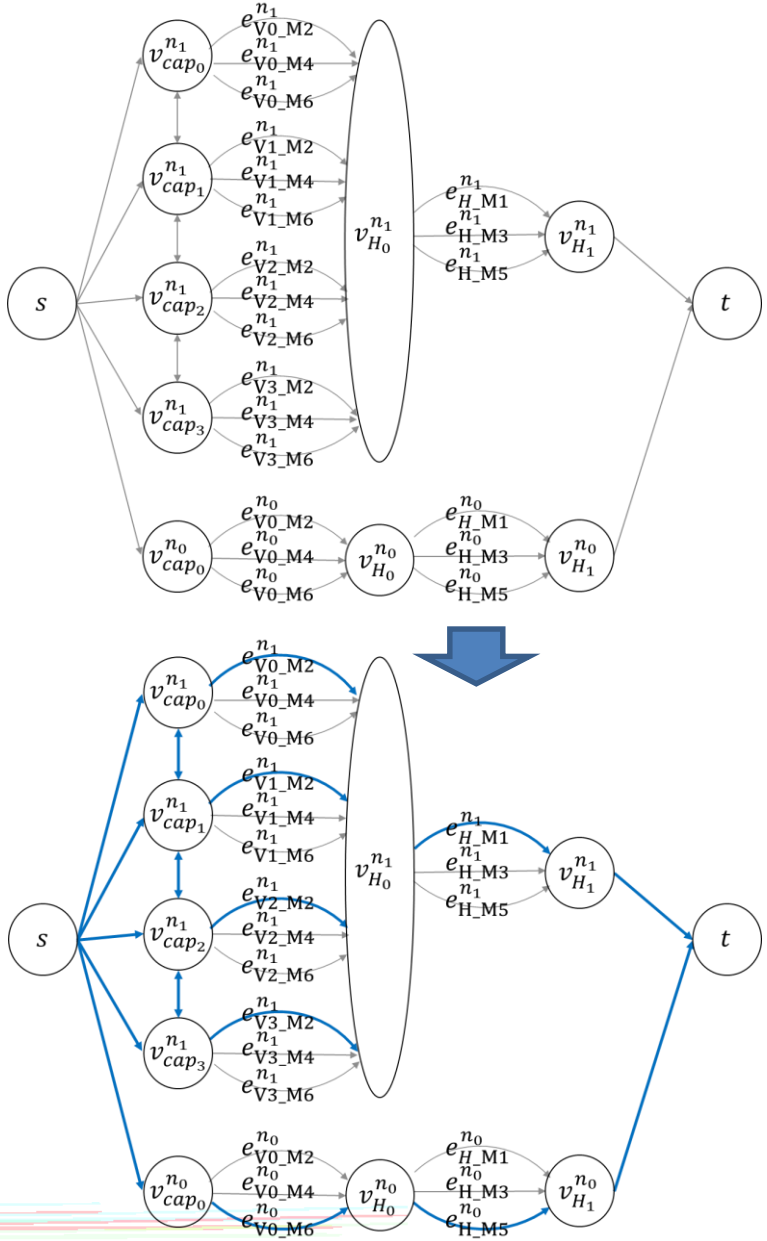
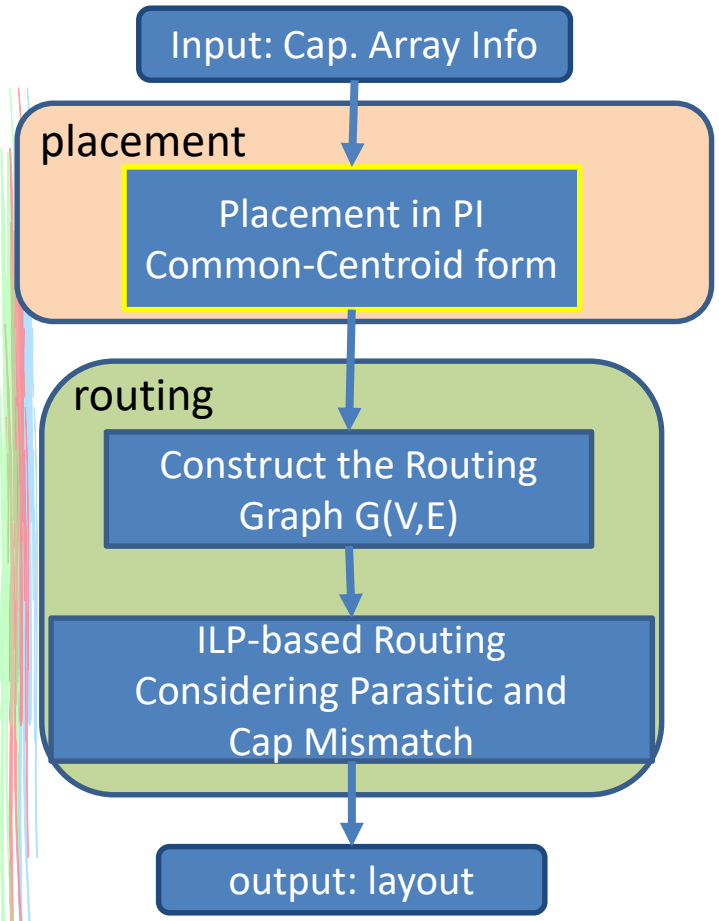
Algorithm Overview



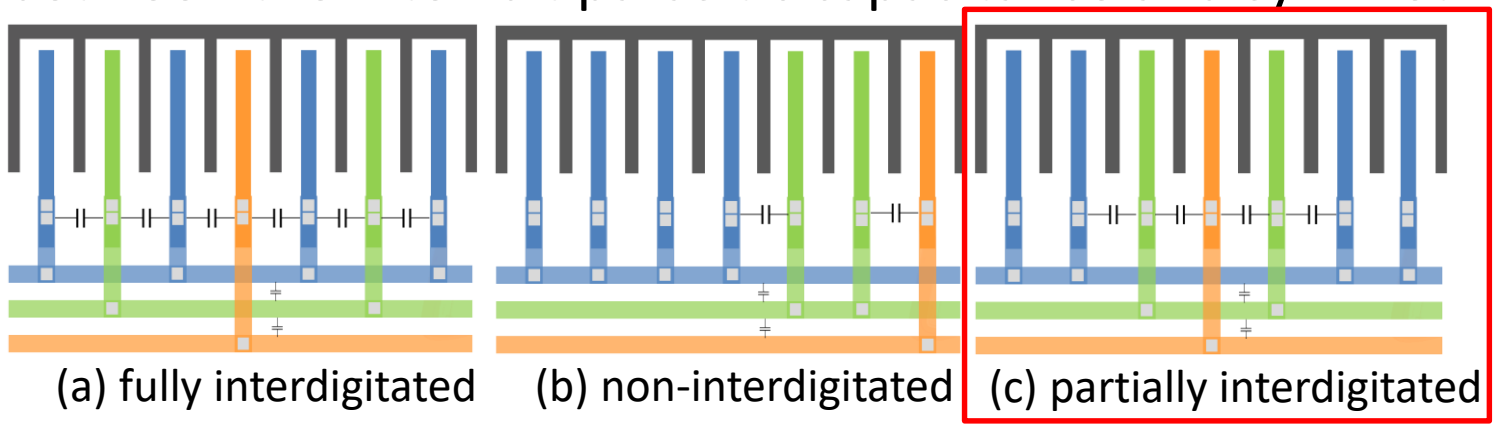




One-Dimension Unit Finger Capacitors Placement



- [10] proposed a common-centroid placement style, “partially interdigitated”(PI), that strikes a balance between the inter-bit parasitic capacitance and symmetric.

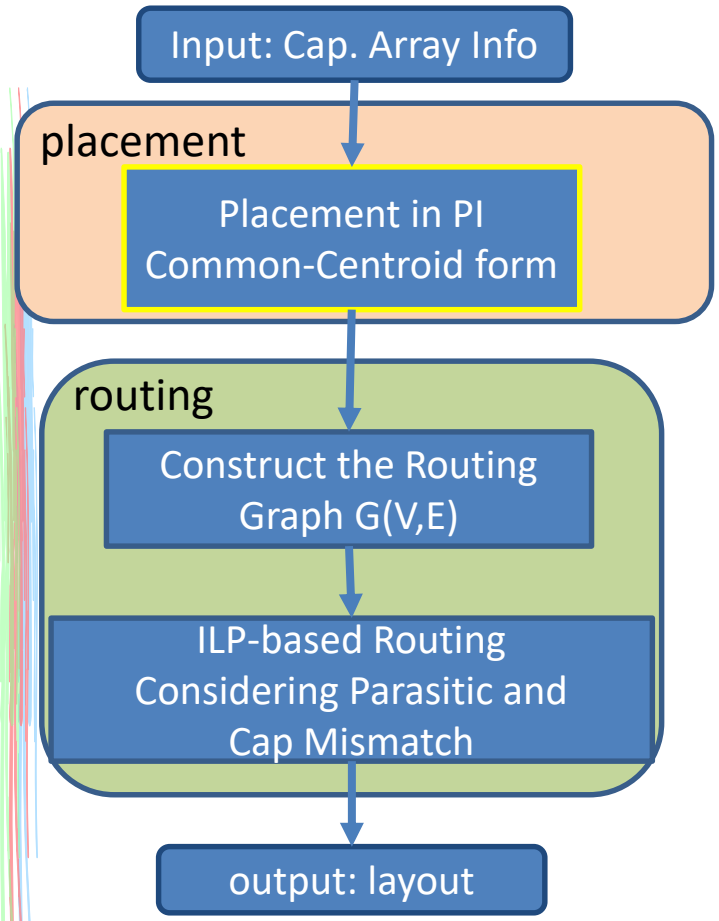


(a) fully interdigitated (b) non-interdigitated (c) partially interdigitated

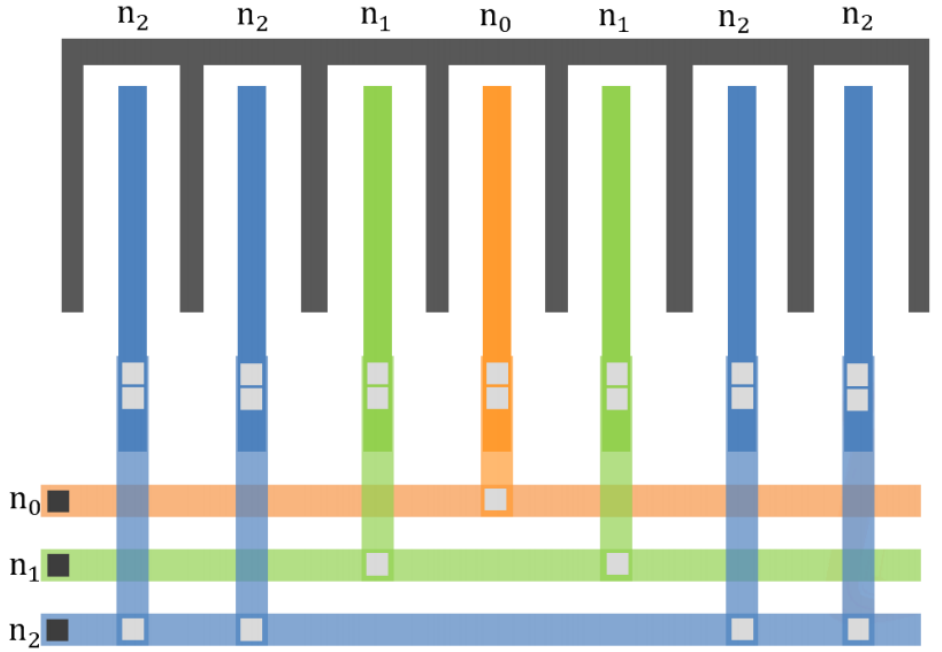
- Most of the previous works evaluate the matching quality of a common-centroid placement with the cost function:

$$M = \sigma\left(2 \times \frac{(C_{u(i_1,j_1)} - C_{u(i_2,j_2)})}{(C_{u(i_1,j_1)} + C_{u(i_2,j_2)})}\right) = \frac{\sigma}{\mu} \cdot \sqrt{2 \cdot (1-\rho)}.$$

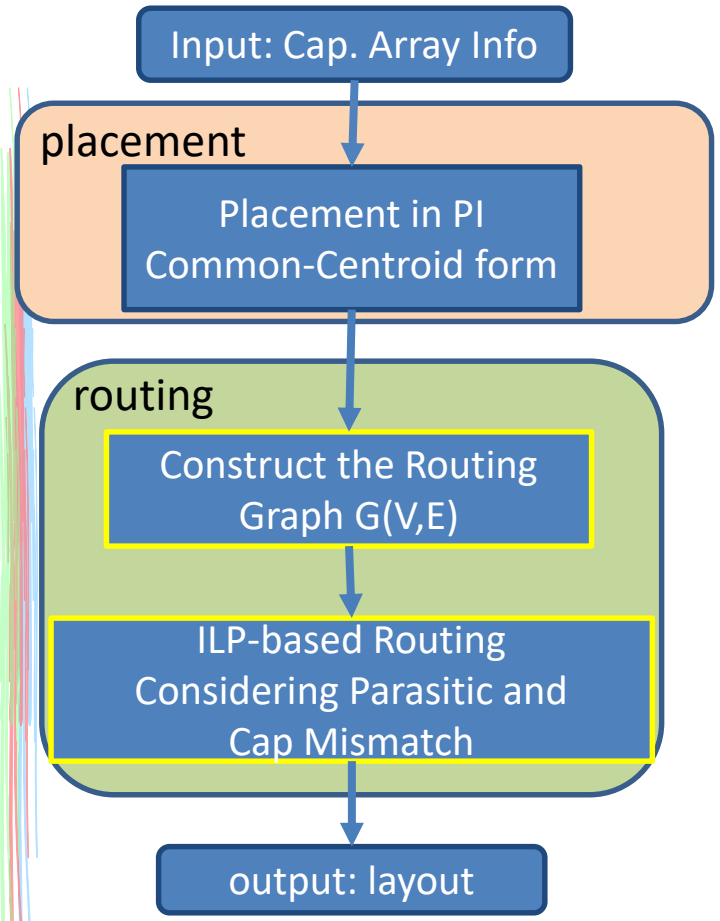
One-Dimension Unit Finger Capacitors Placement



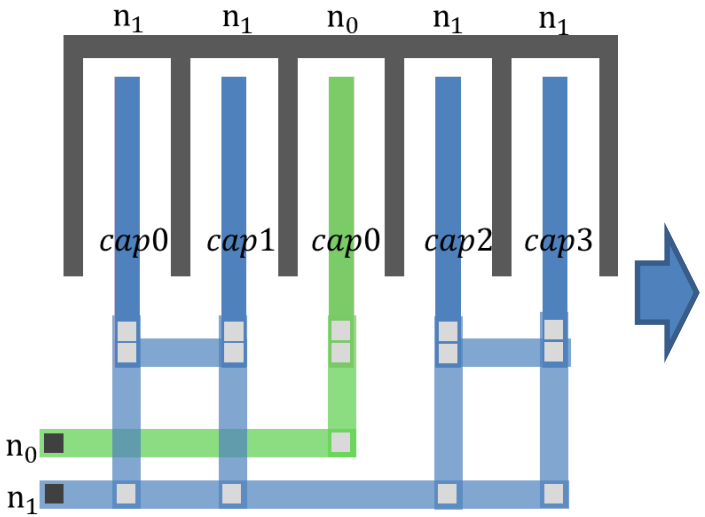
- Example: 3 nets with the ratio 1 : 2 : 4.
  - The capacitors of the net with the biggest ratio are put at the outermost of the array.
  - The vertical line of the net with the biggest ratio is put at the farthest row.

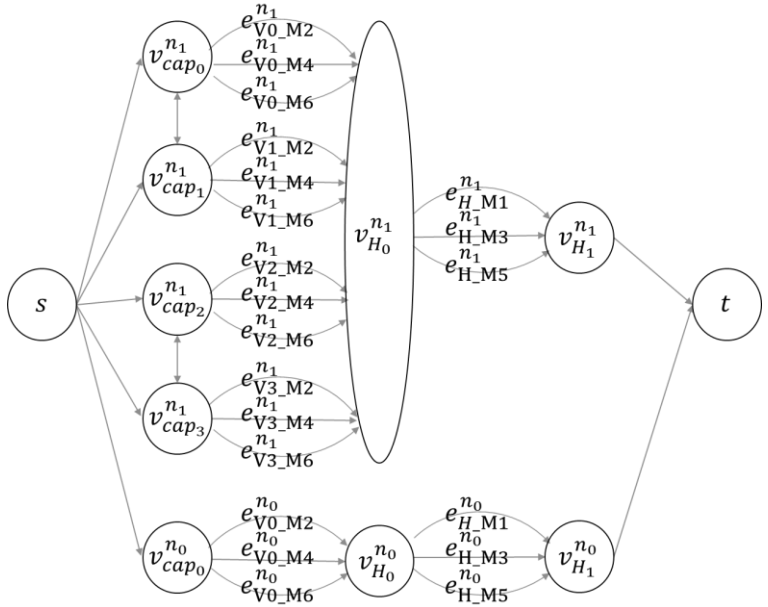


Parasitic-aware ILP-based Weight-Dynamic Network Routing Algorithm



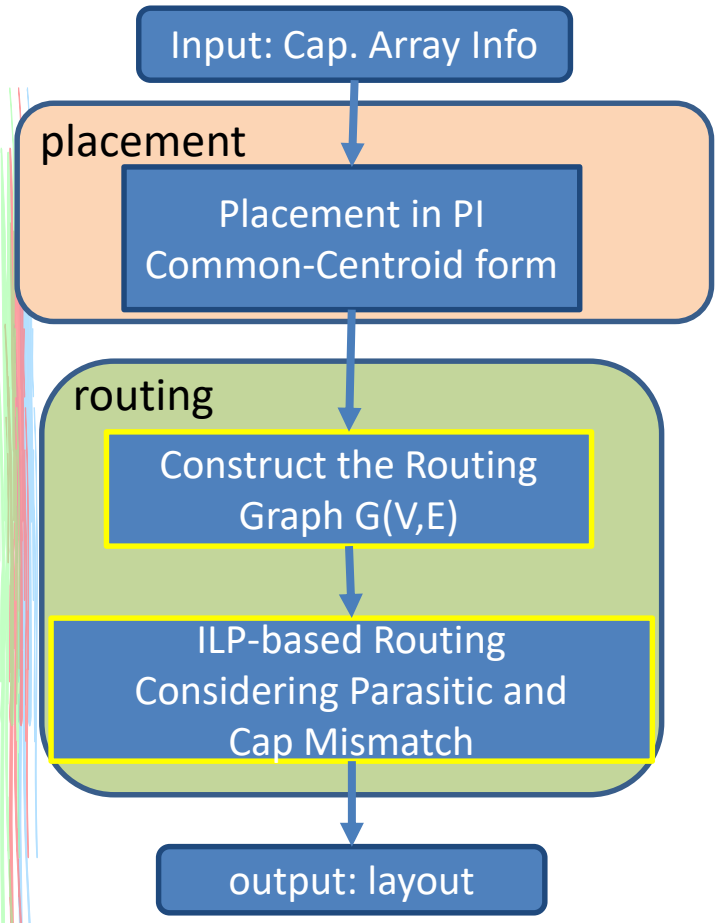
- Cost assignment and network construction
  - Transfer each pin and wire to node.



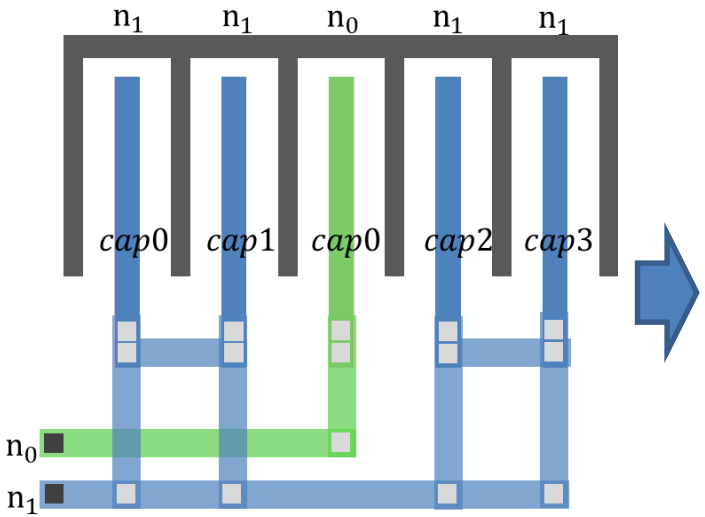


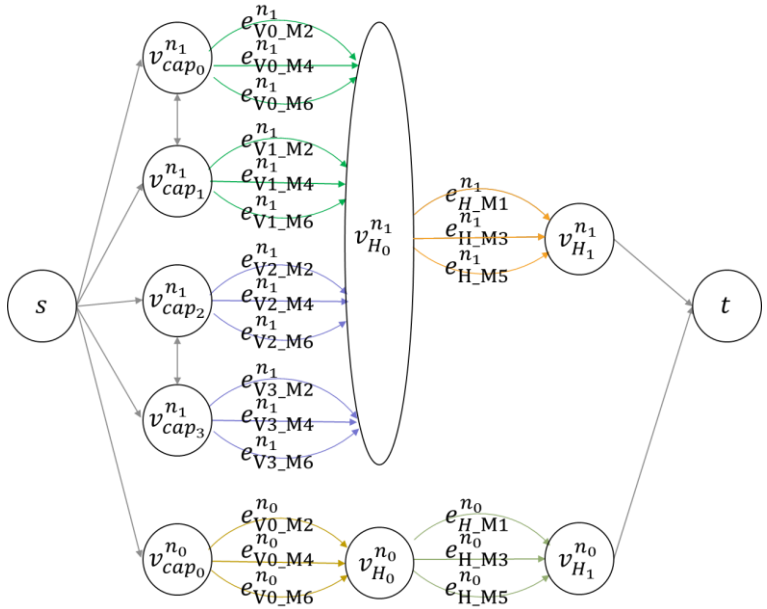
  - $\varphi = \sum_i^N \alpha * \widetilde{C}_i + \beta * \left|\widehat{C}_i - \widetilde{C}_i\right|$
  - where $\widehat{C}_i$ and $\widetilde{C}_i$ is the target and real capacitance.
  - $\widehat{C}_i = \widetilde{C_0} * r_i / r_0$
  - $\widetilde{C}_i = 2^{r_i - 1} * C_u + Cpara_i$

Parasitic-aware ILP-based Weight-Dynamic Network Routing Algorithm



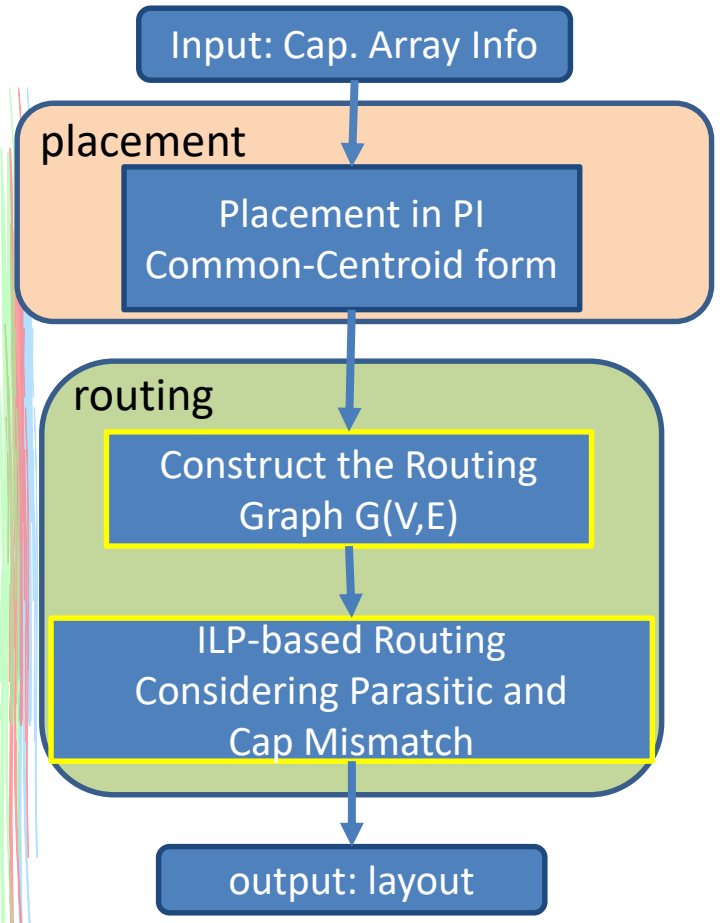
- Connectivity Constraint
  - Group the connected edges for connectivity



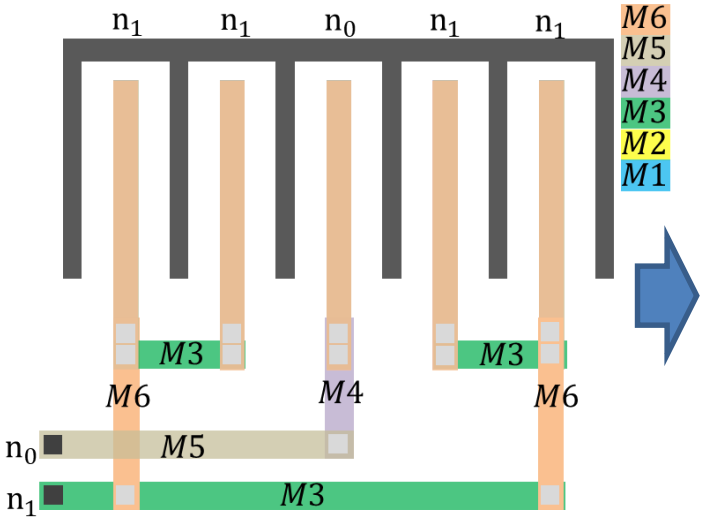


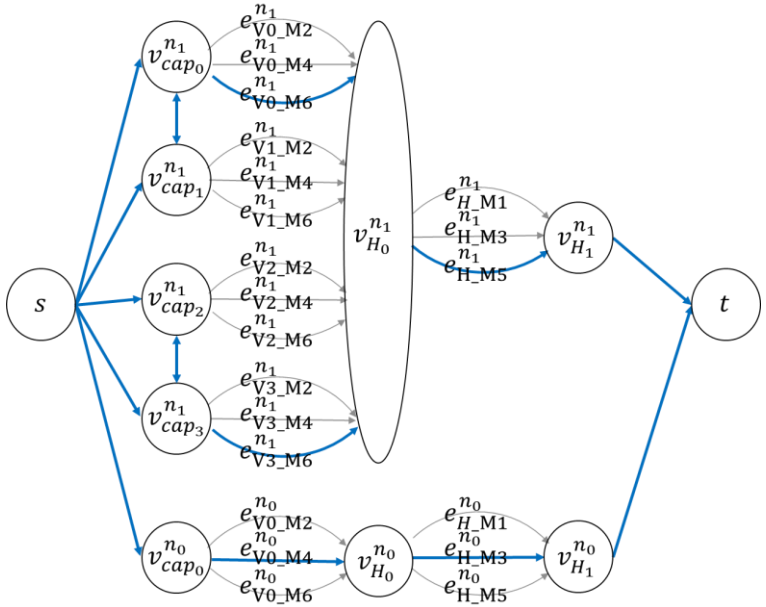
$$\sum_{e}^{gp_E} |e| \geq 1, \; gp_E \in GP_E$$

Parasitic-aware ILP-based Weight-Dynamic Network Routing Algorithm ($\alpha = 1$)



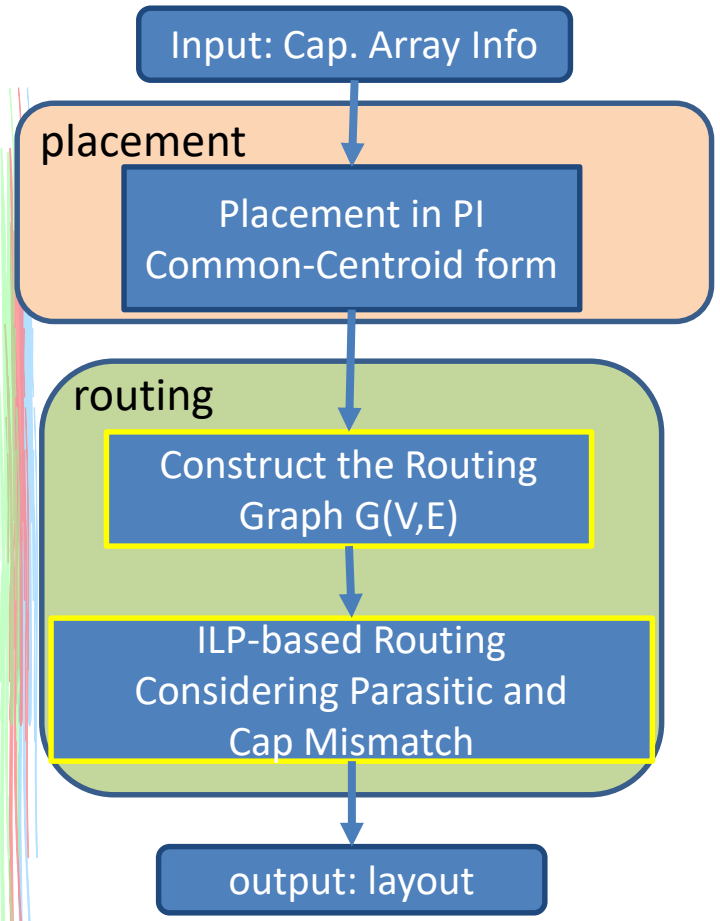
- Cost assignment and network construction
  - Transfer each pin and wire to node.





  - $\varphi = \sum_i^N \alpha * \widetilde{C}_i + \beta * \left|\widehat{C}_i - \widetilde{C}_i\right|$
  - where $\widehat{C}_i$ and $\widetilde{C}_i$ is the target and real capacitance.
  - $\widehat{C}_i = \widetilde{C_0} * r_i / r_0$
  - $\widetilde{C}_i = 2^{r_i - 1} * C_u + Cpara_i$

Parasitic-aware ILP-based Weight-Dynamic Network Routing Algorithm ($\alpha = 0.35$)



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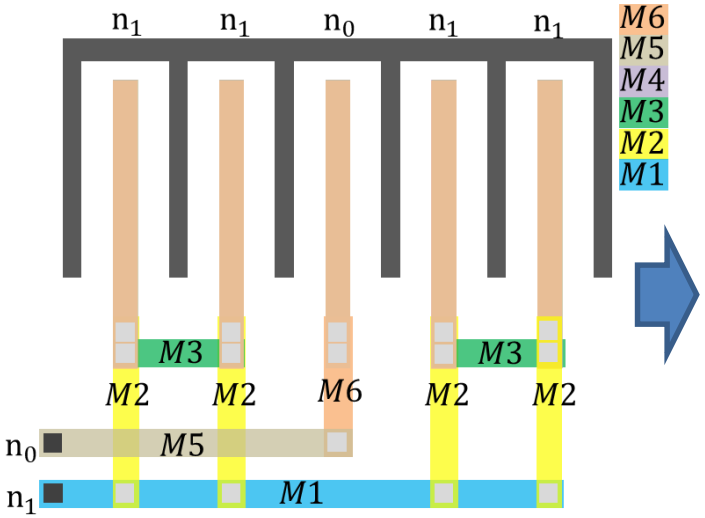

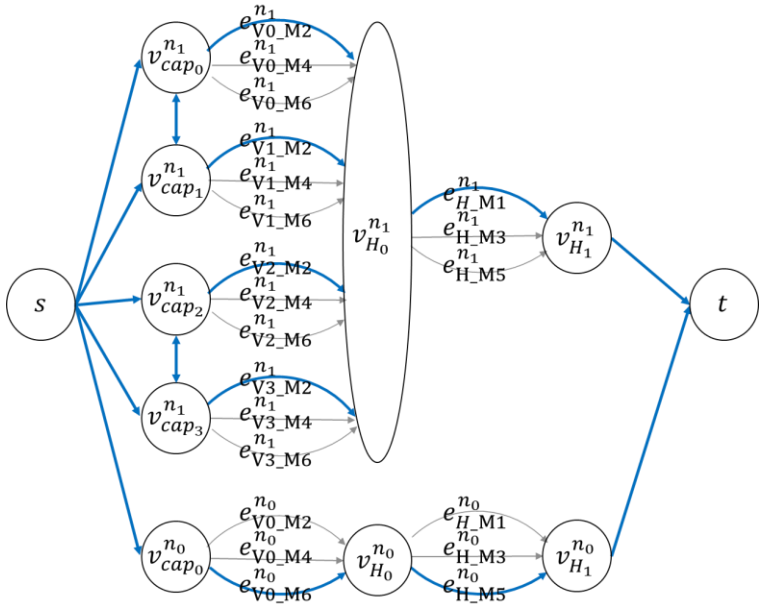

  - $\varphi = \sum_i^N \alpha * \widetilde{C}_i + \beta * \left|\widehat{C}_i - \widetilde{C}_i\right|$
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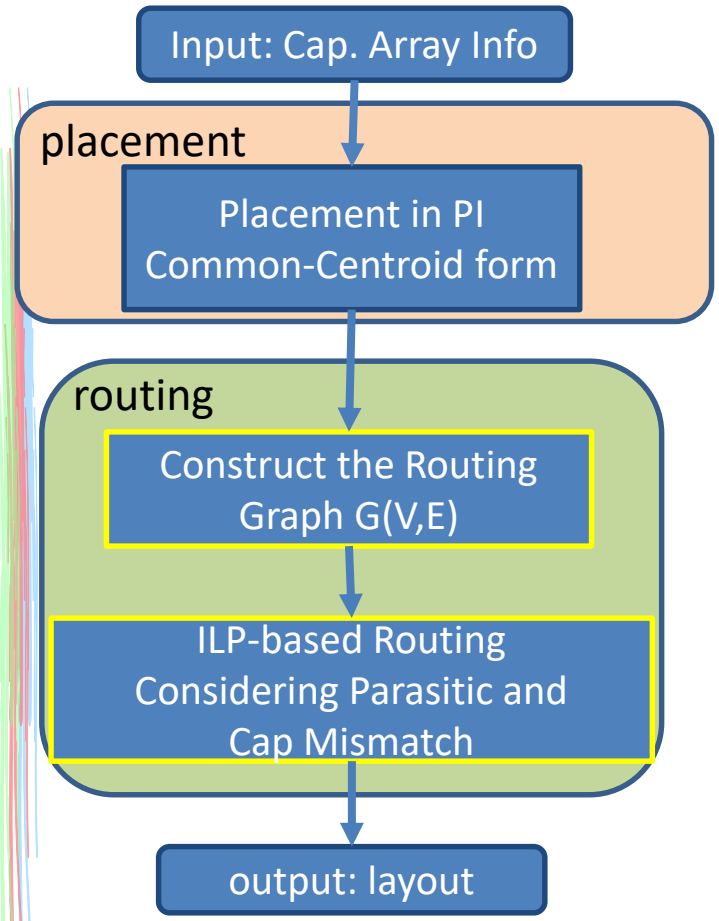
Objective and Constraint Functions for ILP



- The objective function of the ILP-based routing problem:
  - $$\varphi = \sum_{i}^{N} \alpha * \widetilde{C}_i + \beta * \left| \widehat{C}_i - \widetilde{C}_i \right|$$
  - $$Cpara_i = \sum_{e_i}^{E_i} C_{e_i} = \sum_{e_i}^{E_i} \sum_{j}^{N} \sum_{e_j}^{E_j} Cpara\left(e_k^i, e_l^j\right), \ when \ i \ != \ j.$$
  - $$Cpara\left(e_k^i, e_l^j\right) = \begin{cases} Cpara\_model\left(e_k^i, e_l^j\right), & \text{if } \sum_e \left|wall\left(e_k^i, e_l^j\right)\right| = 0 \text{ and } \left|e_k^i\right| + \left|e_l^j\right| = 2 \\ 0, & \text{otherwise} \end{cases}$$
- The constraint function of the ILP-based routing problem:
  - $$\sum_{e}^{gp_E} |e| \geq 1, \ gp_E \in GP_E$$

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Experiments

- Implement on 4-bit binary search SAR ADC
  - cap. ratio = 1:1:2:2:4:4
  - ideal ENOB = 4-bit
- The proposed algorithm can generate the layout with better ENOB
  - Considering the total cap. and cap. ratio mismatch

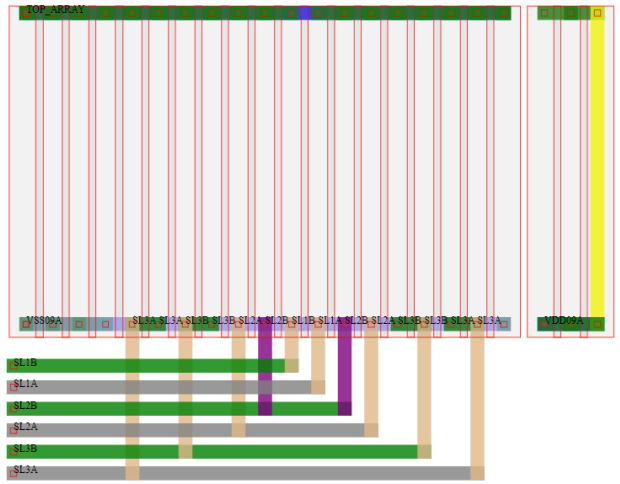
4-bit SAR ADC					
Approach	Total cap.	Interconnect C_{para}	Cap-Ratio Mismatch	ENOB (preSim: 3.4293)	Comparison
Manual	2.06e-14 fF	9.37e-15 (45.5%)	32.9% (avg=12%)	3.263 bits	–
Lin et al.'s approach [11]	1.83e-14 fF	7.3e-15 (39.4%)	30.2% (avg=9.63%)	3.374 bits	15.1%
Ho et al.'s approach [9]	1.97e-14 fF	8.46e-15 (43%)	24.2% (avg=8.5%)	3.342 bits	10.8%
Our approach	1.79e-14 fF	6.7e-15 (38.4%)	9.96% (avg=3.46%)	3.429 bits	22.5%
Our approach only considering total cap.	1.67e-14 fF	5.51e-15 (33%)	34.2% (avg=13.3%)	3.363 bits	13.6%

[8] M. P.-H. Lin, V. W.-H. Hsiao, C.-Y. Lin, and N.-C. Chen, "Parasitic-aware common-centroid binary-weighted capacitor layout generation integrating placement, routing, and unit capacitor sizing," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 36, no. 8, pp. 1274–1286, 2017.
[12] K.-H. Ho, H.-C. Ou, Y.-W. Chang, and H.-F. Tsao, "Coupling-aware length-ratiomatching routing for capacitor arrays in analog integrated circuits," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 34, no. 2, pp. 161–172, 2015.

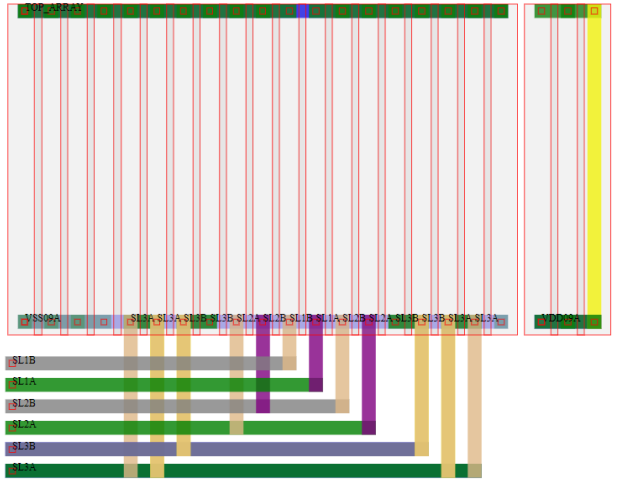
Experiments

- Although (a) has lowest total cap., the layout (b) with considering both total cap. and cap. ratio shows better ENOB result

4-bit SAR ADC					
Approach	Total cap.	Interconnect C_{para}	Cap-Ratio Mismatch	ENOB (preSim: 3.4293)	Comparison
Manual	2.06e-14 fF	9.37e-15 (45.5%)	32.9% (avg=12%)	3.263 bits	–
Lin et al.'s approach [11]	1.83e-14 fF	7.3e-15 (39.4%)	30.2% (avg=9.63%)	3.374 bits	15.1%
Ho et al.'s approach [9]	1.97e-14 fF	8.46e-15 (43%)	24.2% (avg=8.5%)	3.342 bits	10.8%
Our approach	1.79e-14 fF	6.7e-15 (38.4%)	9.96% (avg=3.46%)	3.429 bits	22.5%
Our approach only considering total cap.	1.67e-14 fF	5.51e-15 (33%)	34.2% (avg=13.3%)	3.363 bits	13.6%



(a) Only minimum $\widetilde{C}_i$



(b) Considering cap ratio matching

Outline

- Introduction
- Problem Formulation
- Proposed Method
- Experiments
- Conclusion

Conclusion

- We present a framework to synthesize binary-weighted capacitors in the structure of Finger-Cap-Array.
  - The partially interdigitated common-centroid placement is presented to generate a placement result considering the parasitic effect and the process-gradient-induced mismatch.
  - The parasitic-aware ILP-based weight-dynamic network routing algorithm is performed to finish the connectivity for all net simultaneously as well as minimize the parasitic capacitance and capacitance ratio mismatch with the proposed objective function and constraints

Thank you