An Integrated Circuit Partitioning and TDM Assignment Optimization Framework for Multi-FPGA Systems

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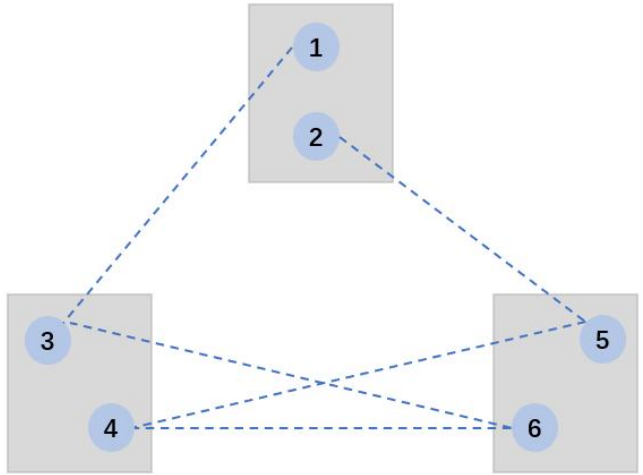
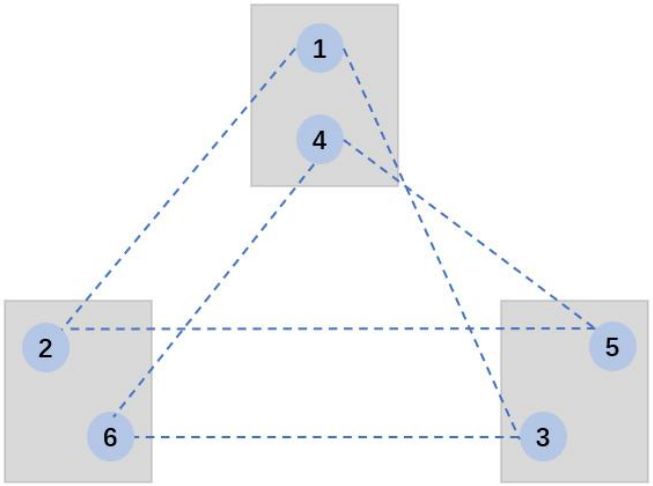
Motivations

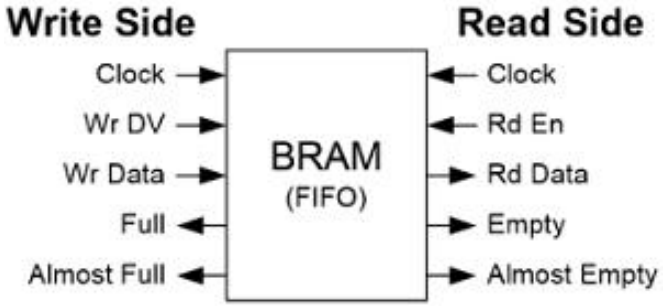


(a)



(b)

Multi-Clock



TDM Ratio

Maximum number of signals that a physical wire accommodates

Multiples of TDM ratio step

https://nandland.com/articles/images/block-ram-fifo.png
https://ignitarium.com/wp-content/uploads/2022/06/image-1.jpeg
https://ignitarium.com/wp-content/uploads/2022/06/image-1.png

Problem Formulation

- a circuit graph $G(V, E)$
- a set F of FPGA nodes
- a set of clocks C
- a set of fixed nodes $V\gamma$ ($V\gamma \subset V$)
- TDM ratio step s

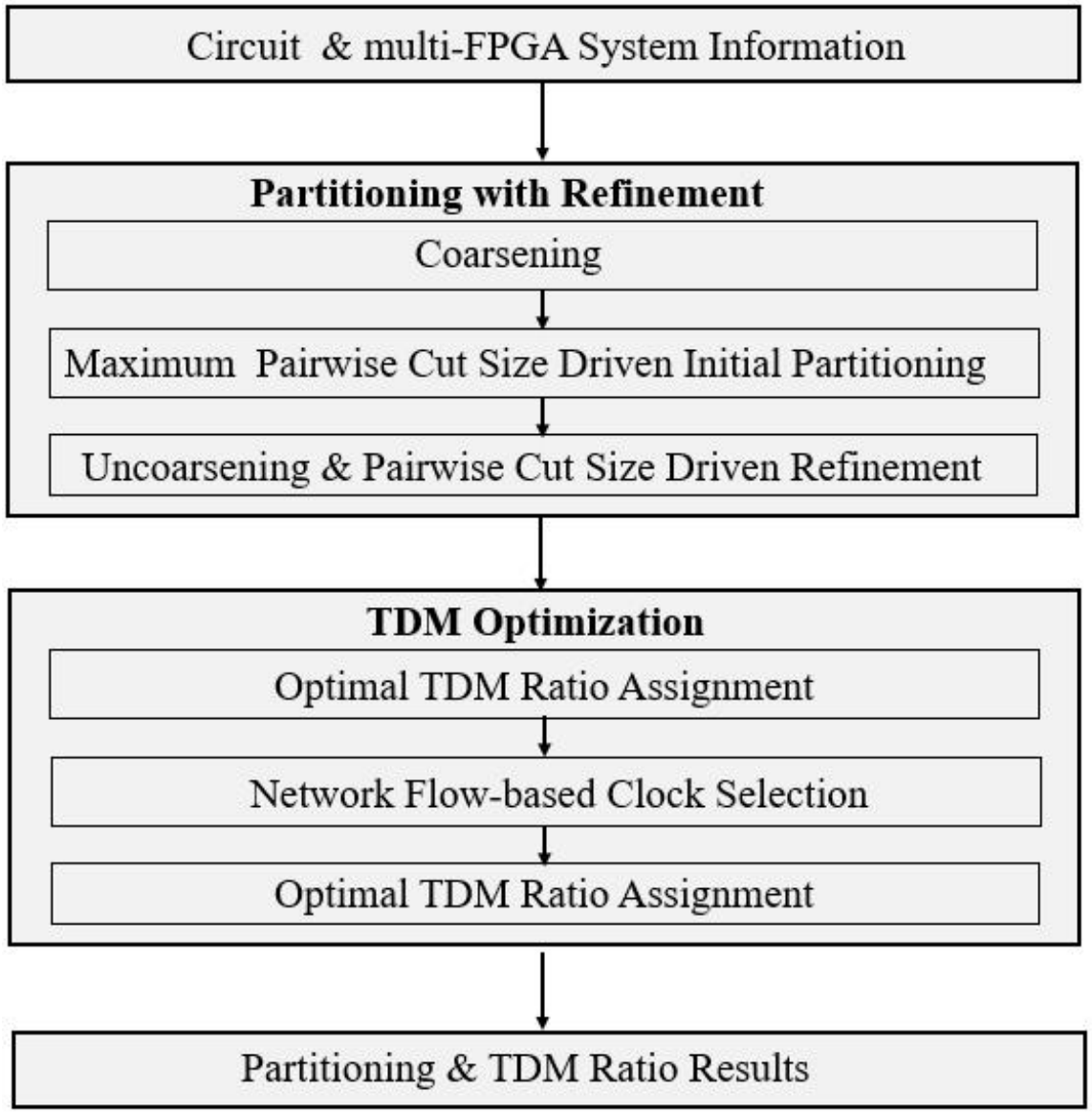
Objective:

- Find a partitioning P
- Minimize the maximum TDM ratio

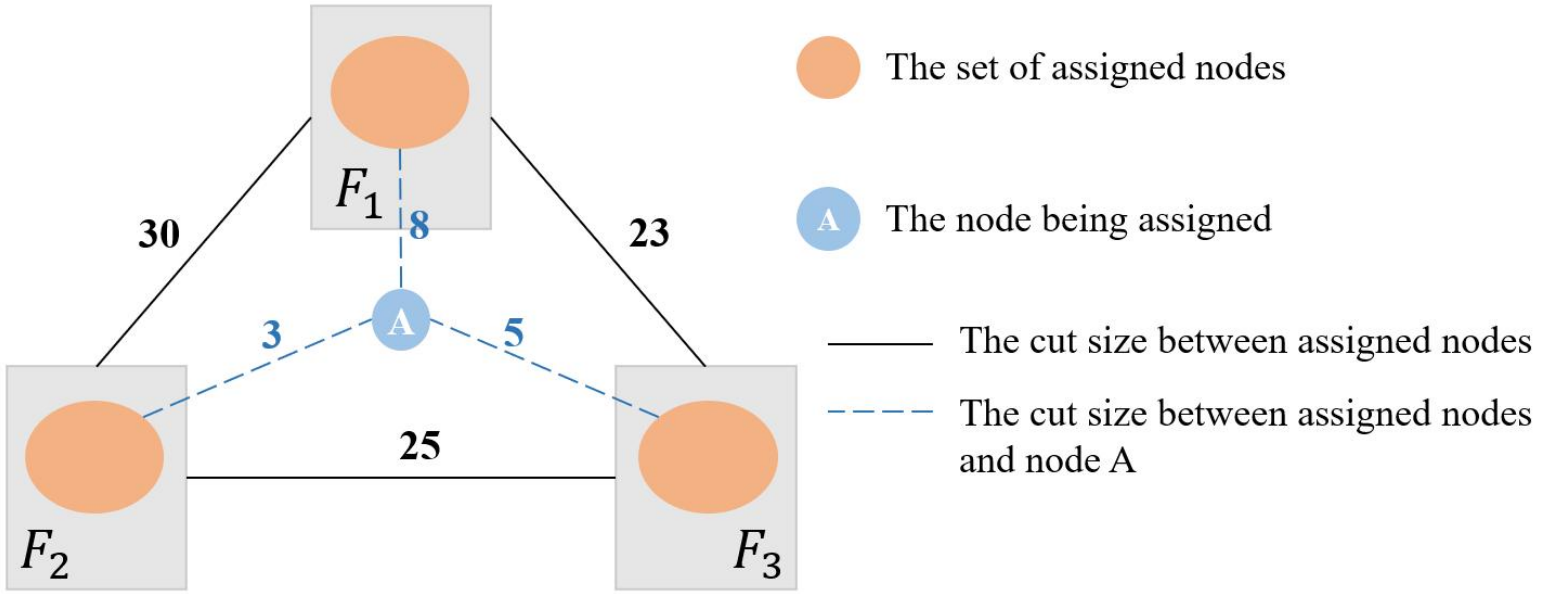
Constraints:

- Each fixed node is assigned to its corresponding FPGA
- TDM ratio t is a multiple of s
- Only inter-FPGA nets, either driven by the same clock or not driven by any clock, with the same TDM ratio in the same direction can be assigned to the same wire;
- If an inter-FPGA net is driven by a clock group, one clock c_i among them should be selected

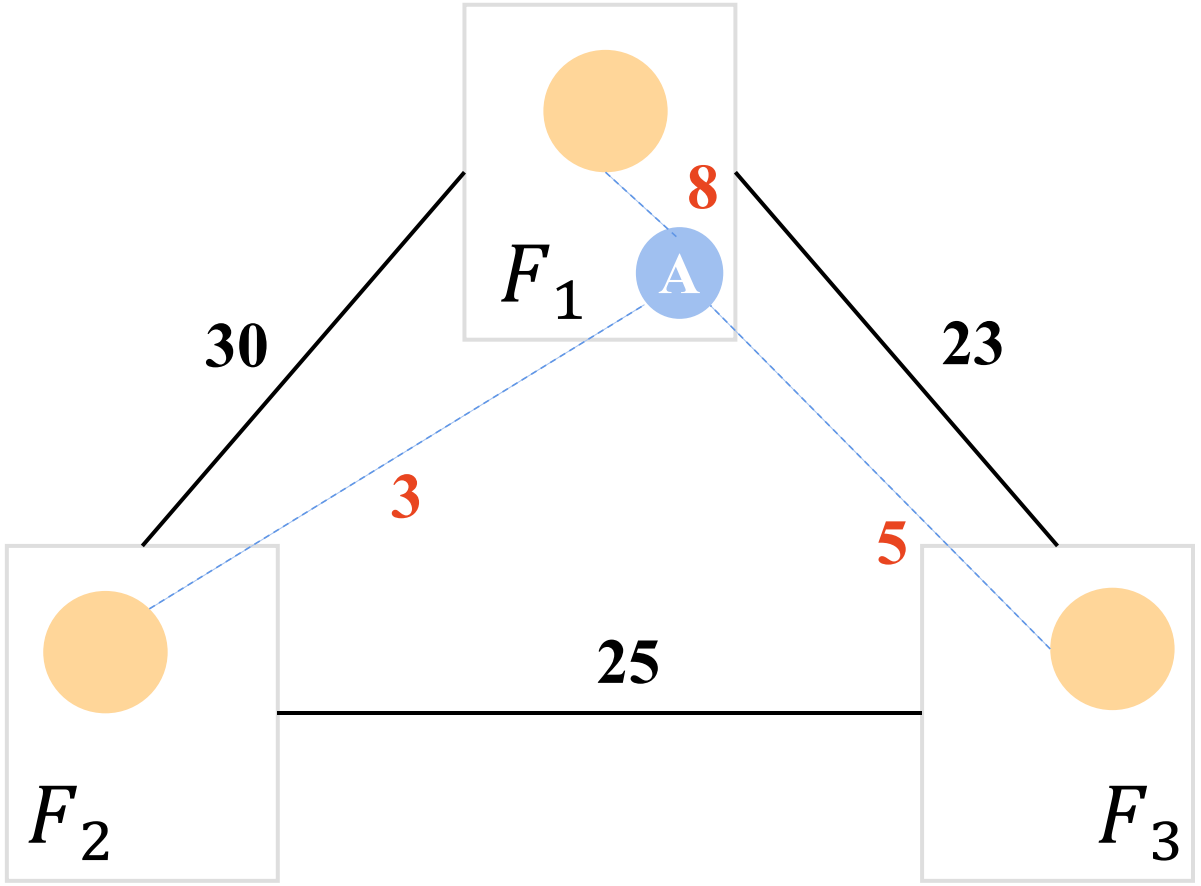
Algorithm Flow



Pairwise Cutsize Initial Partitioning



Initial Partitioning

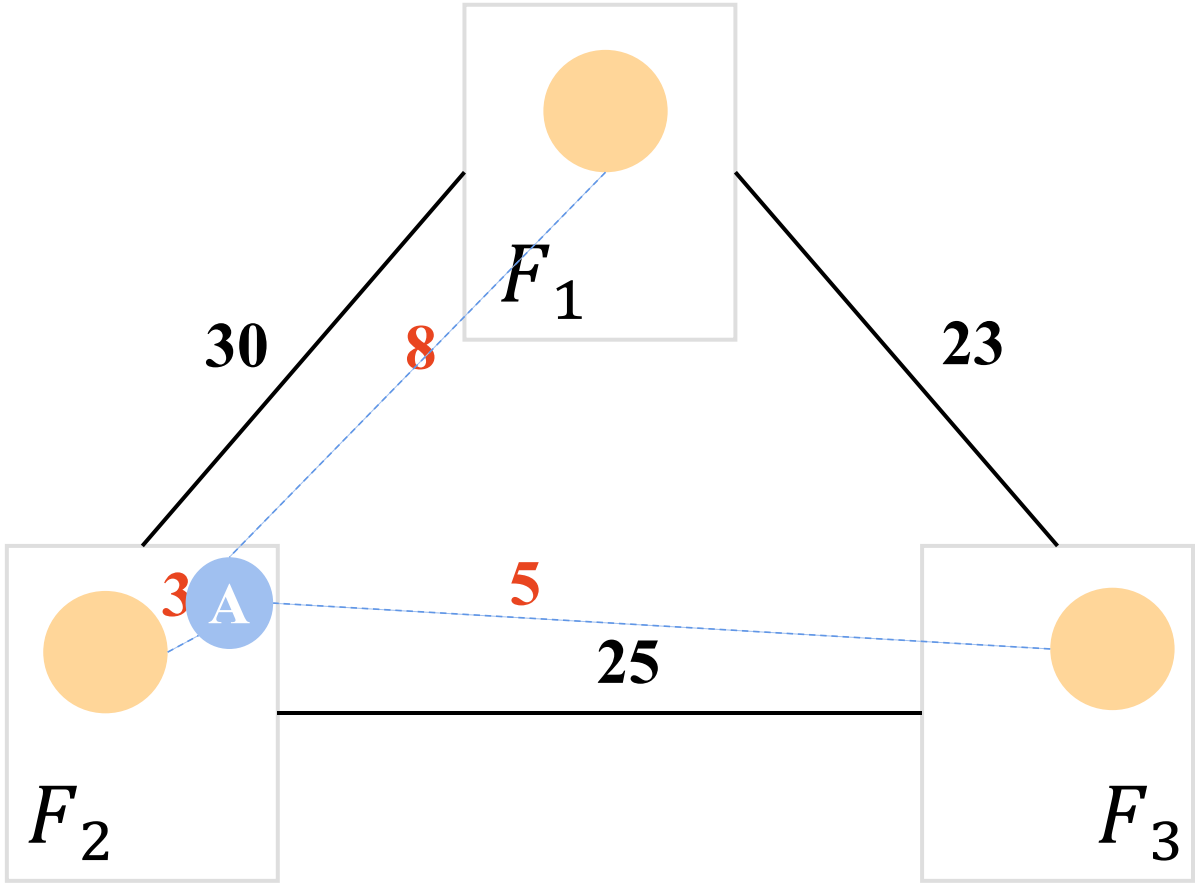


- Assign Node A to FPGA F_1

FPGA Pair	Cut Size
F_1F_2	33
F_1F_3	28
F_2F_3	25

FPGA	Maximum Cut Size
F_1	33
F_2	
F_3	

Initial Partitioning

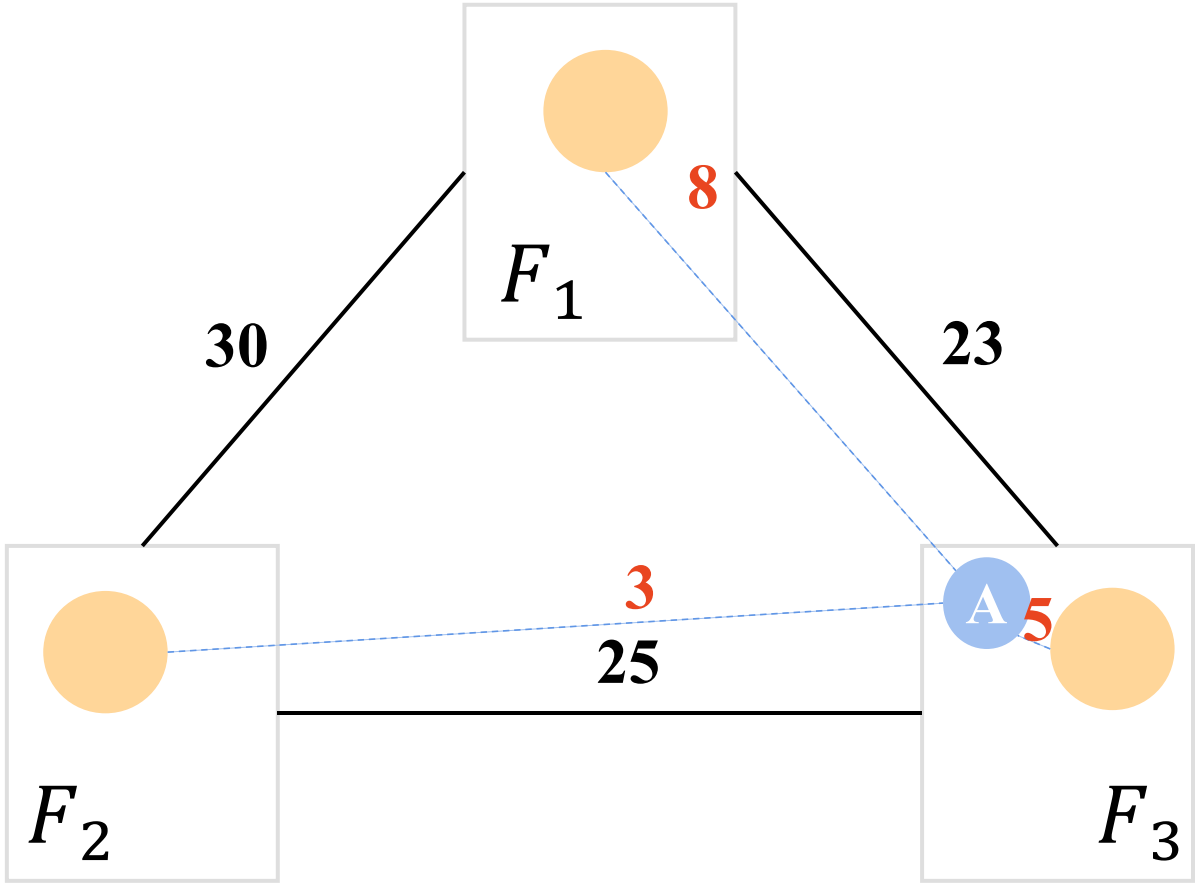


- Assign Node A to FPGA F_2

FPGA Pair	Cut Size
F_1F_2	38
F_1F_3	23
F_2F_3	30

FPGA	Maximum Cut Size
F_1	33
F_2	38
F_3	

Initial Partitioning

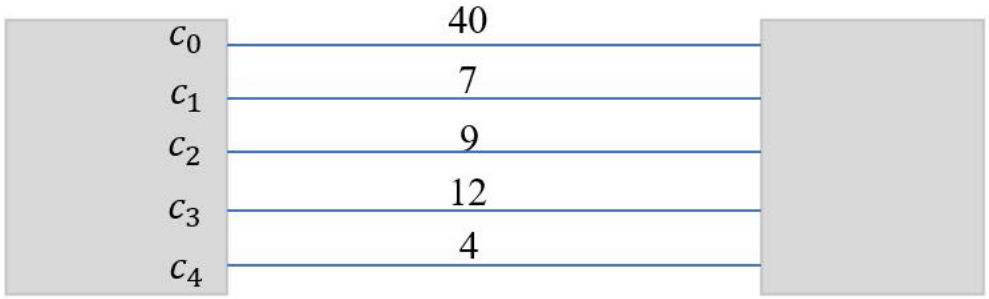


- Assign Node A to FPGA F_3

FPGA Pair	Cut Size
F_1F_2	30
F_1F_3	31
F_2F_3	28

FPGA	Maximum Cut Size
F_1	33
F_2	38
F_3	31

Optimal TDM Initial Assignment



physical wires: 10

TDM Ratio step: 2

Lower bound: $\left\lceil \frac{72}{2*10} \right\rceil * 2 = 8$

Expected wire number: 5.56, 0.97, 1.25, 1.67, 0.55

Updated expected wire number: 5.25, 1.18 , 1.57

Upper bound: $\max\left\{\left\lceil \frac{40}{\lfloor 5.25 \rfloor * 2} \right\rceil * 2, \left\lceil \frac{9}{\lfloor 1.18 \rfloor * 2} \right\rceil * 2, \left\lceil \frac{12}{\lfloor 1.57 \rfloor * 2} \right\rceil * 2\right\} = 12$

The optimal TDM ratio $t_{opt} = 10$

Clock Selection

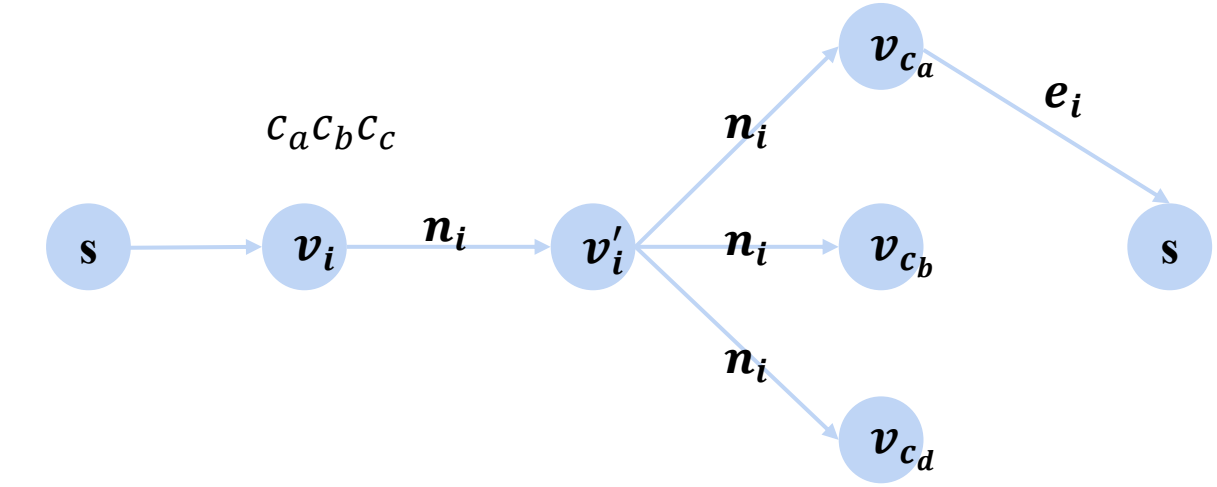
Occupied

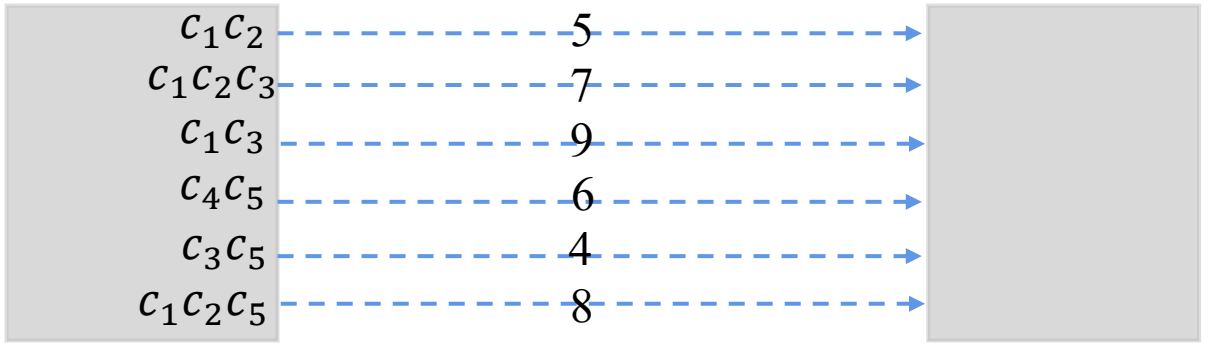
Empty

Objective:

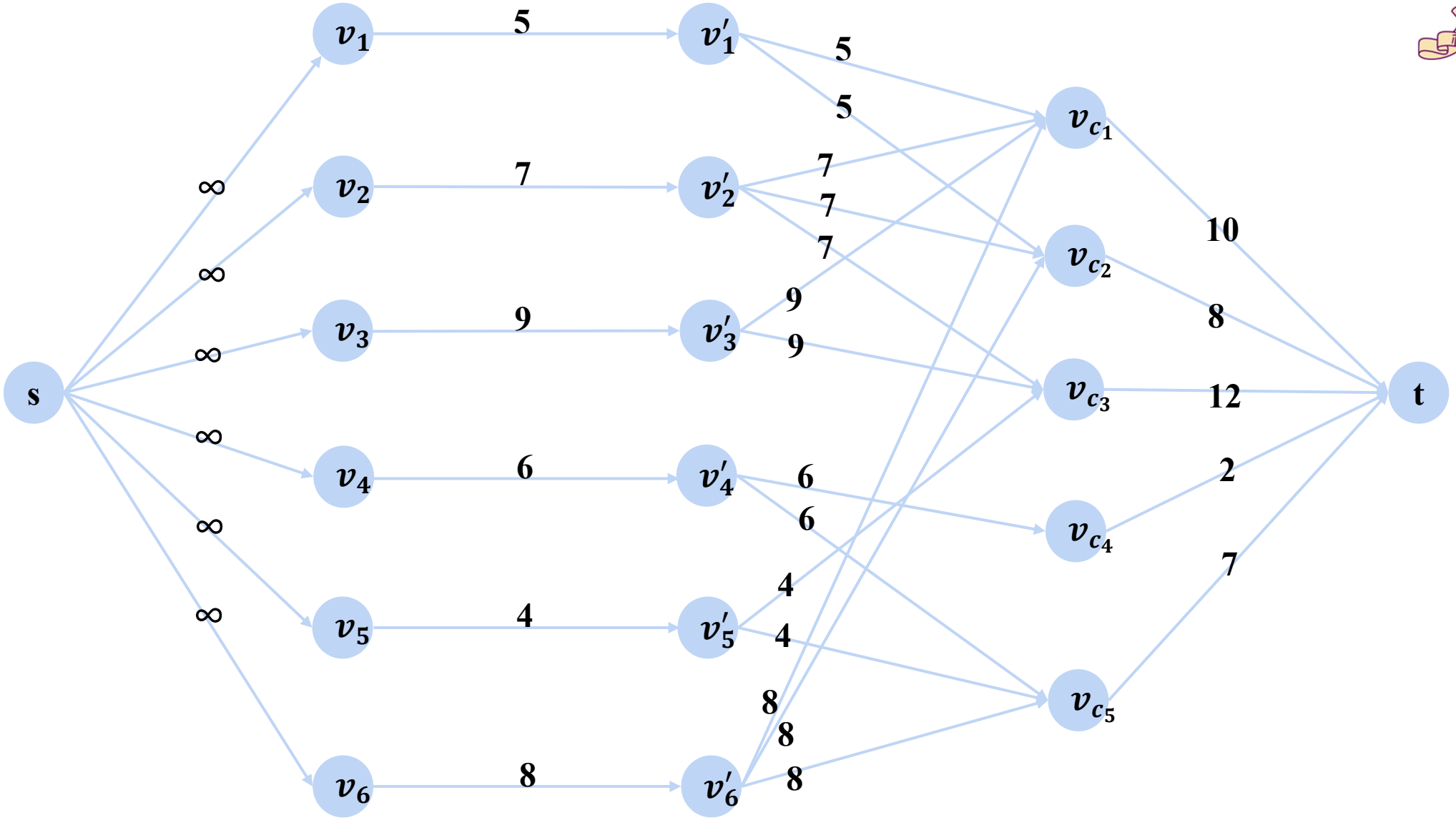
Minimize the increment of t_{opt}

Clock Selection

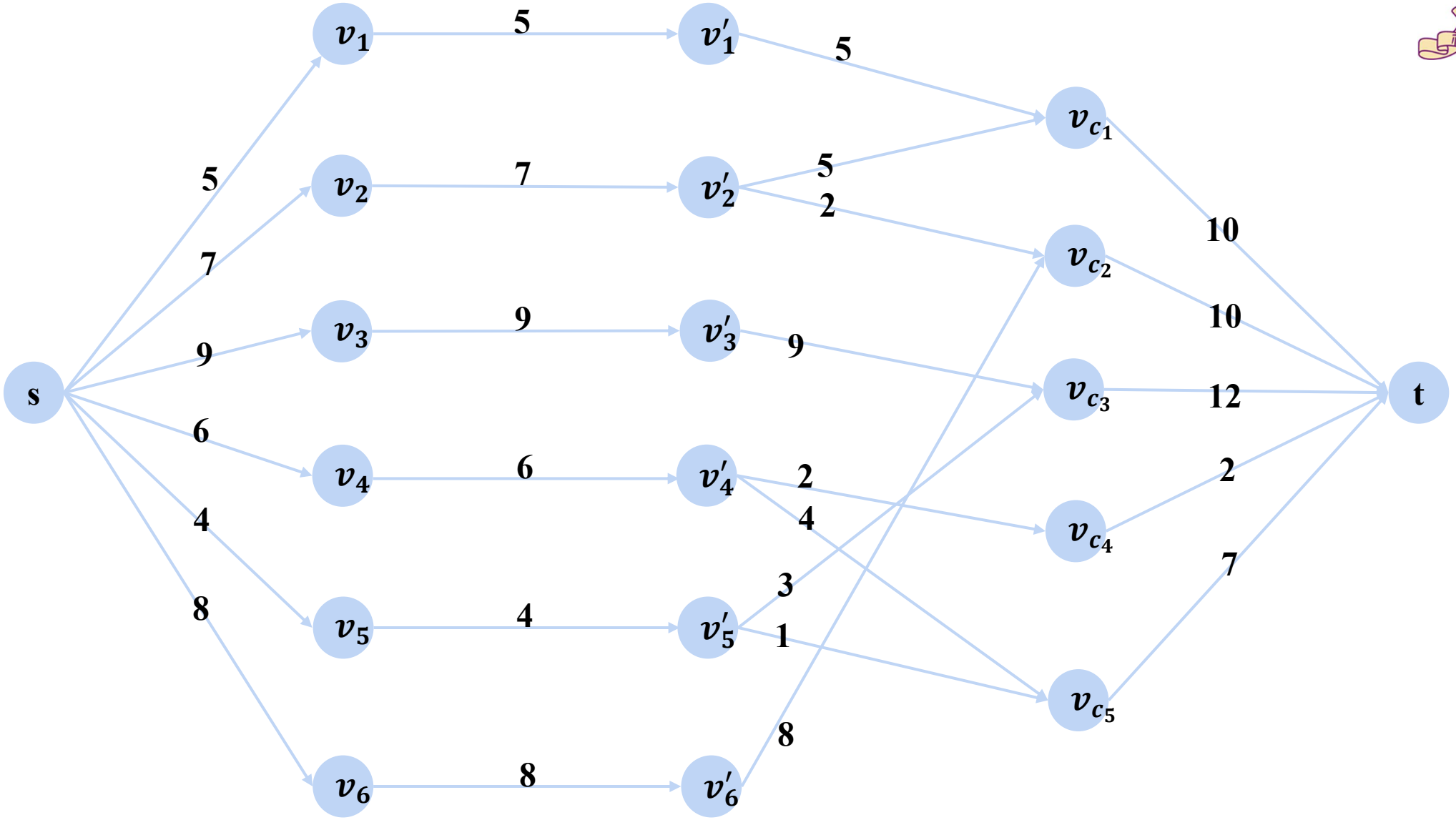




Clock Selection



Clock Selection



Experimental Results

Benchmark	PaToH + TDM Optimization					Ours				
	Max. Cut Size	Ratio	Max. TDM Ratio	Ratio	Time (s)	Max. Cut Size	Ratio	Max. TDM Ratio	Ratio	Time (s)
sparcT1_core	14715	1.0	972	1.0	2.200	12532	0.852	826	0.850	8.887
neuron	29210	1.0	1948	1.0	1.650	16076	0.550	1048	0.538	6.174
stereo_vision	14442	1.0	916	1.0	1.464	9854	0.682	624	0.681	6.667
des90	21491	1.0	1380	1.0	4.023	17935	0.835	1040	0.754	8.094
SLAM_spheric	7949	1.0	456	1.0	3.085	6480	0.815	400	0.877	6.472
cholesky_mc	42941	1.0	2992	1.0	2.220	21494	0.501	1396	0.467	7.951
segmentation	6079	1.0	348	1.0	3.153	4937	0.812	280	0.805	6.553
bitonic_mesh	46826	1.0	2980	1.0	6.385	33235	0.710	1892	0.635	14.035
openCV	34615	1.0	2256	1.0	4.793	28379	0.820	1761	0.781	17.250
stap_qrd	84498	1.0	5916	1.0	6.709	32073	0.380	2130	0.360	14.275
minres	56356	1.0	3576	1.0	6.531	18362	0.326	1084	0.303	12.862
cholesky_bdti	91666	1.0	6468	1.0	7.810	47607	0.519	3100	0.479	17.433
denoise	7311	1.0	420	1.0	6.458	6893	0.943	412	0.981	11.110
sparcT2_core	35410	1.0	2476	1.0	9.732	46360	1.309	2974	1.201	28.808
gsm_switch	119146	1.0	7376	1.0	15.319	110236	0.925	7324	0.993	49.960
mes_noc	134744	1.0	7863	1.0	18.425	64957	0.482	4341	0.552	33.784
LU230	140484	1.0	8276	1.0	20.333	124392	0.885	7160	0.865	58.174
LU_Network	110819	1.0	7328	1.0	24.942	84041	0.758	5384	0.735	54.447
sparcT1_chip2	118484	1.0	8188	1.0	40.648	92317	0.779	6072	0.742	65.728
directrf	228031	1.0	15789	1.0	22.743	113093	0.496	7587	0.481	56.132
bitcoin_miner	227944	1.0	14872	1.0	45.072	121119	0.531	7848	0.528	83.550
Avg. Ratio	1.0	1.0	1.0	1.0	1.0	0.710	0.710	0.696	0.696	2.619

Conclusion

Partitioning

- Maximum pairwise cut size driven partitioning algorithm

TDM assignment

- Network flow-based clock selection approach
- Binary search based TDM optimization algorithm