CompaSeC: A Compiler-assisted Security Countermeasure to Address Instruction Skip Fault Attacks on RISC-V

J. Geier[1], L. Auer[2], D. Mueller-Gritschneder[1], U. Sharif[1], and U. Schlichtmann[1]
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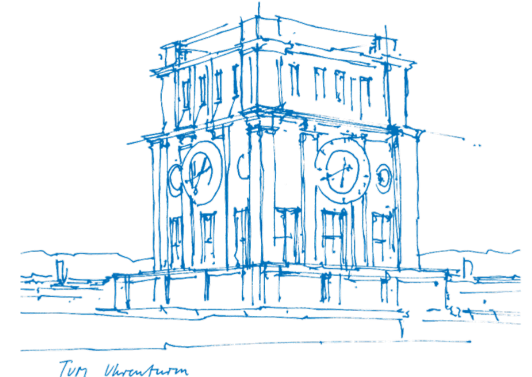
ASIA SOUTH PACIFIC DAC DESIGN AUTOMATION CONFERENCE



Outline

1. Motivation

2. Compiler-assisted Countermeasures Against Instruction Skip Fault Attacks

3. Evaluation and Performance Results

4. Conclusion

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Software Implemented Hardware Fault Tolerance

Fault Model

Exploit		Bypass Secure Boot: Boot unverified software image
Manifestation	**Instruction Set Architecture**	Instruction corruption
		Architectural state corruption
		Memory op. corruption
	Imple-mentation	µArch register corruption
		Logic state corruption
Physical Attack		Optical/Laser Fault (LFI)
		Clock/Voltage Glitch

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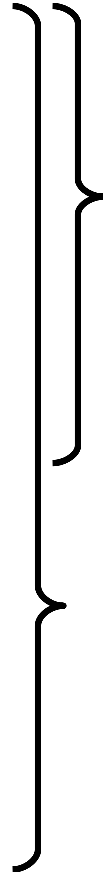

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- additional hardware
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Source Level

- Target (ISA) independent
- Algorithm dependent

Example:

- Algorithm re-execution

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Instruction-level

- Target dependent, e.g. RISC-V
- Algorithm independent

Examples:

- Instruction re-execution
- Dual module redundancy (DMR)
- Runtime signature monitoring (RSM)

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CompaSeC Framework

- Source code agnostic

```
if(a == 0) {
    ... // taken
} else {
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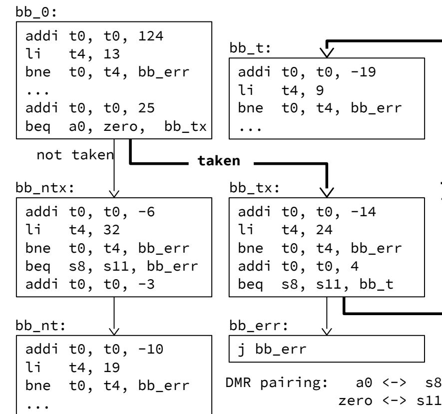
Source Code Project (.h/.c/.cpp)



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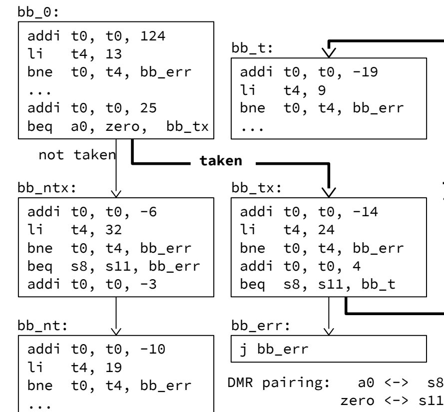
LLVM Compiler Frontend

LLVM IR

hardened object code (.asm)



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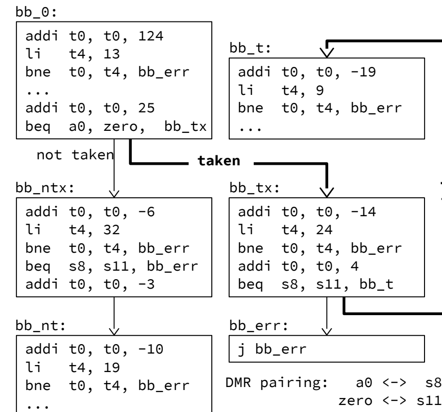

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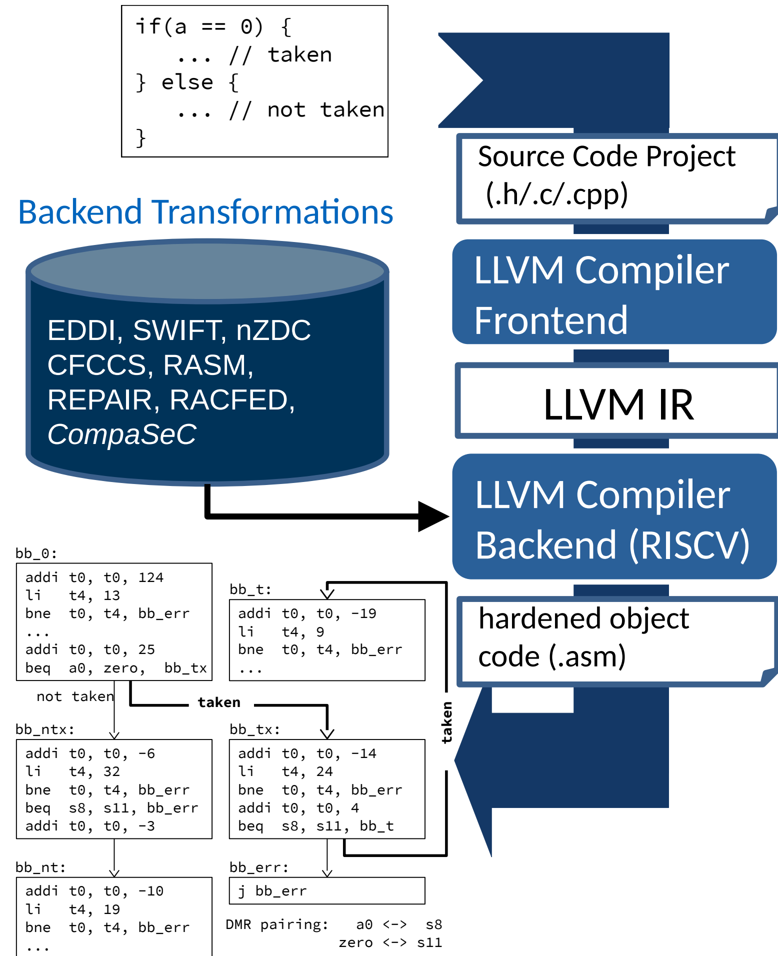

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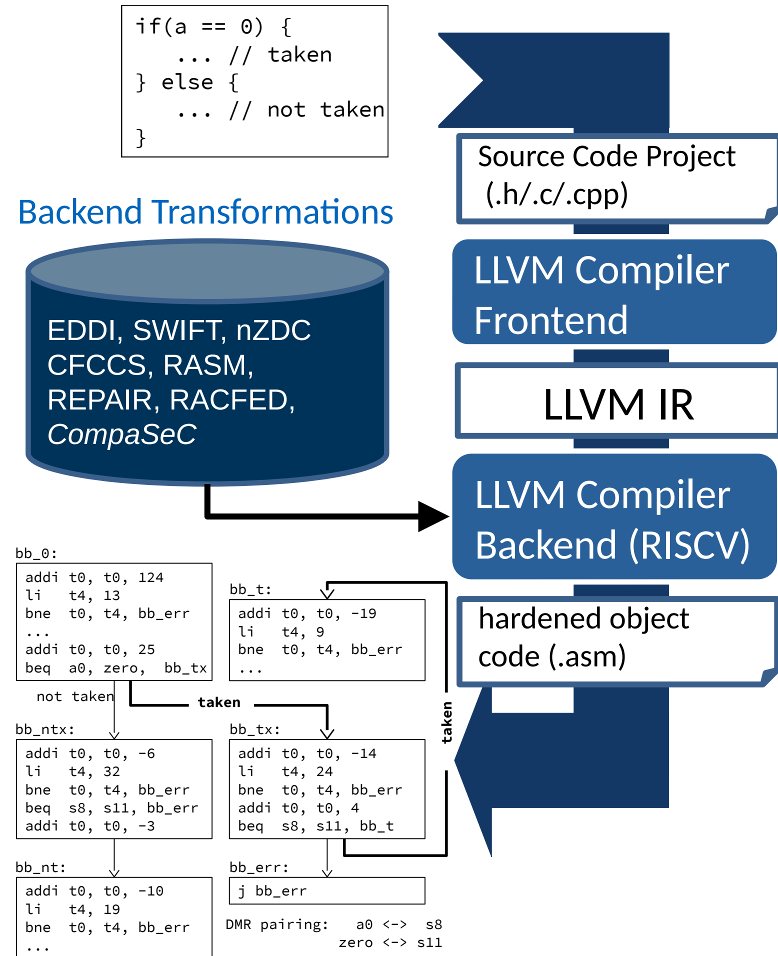
- **CompaSeC**: **Combination** of existing methods to eliminate Instruction Skip Faults in RISC-V



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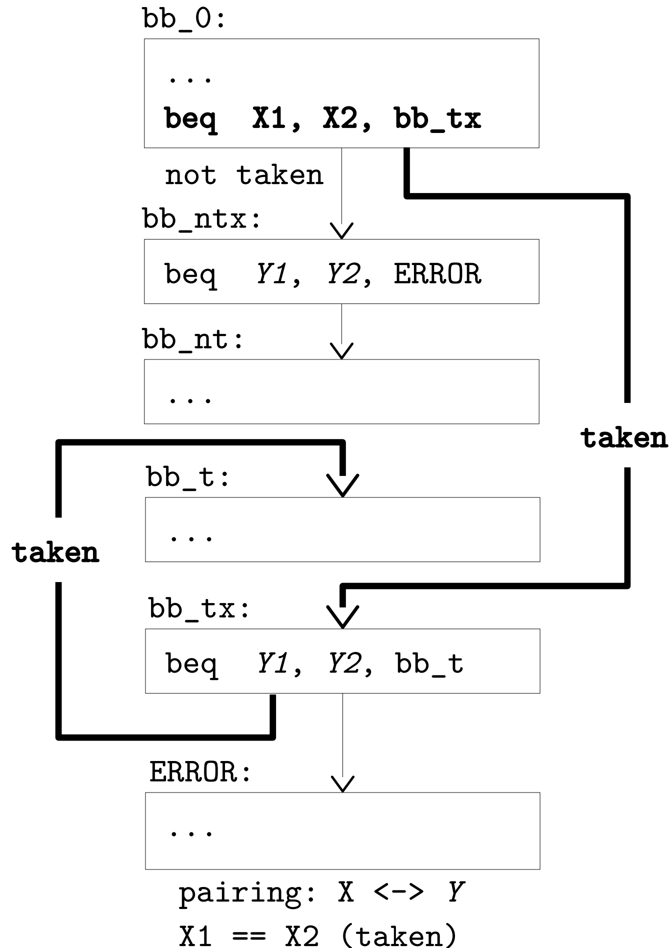
3. **Verification** in Secure Boot Scenario

Dual Module Redundancy (DMR) Transformation



(DMR): nZDC+NEMESIS [2, 3]

1. Reserve half of ISA register file
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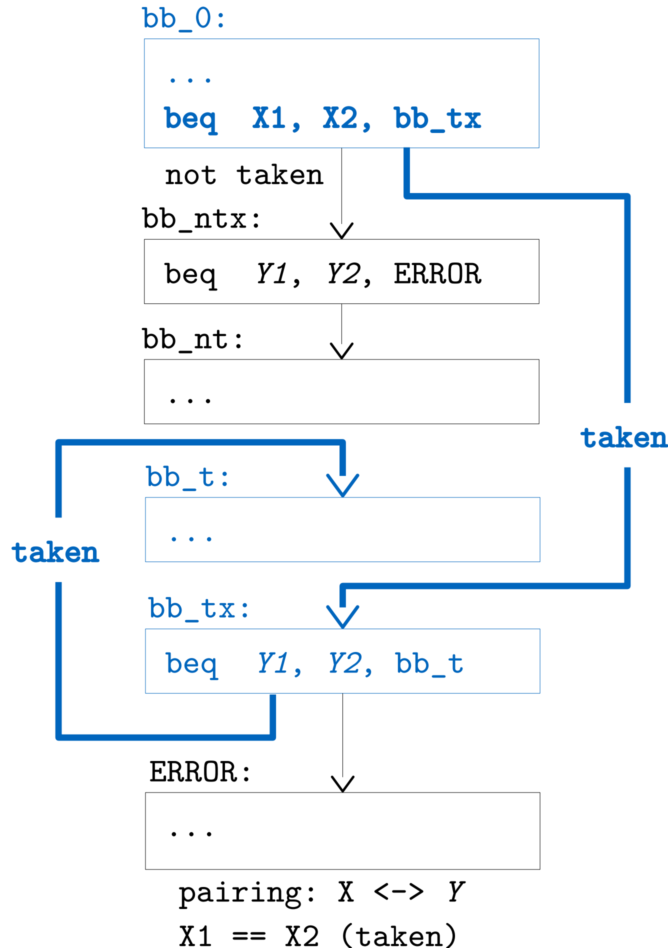

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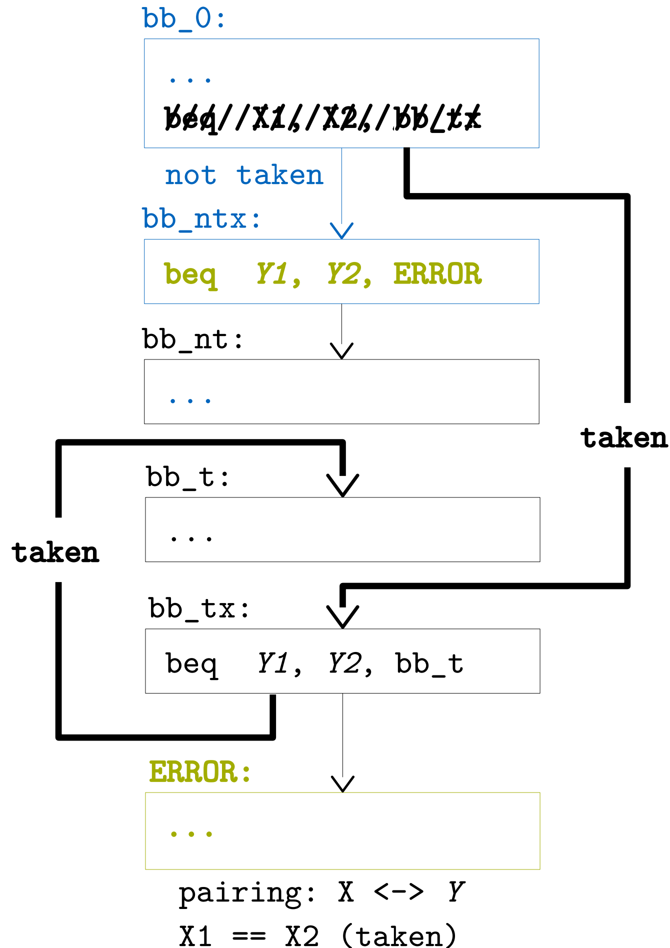

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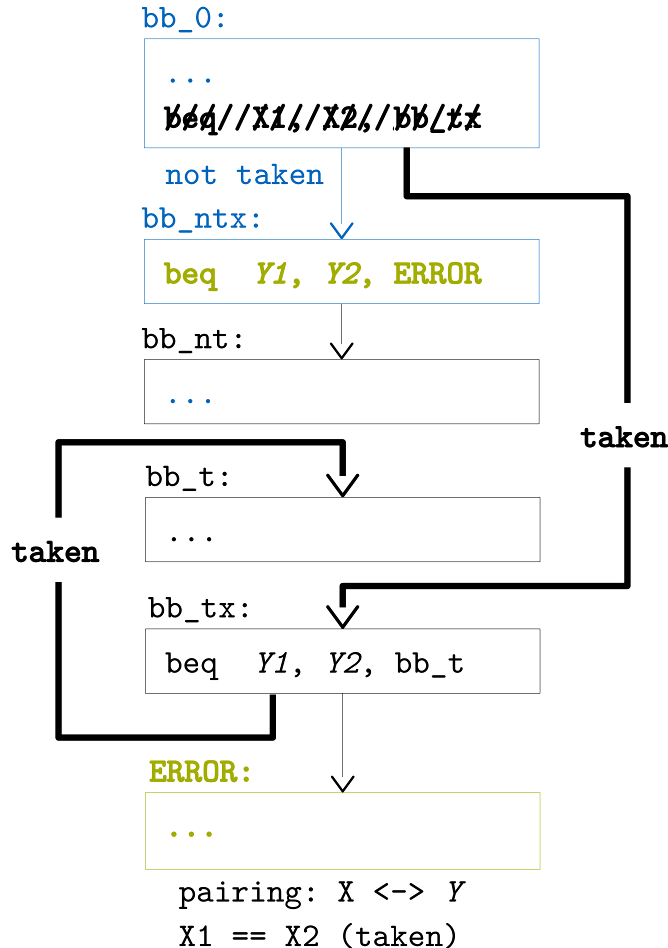

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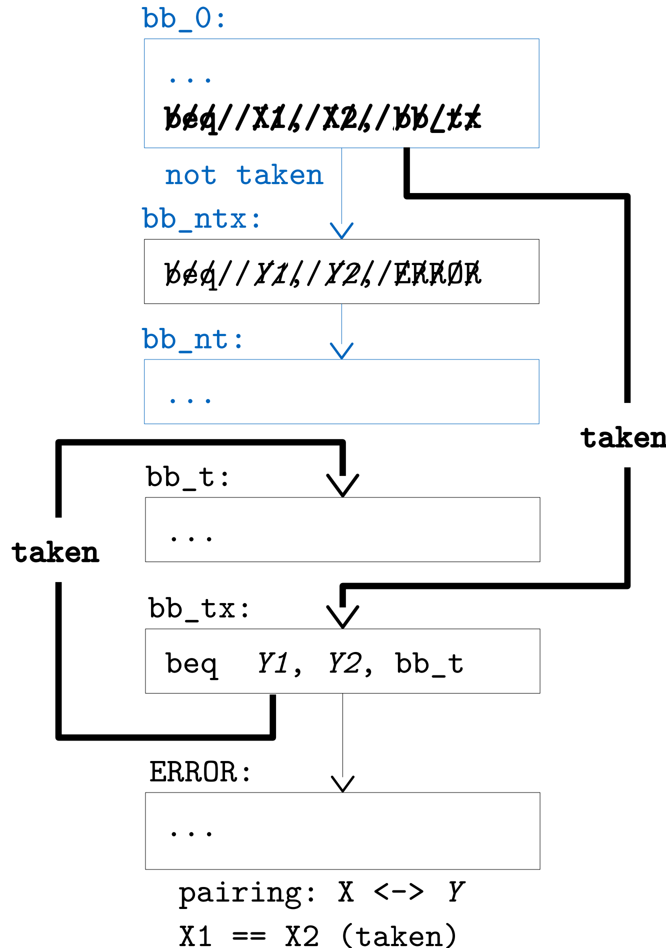

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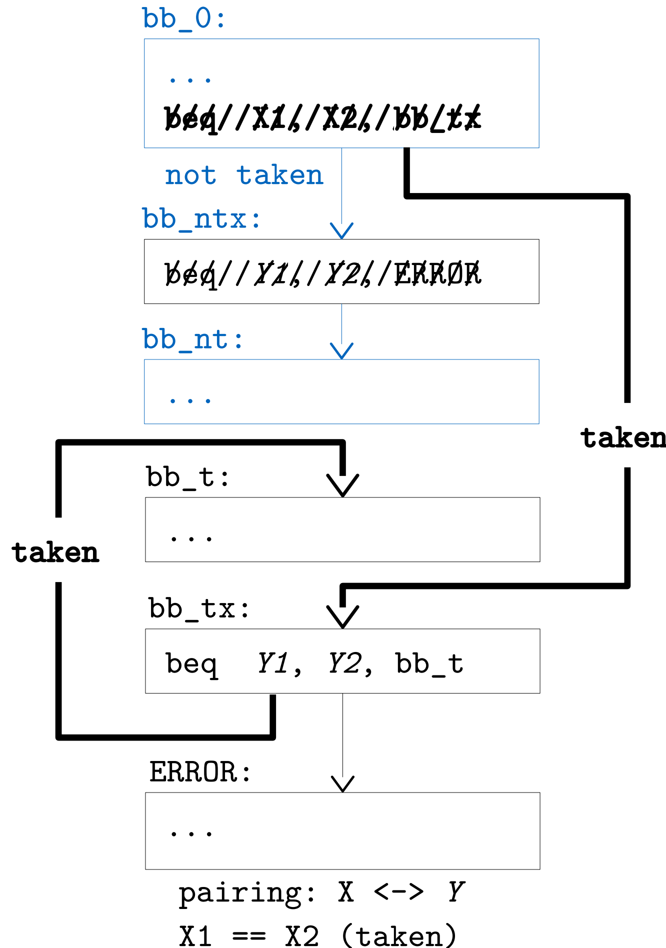

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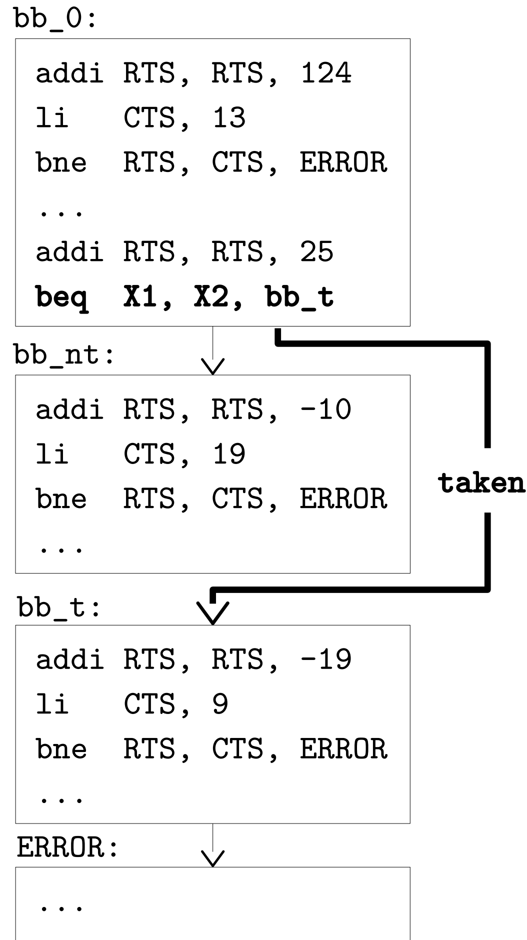
Runtime Signature Monitoring (RSM) Transformation



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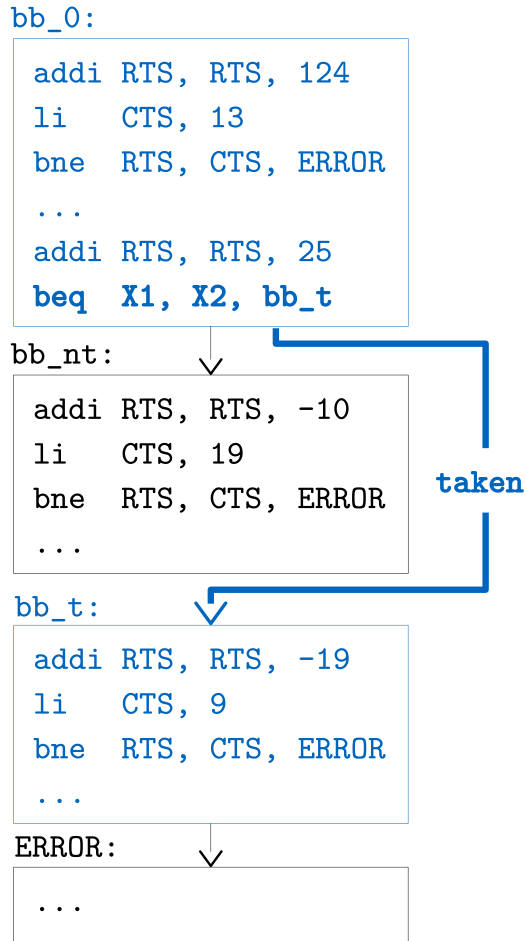

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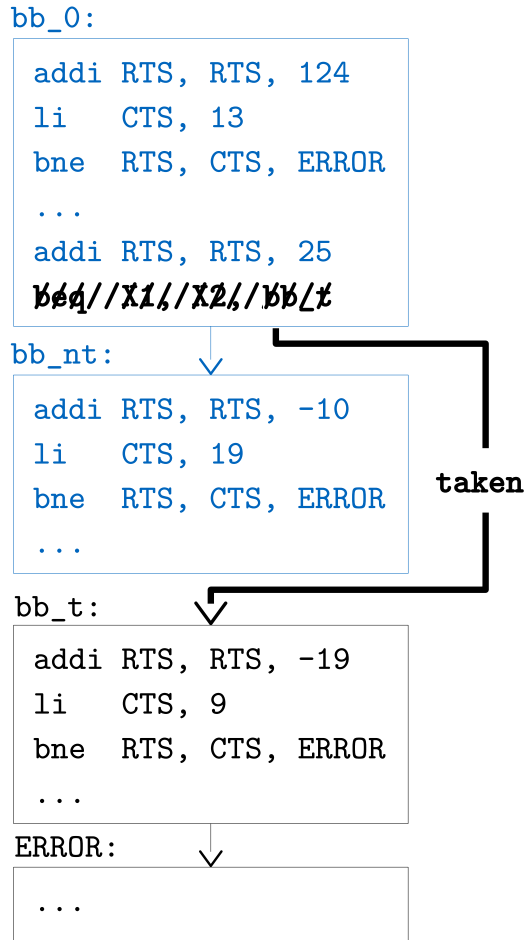

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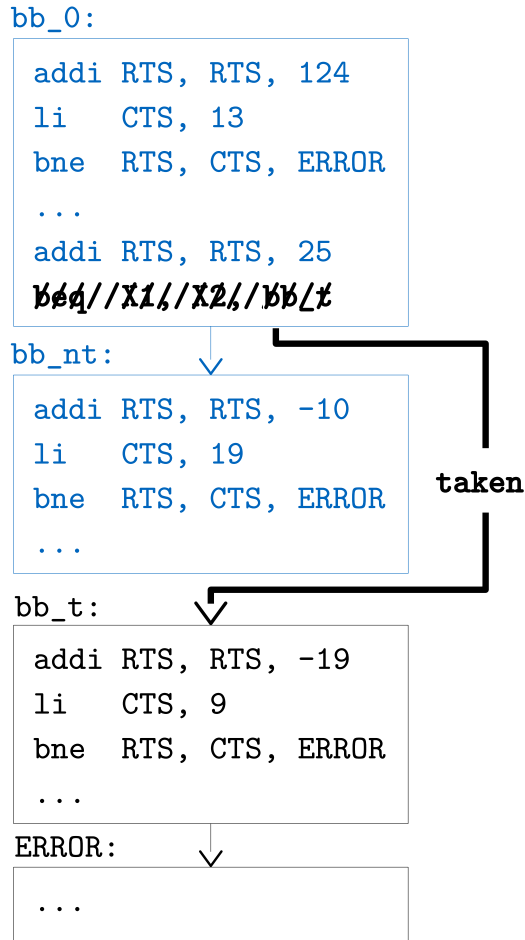

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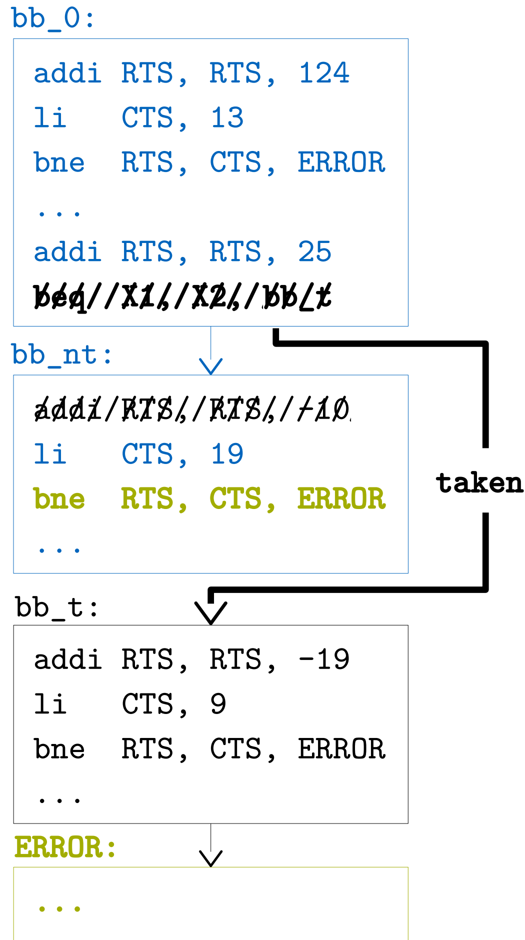

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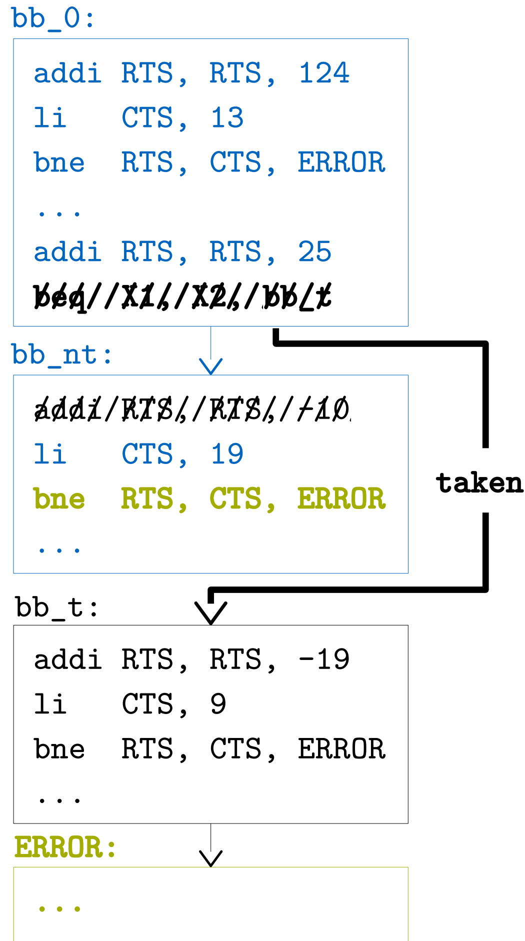

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   - ▶ Control Flow Checks CTS==RTS

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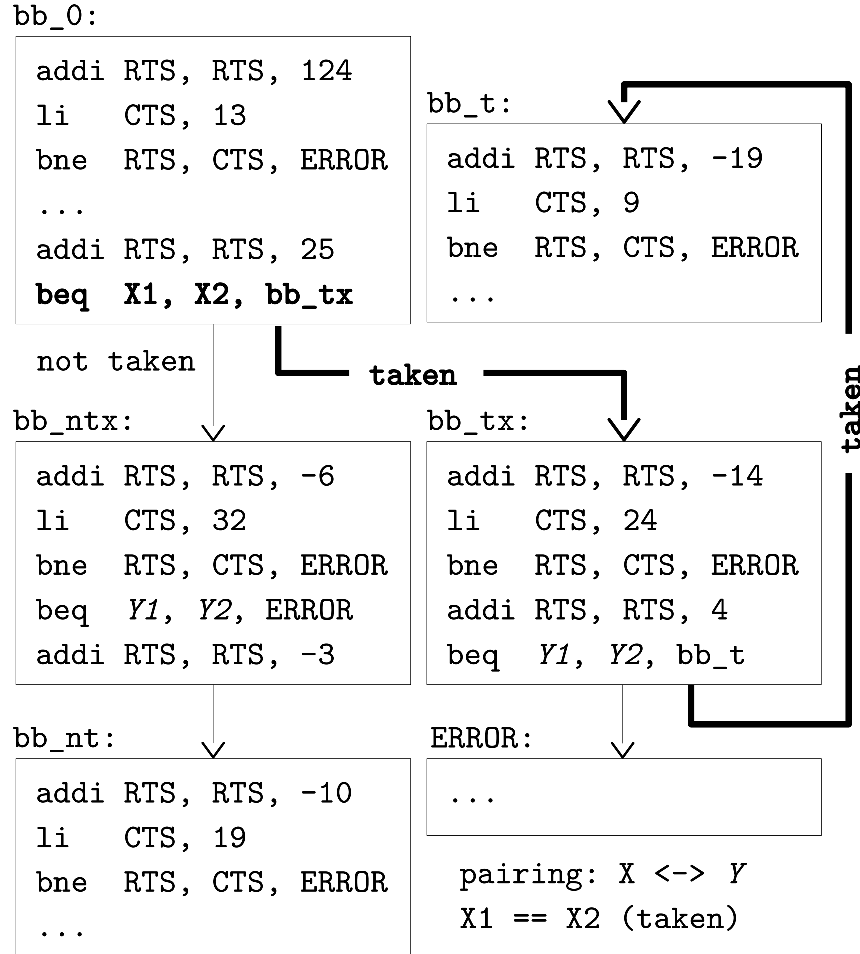
- Multi Instruction Skips
  - ▶ detect Breaks gradual runtime signature
    Trips ERROR with next check

Combining DMR and RSM



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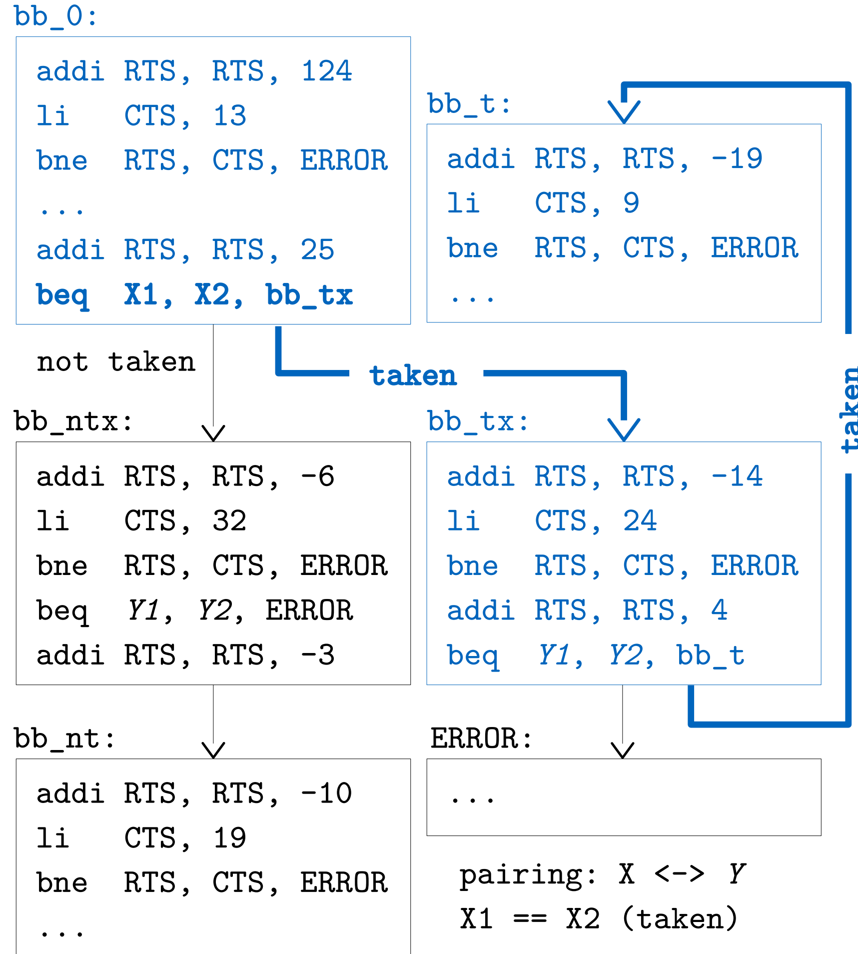

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```
bb_0:
addi  RTS, RTS, 124
li    CTS, 13
bne   RTS, CTS, ERROR
...
addi  RTS, RTS, 25
beq   X1, X2, bb_tx   (struck out)
```

not taken / taken

```
bb_t:
addi  RTS, RTS, -19
li    CTS, 9
bne   RTS, CTS, ERROR
...
```

```
bb_ntx:
addi  RTS, RTS, -6
li    CTS, 32
bne   RTS, CTS, ERROR
beq   Y1, Y2, ERROR
addi  RTS, RTS, -3
```

```
bb_tx:
addi  RTS, RTS, -14
li    CTS, 24
bne   RTS, CTS, ERROR
addi  RTS, RTS, 4
beq   Y1, Y2, bb_t
```

taken

```
bb_nt:
addi  RTS, RTS, -10
li    CTS, 19
bne   RTS, CTS, ERROR
...
```

```
ERROR:
...
```

```
pairing: X <-> Y
X1 == X2 (taken)
```

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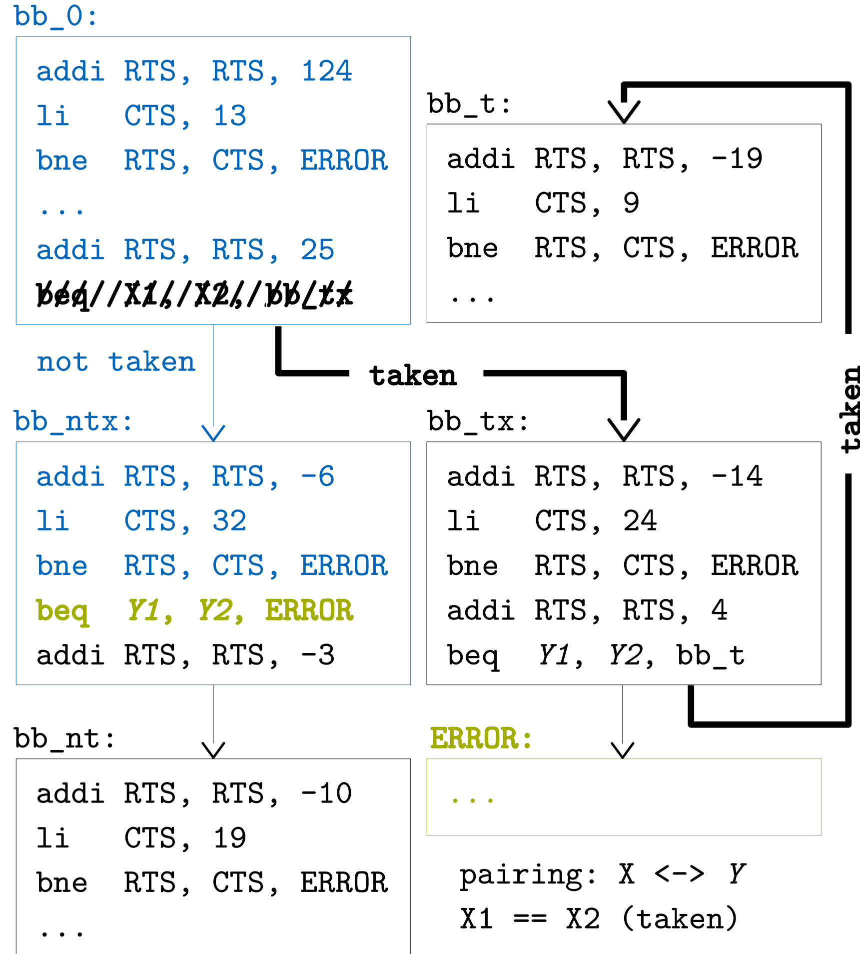

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  - DMR detect

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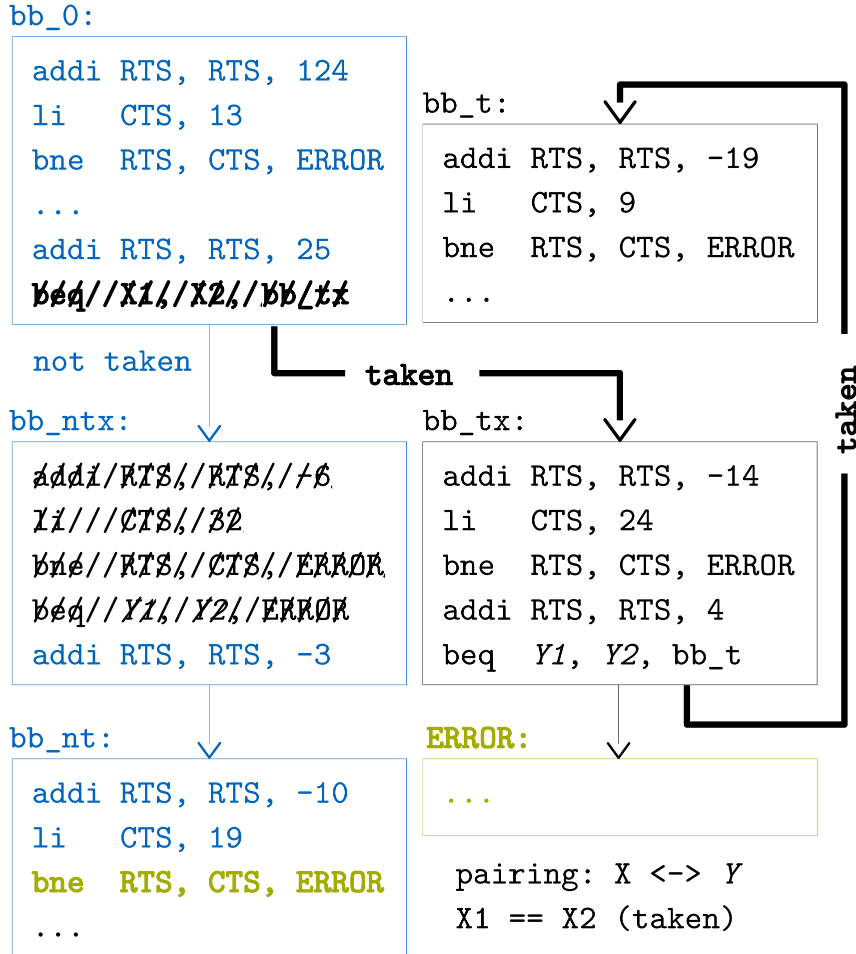

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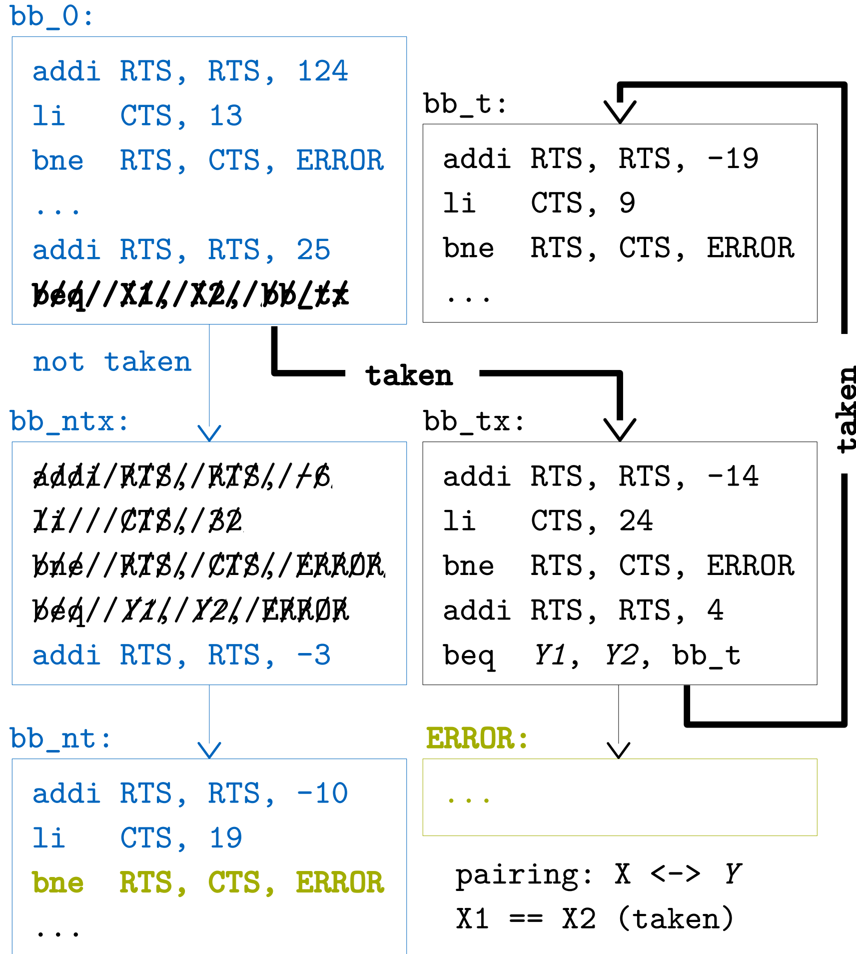

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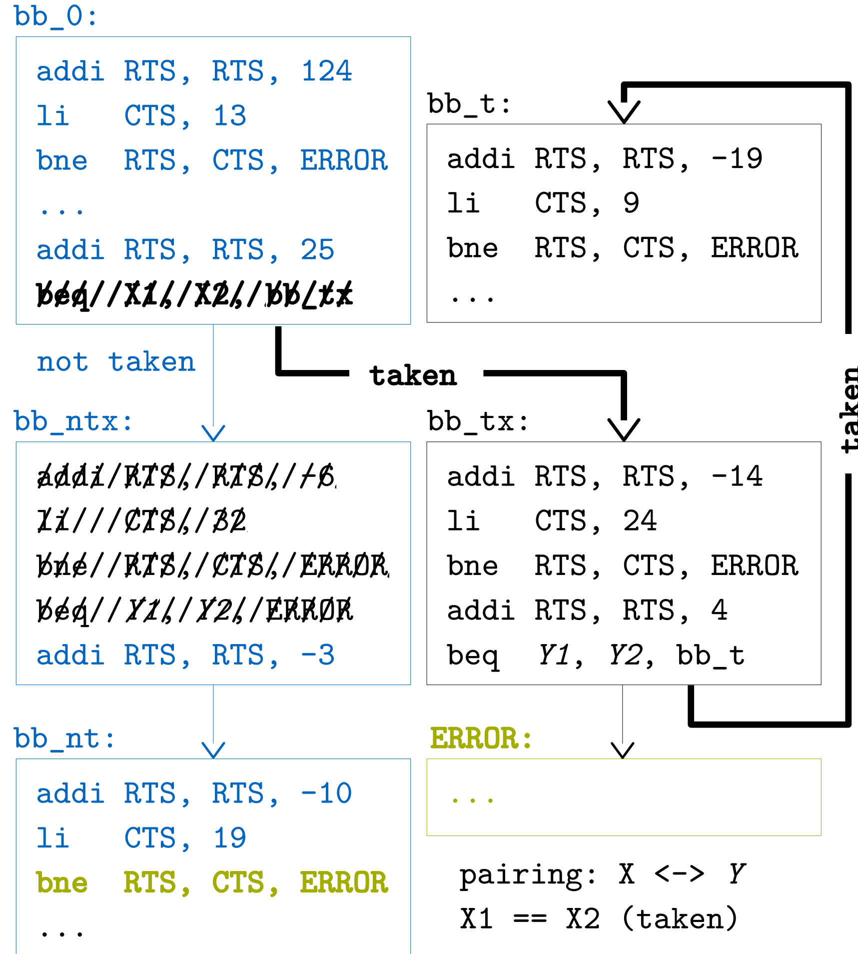

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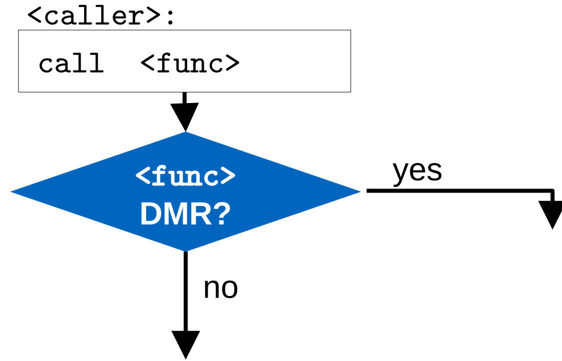
DMR↔RSM Symbiosis:

- DMR dataflow integrity
- RSM control flow integrity

Selective Hardening



- For all function calls during transformation

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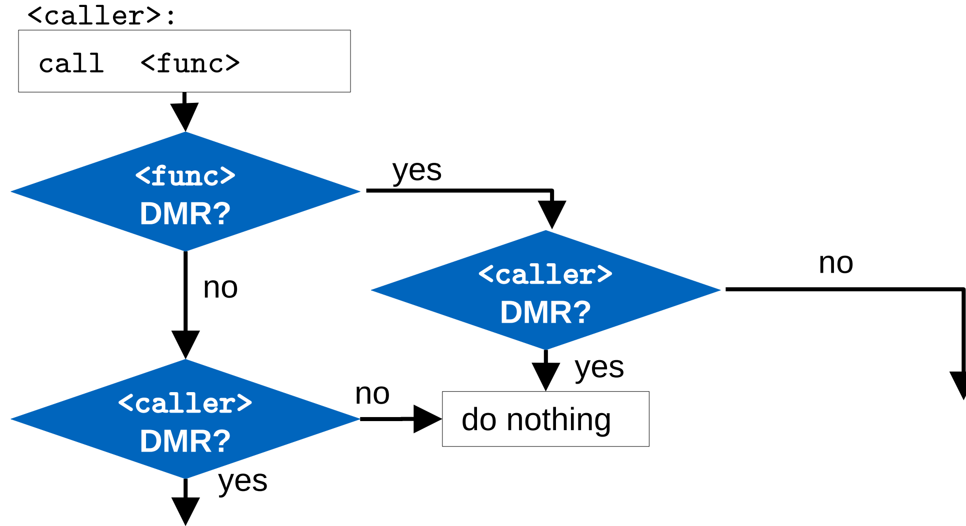

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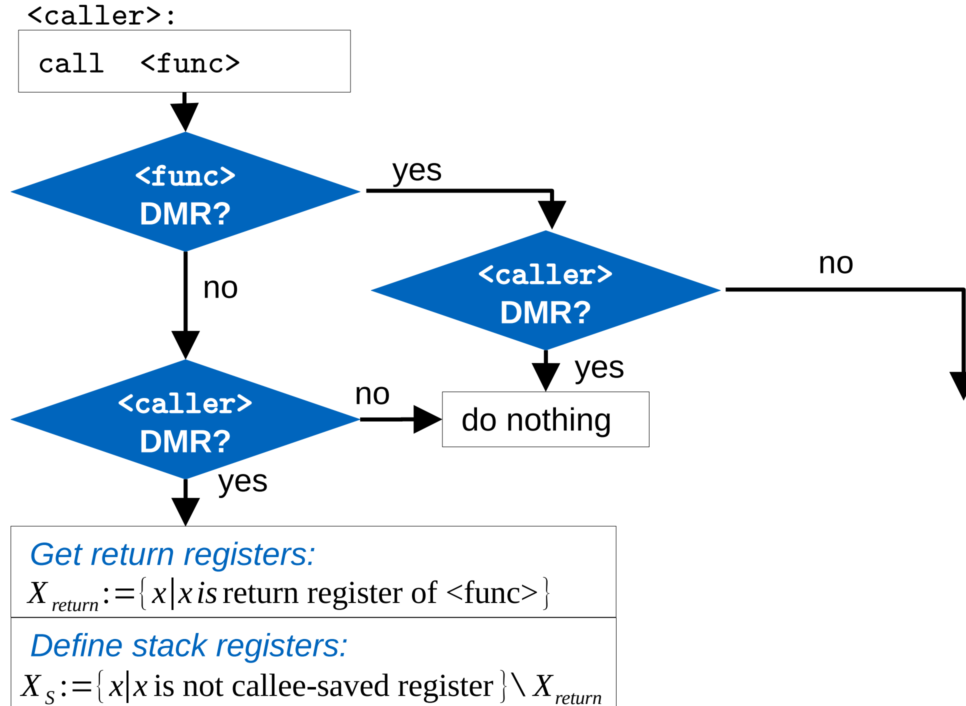

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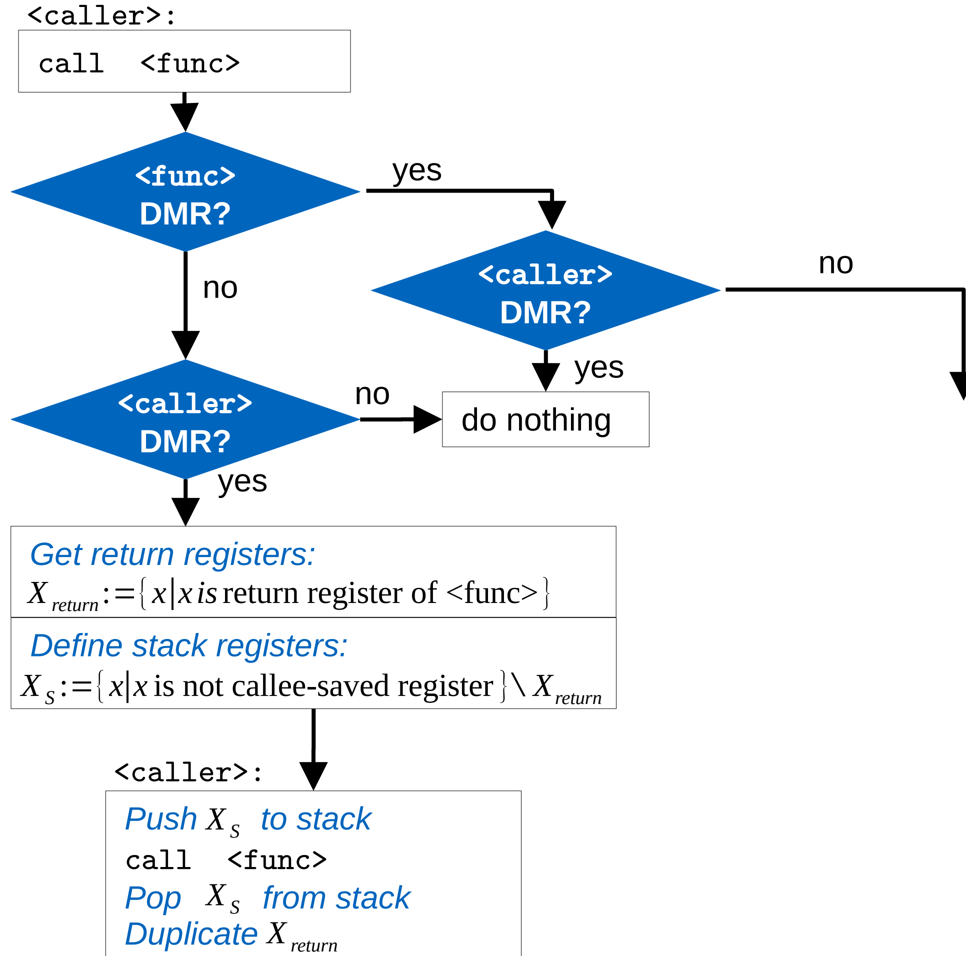

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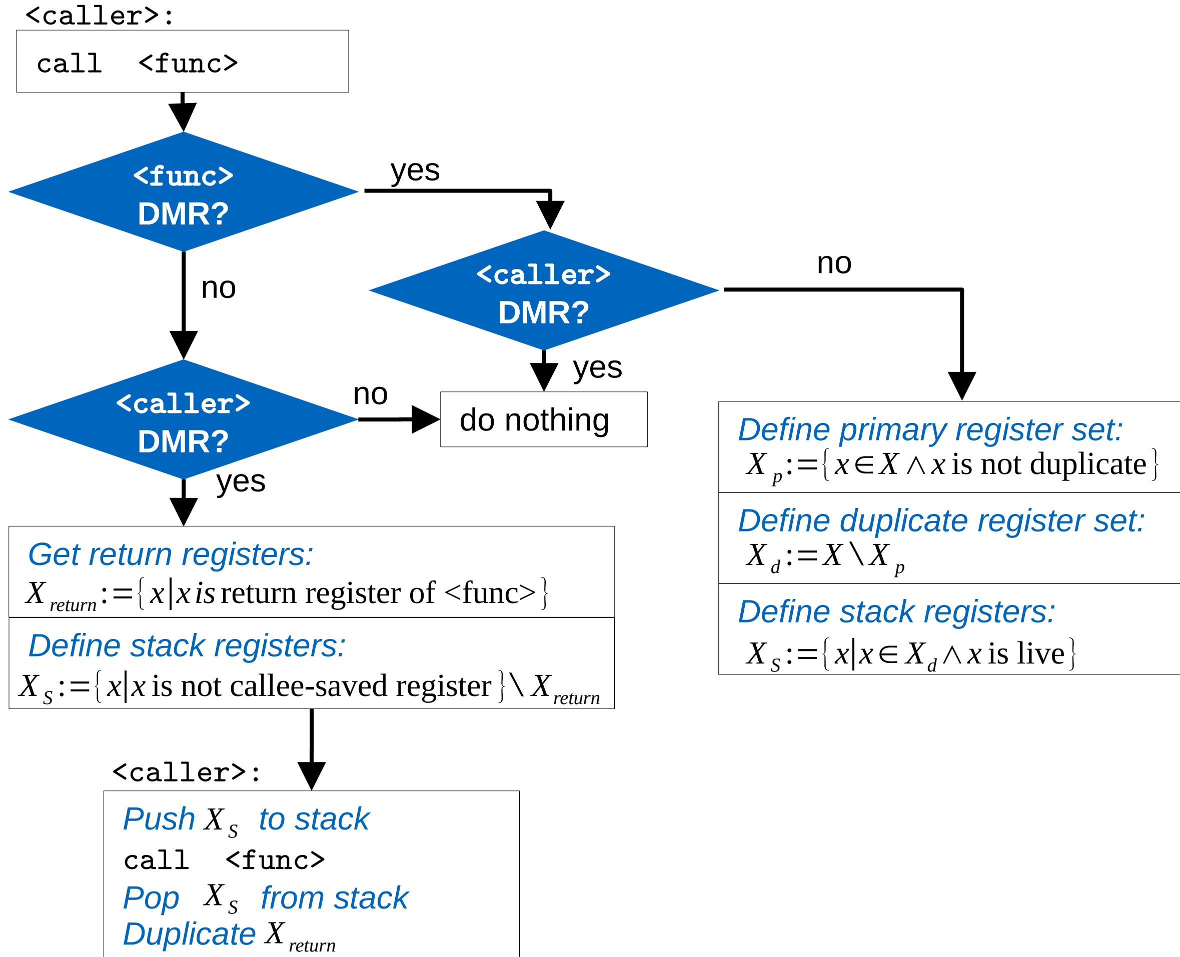

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- **non-DMR**→DMR prepare duplicates and asserts balance after return

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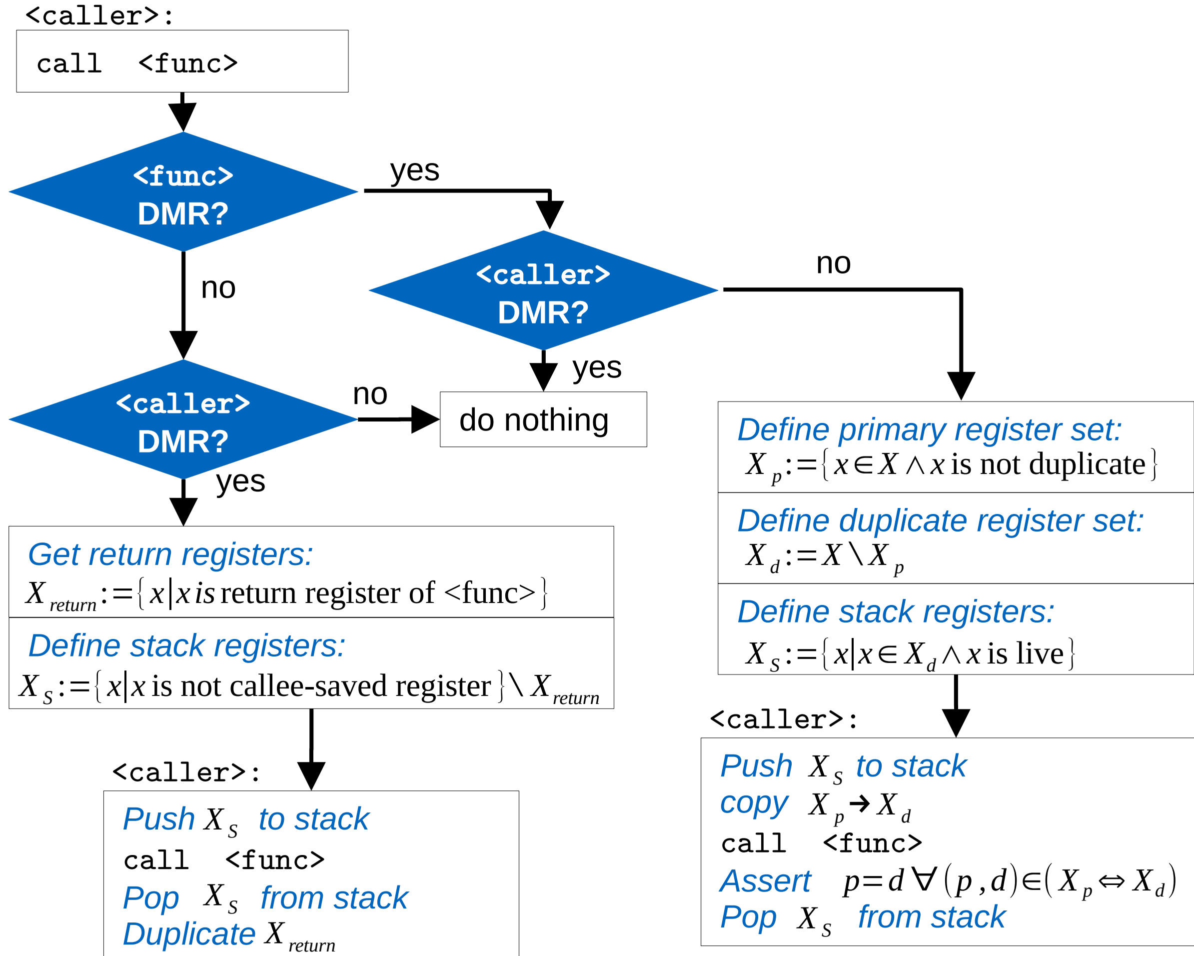

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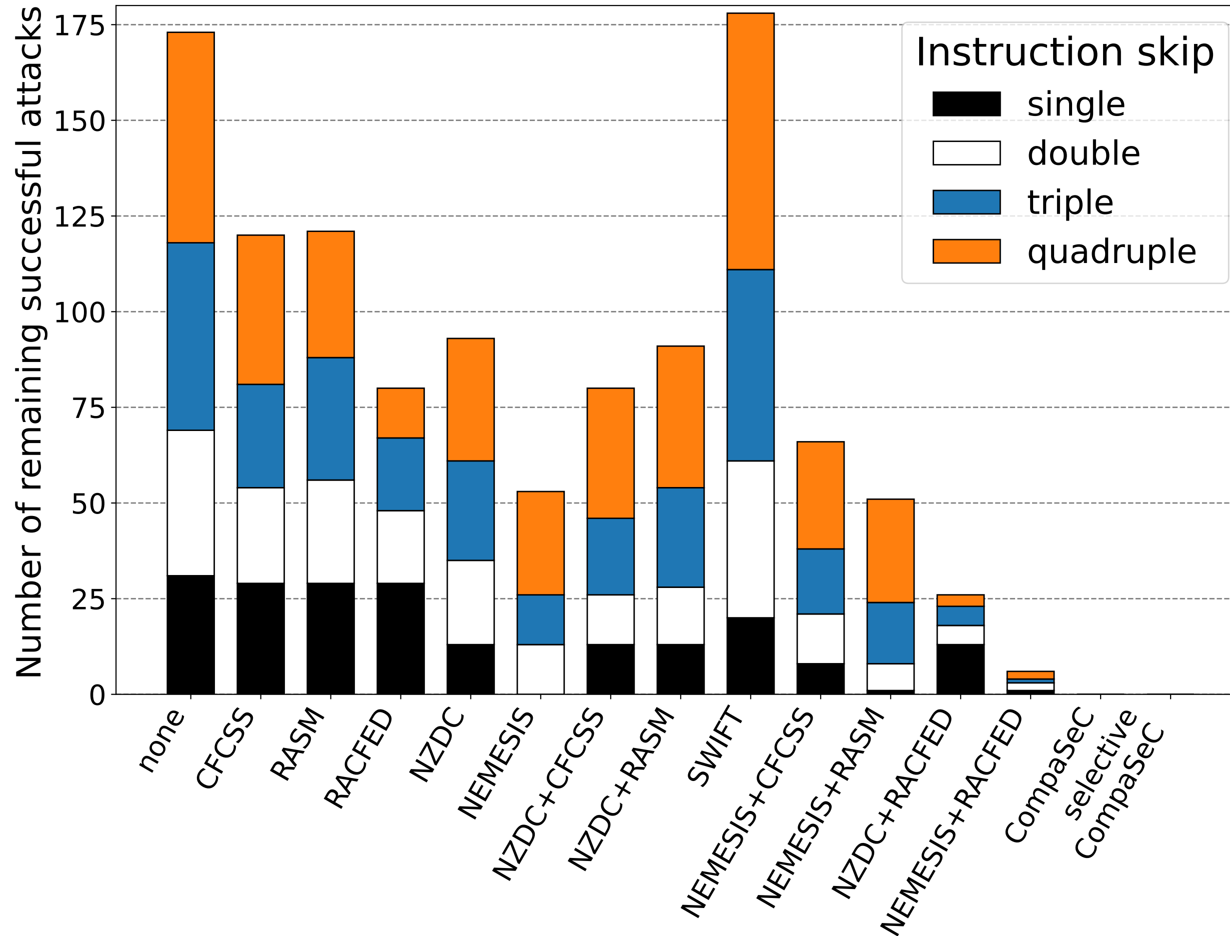
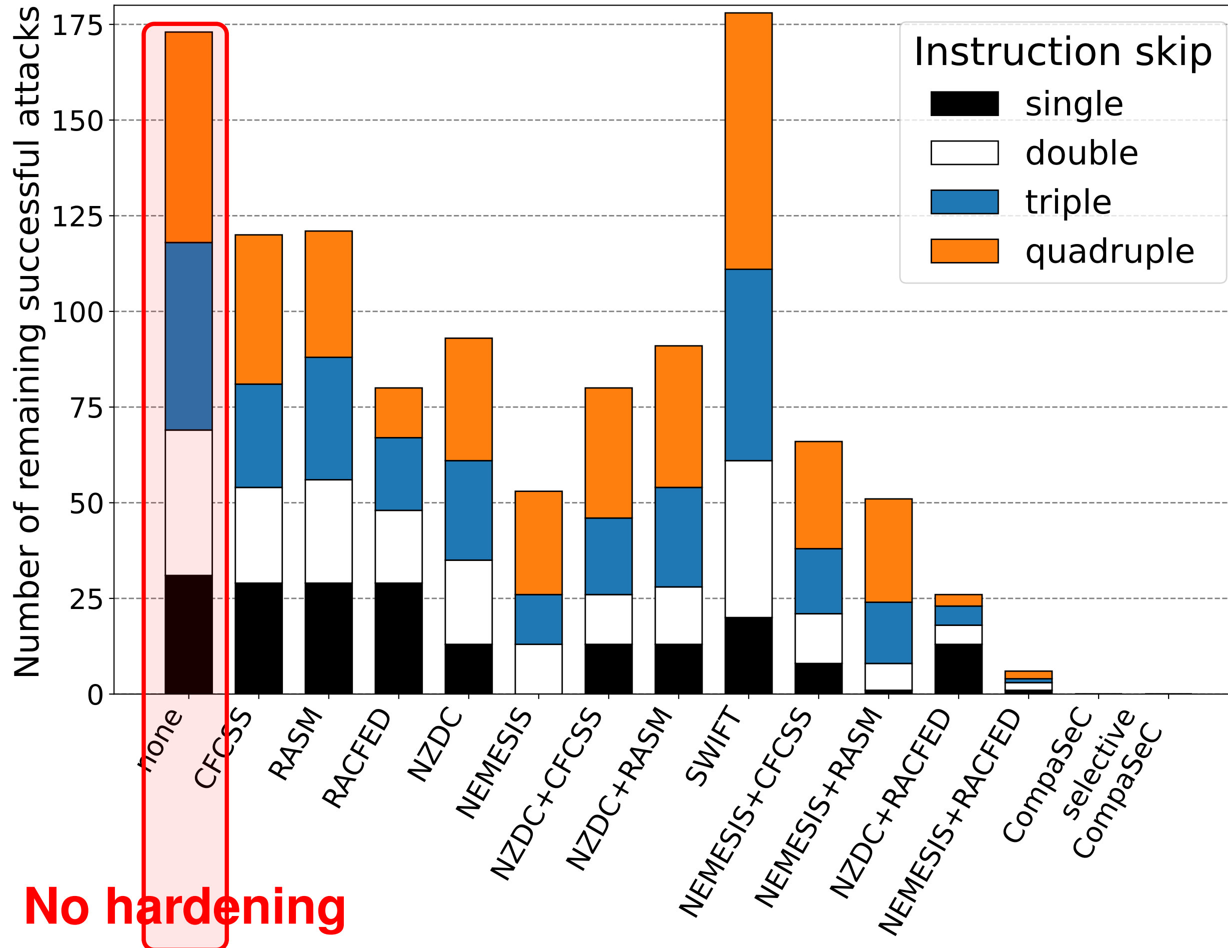
2. Simulate and Categorize

DMR	RSM	Fault Candidates [10^3]	Successful Faults	Detection Rate [%]
none		91	173	-
CompaSeC		685	0	85.9

Efficacy: Remaining Successful Fault Attacks



Efficacy: Remaining Successful Fault Attacks



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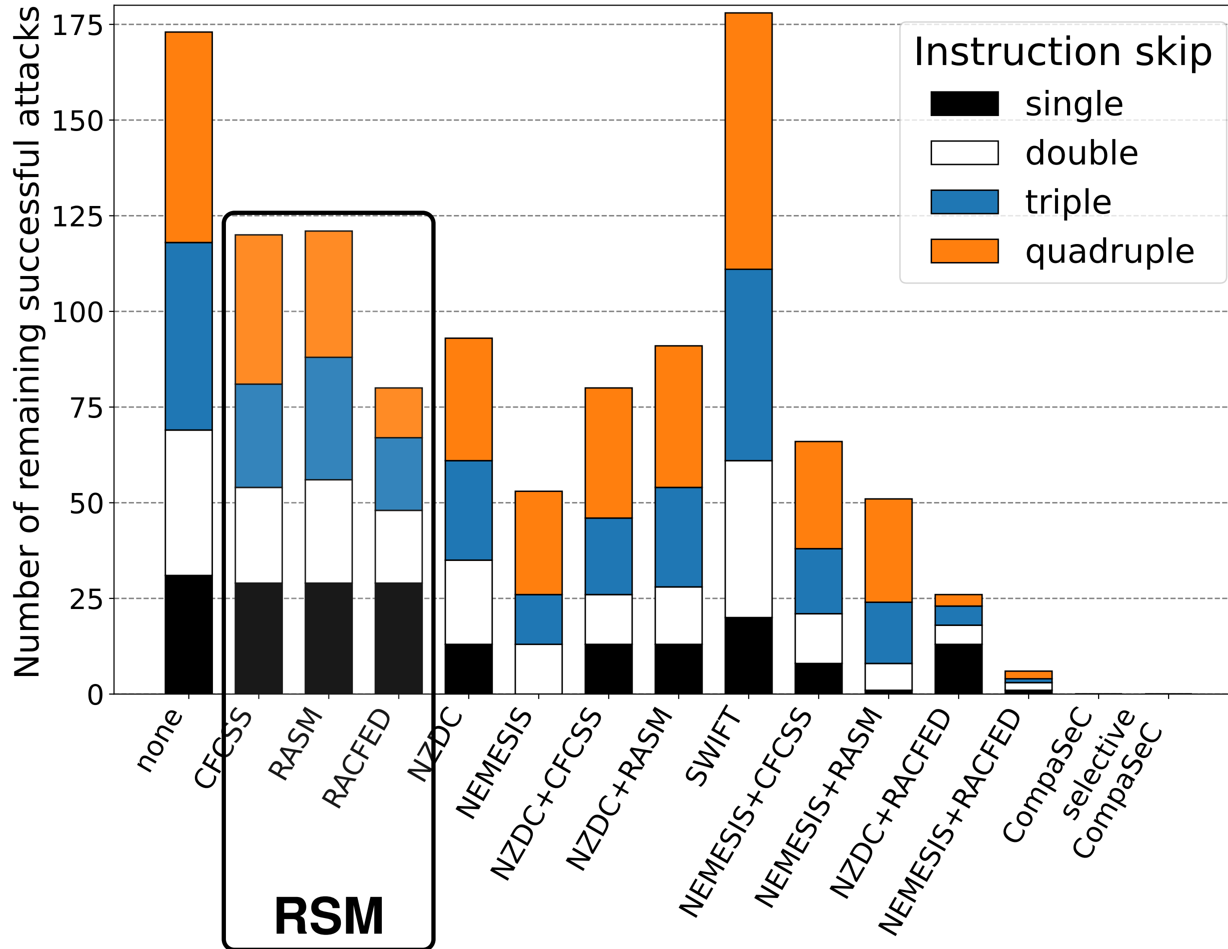

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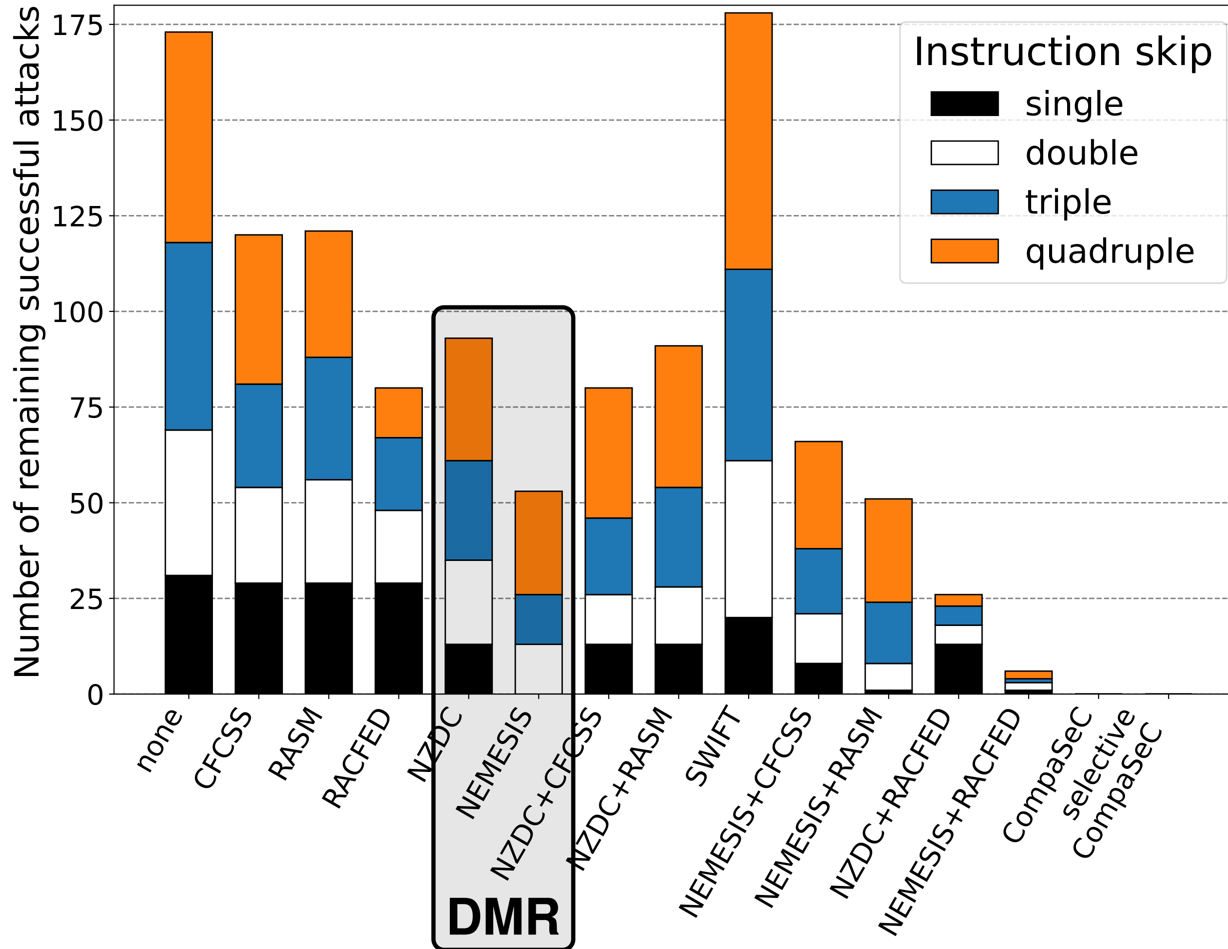

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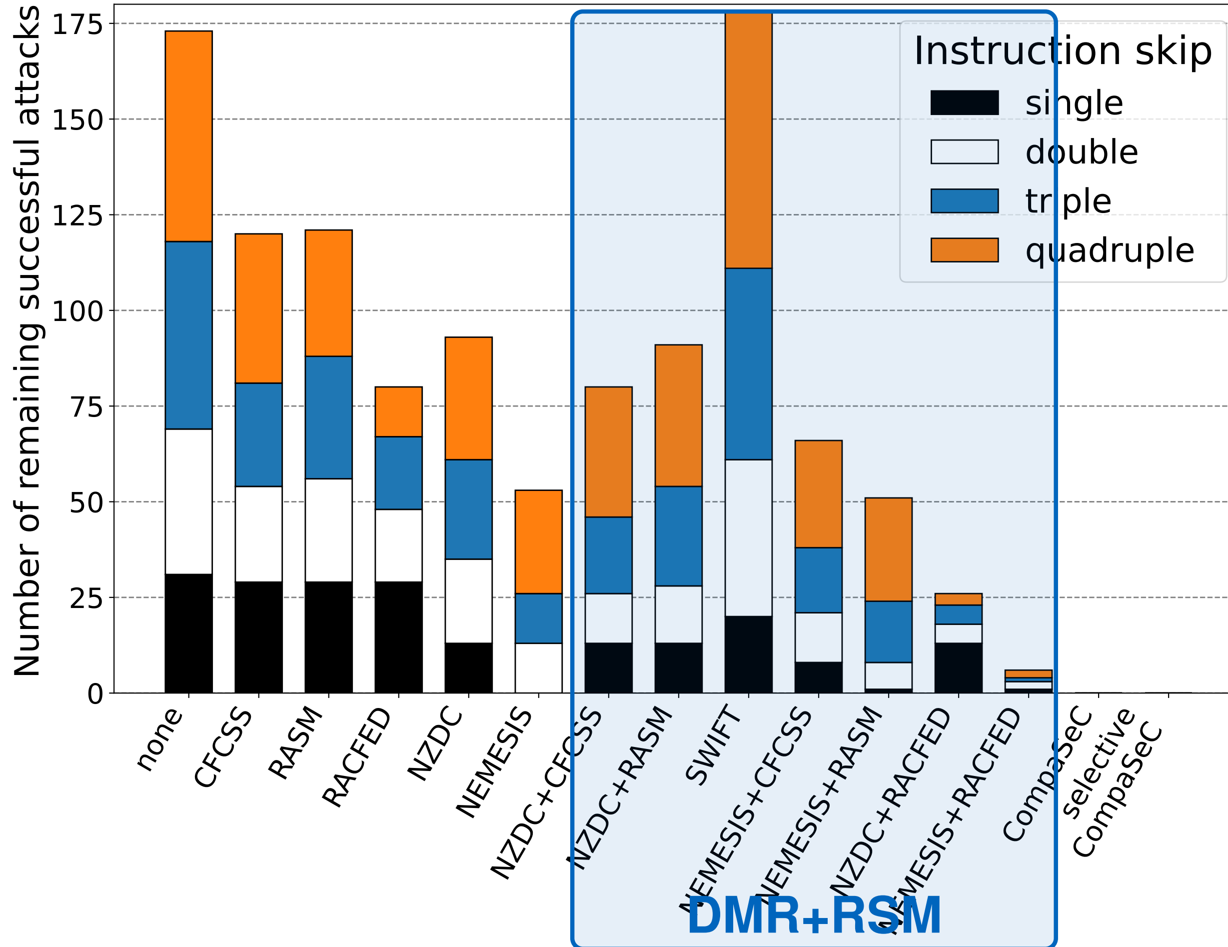

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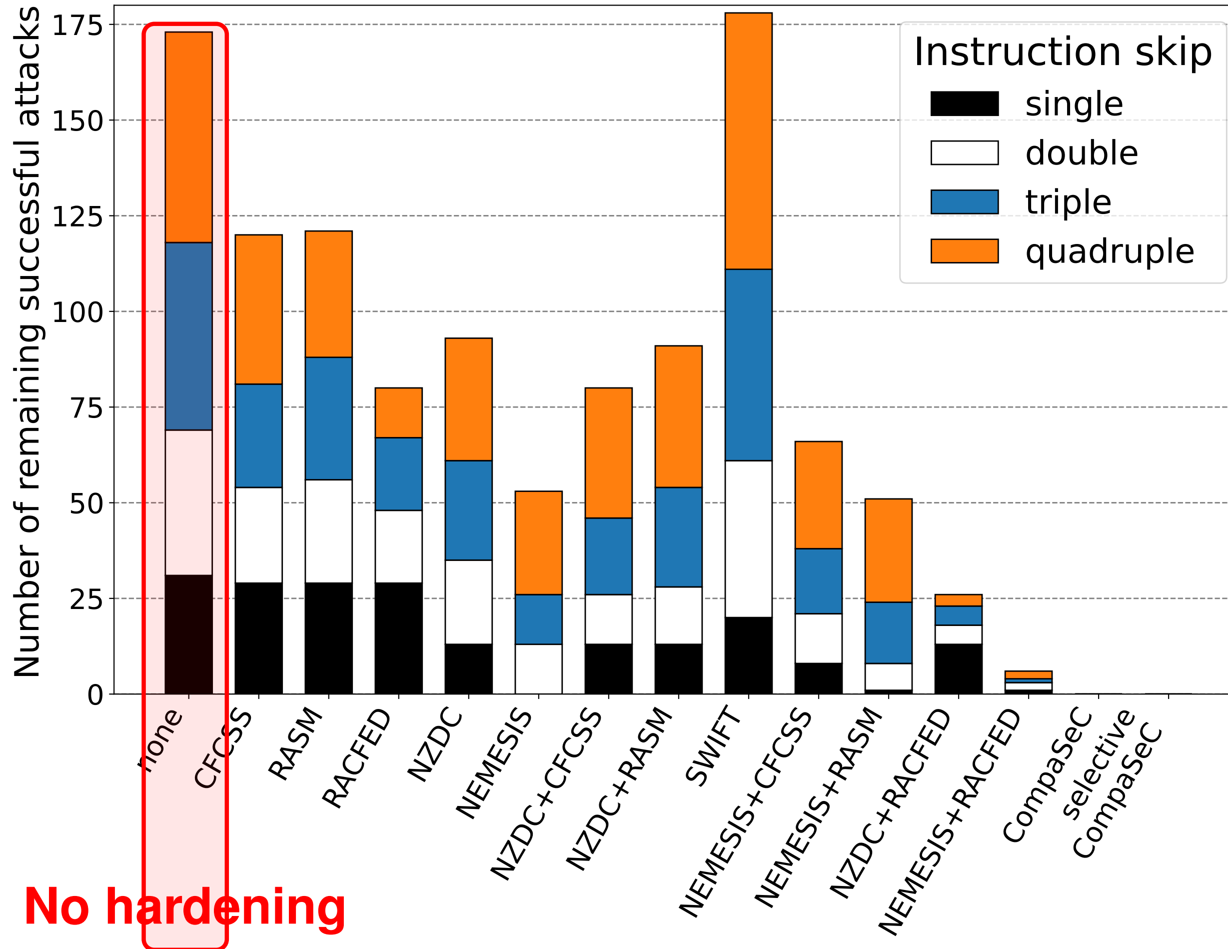

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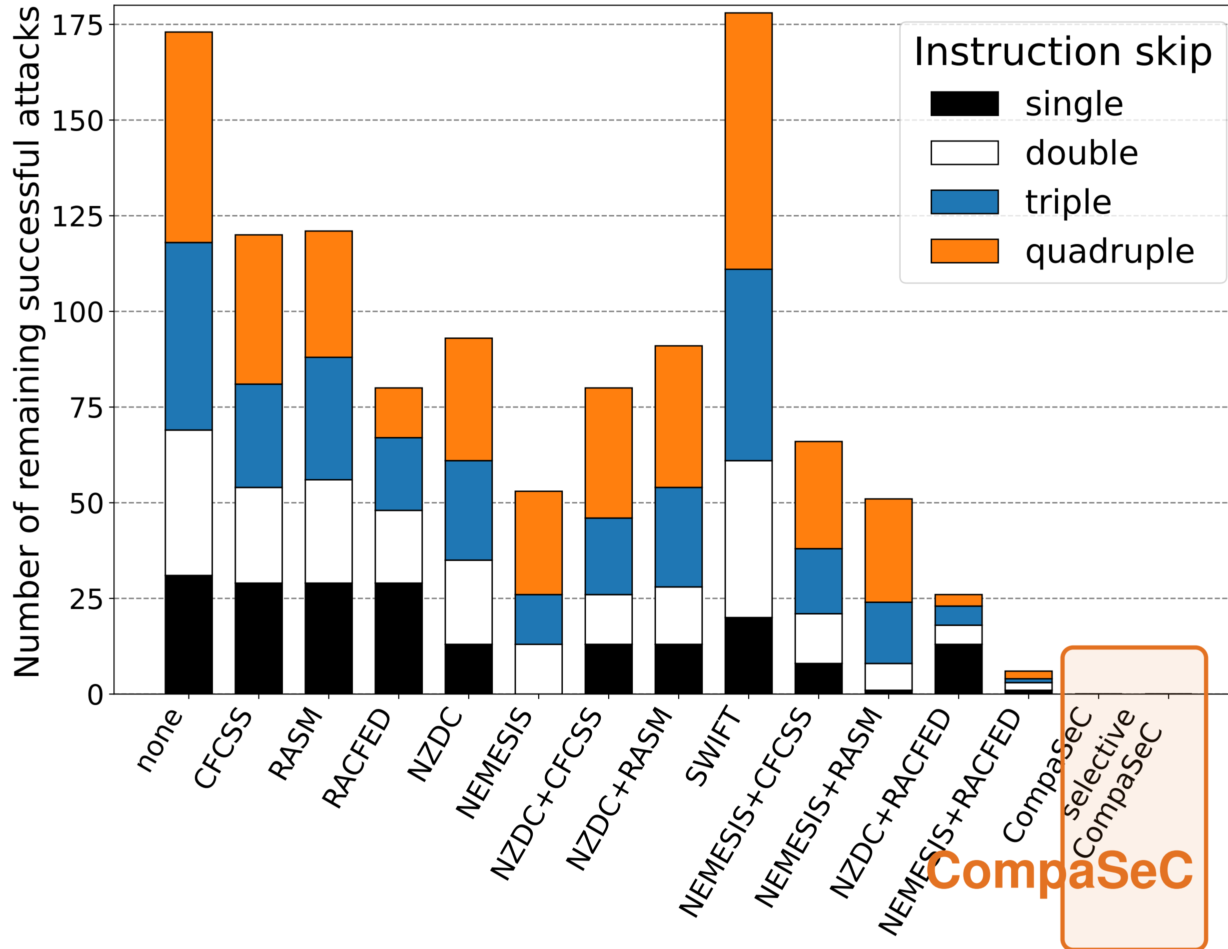
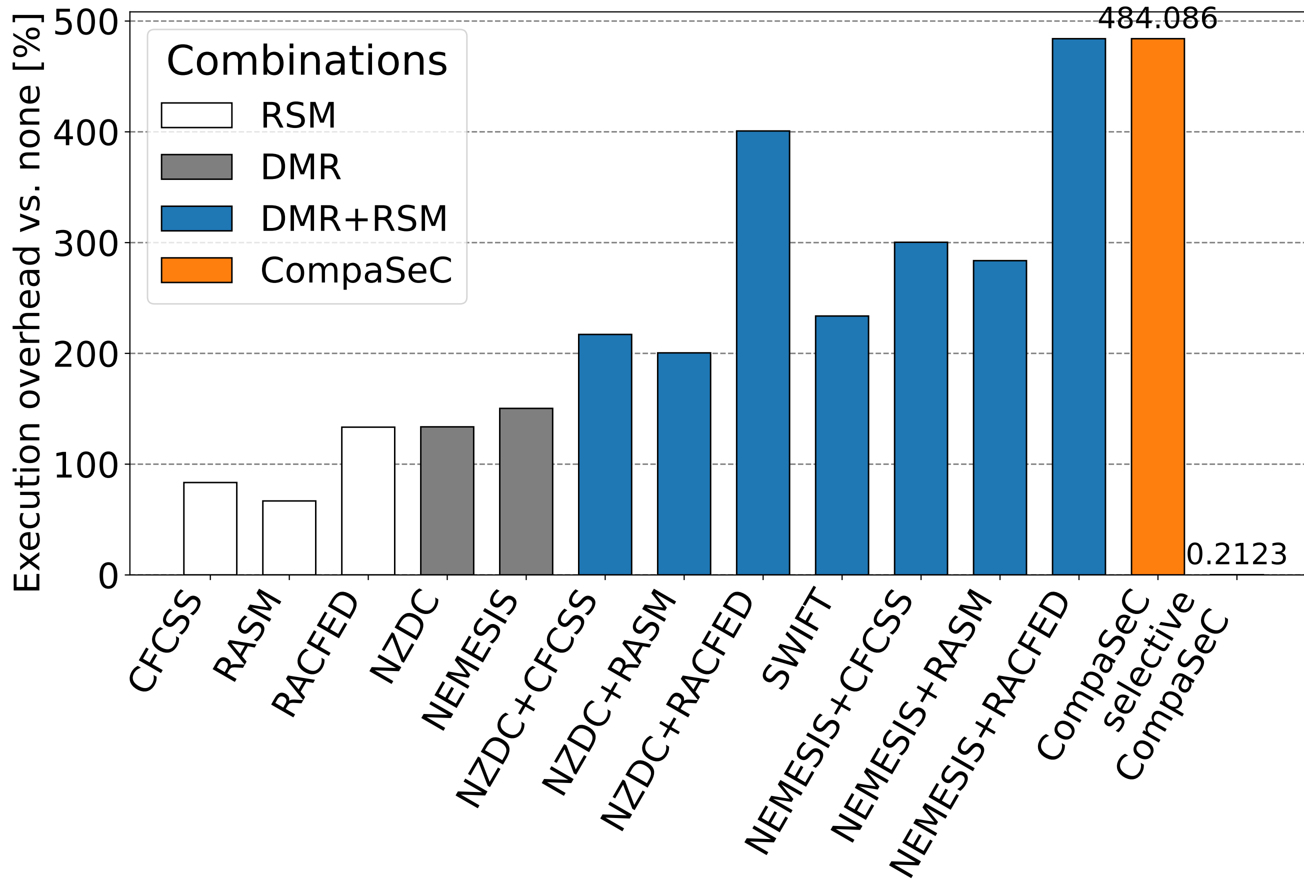


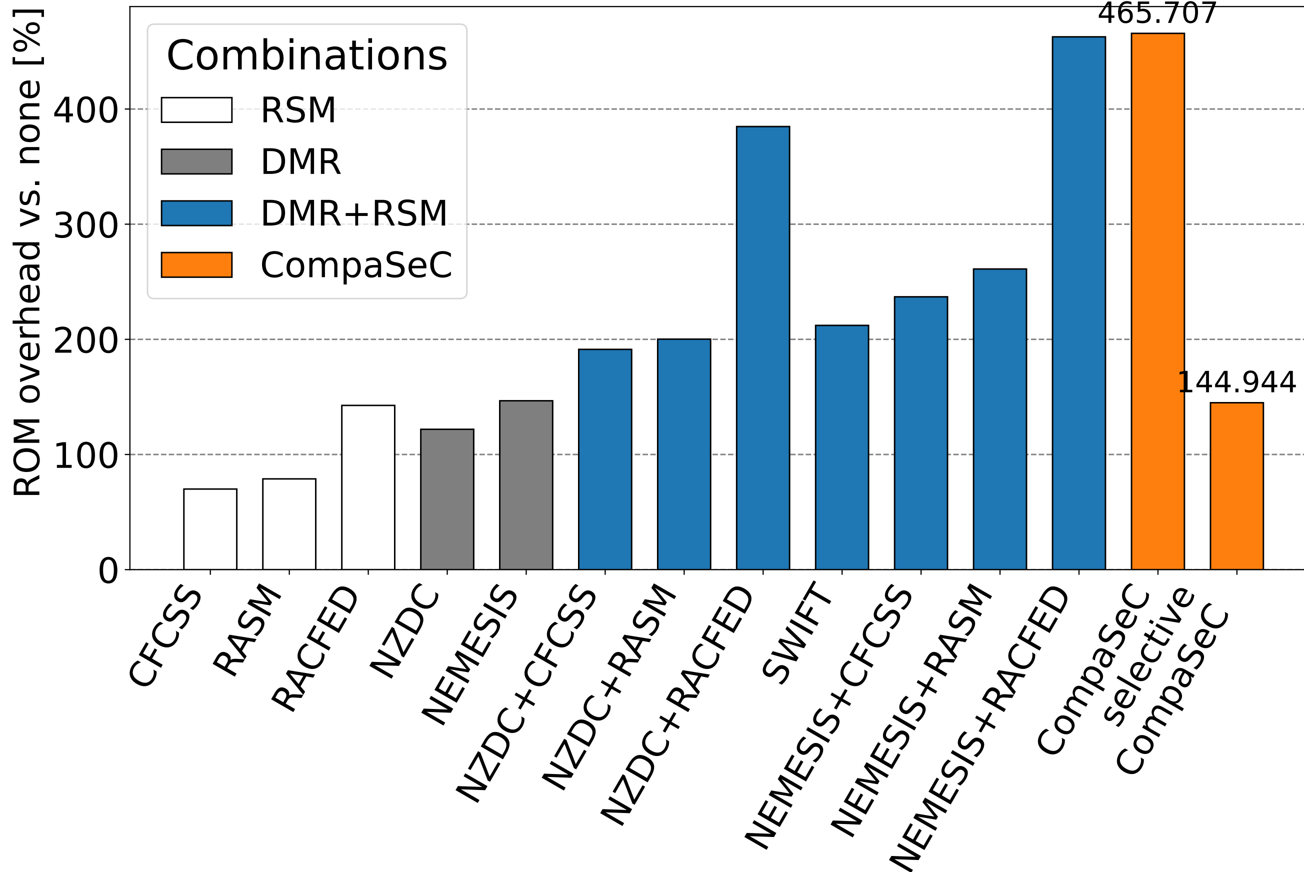
Performance: Execution Overhead

Metric: Number of executed instructions



Performance: ROM Size Overhead

Metric: ROM footprint for Secure Boot



Outline

1. Motivation

2. Compiler-assisted Countermeasures Against Instruction Skip Fault Attacks

3. Evaluation and Performance Results

4. Conclusion

Summary

Summary

- Security-aware compiler-assisted countermeasure
  - strong vs. single skip
  - weak vs. multi skip

  - weak vs. single skip
  - strong vs. multi skip

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  Dual Module Redundancy (DMR):
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  Runtime Signature Monitoring (RSM):
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- Combining DMR and RSM:
  - *"Symbiotic Interplay"* at large overhead and high protection

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- Verification against known Fault Model allows:
  - Identifying vulnerable code sections
  - Selective Hardening: small overhead and high protection

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Open Source:

github.com/tum-ei-eda/compas-ft-riscv

Compas [10]/CompaSeC [11] LLVM-based Compiler

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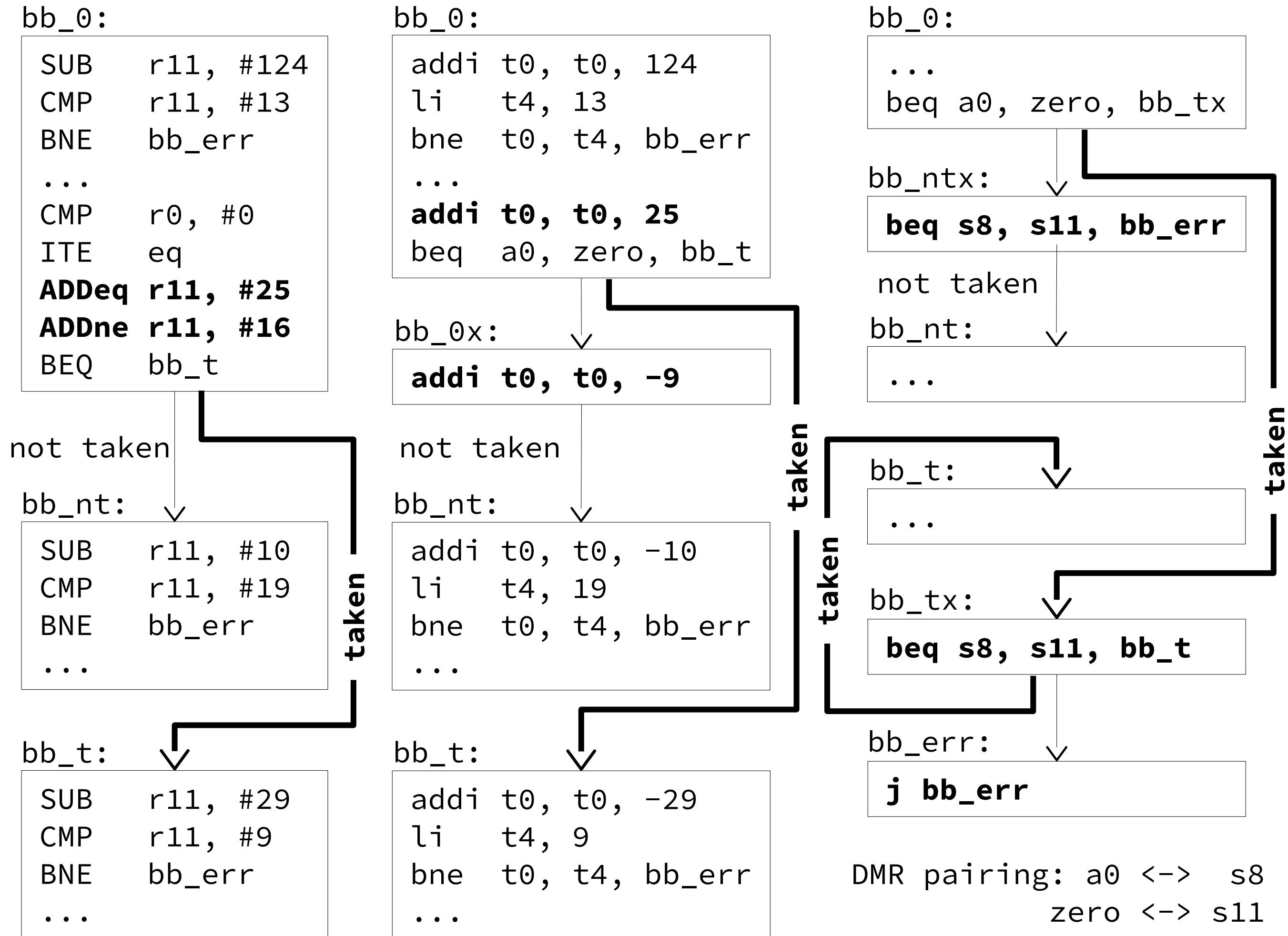
Speaker

Johannes Geier received the B.Eng. (2018) in Electrical Engineering from OTH Regensburg and M.Sc. (2020) in Electrical Engineering from Technical University of Munich (TUM), Germany. Currently, he is a doctoral candidate at the Chair of Electronic Design Automation at TUM.
His research interests include virtual prototypes, fault injection simulations, and instruction set architectures.

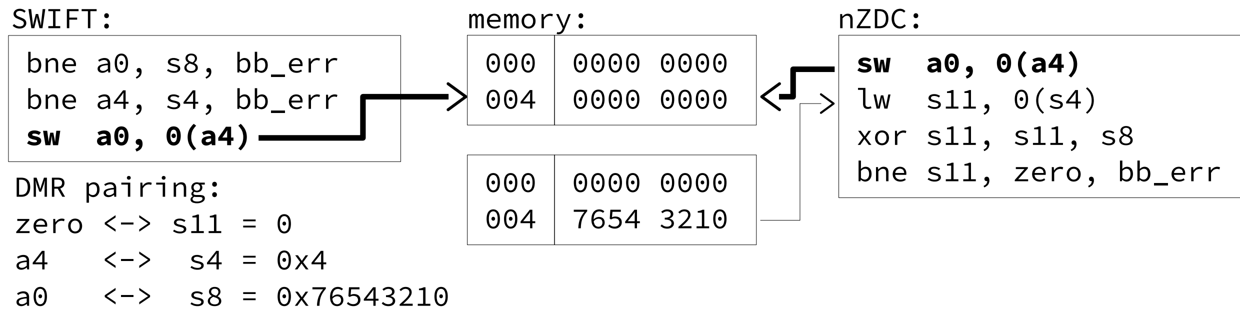
Backup - Predicated Problem



Backup - CompaSeC Combination Details

DMR

- *nZDC+NEMESIS* [2, 3] duplication, memory store-load-back loop, and balance check schedule
- *SWIFT* [4] **volatile** memory store protection
- Duplicated branches as basic block entities



RSM

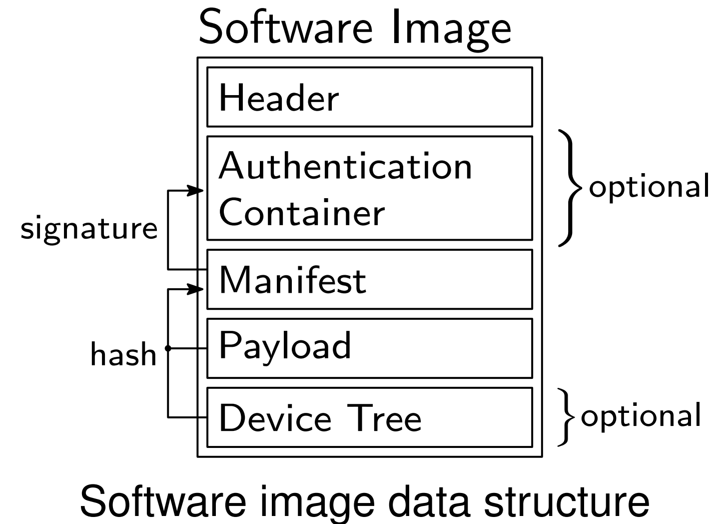
- *RACFED* [7] instruction level additive signature, basic block level checks. Adapted algorithm for minimal basic blocks size
- Pass includes DMR code

Backup - Scenario: Bypass Secure Boot

Goal: Boot a malicious Software Image, that has ...

- "No signature"
  - No authentication container is included
  - Verification of SW image is not possible
  - Not accepted by Secure Boot

- "Incorrect signature"
  - Authentication container is included
  - Signing key is not trusted
  - Not accepted by Secure Boot



Software image data structure

→ Secure Boot binary hardened with combinations of DMR and RSM techniques

Backup - Efficacy Details

DMR	RSM	Fault Candidates [10^3]	Successful Faults	Detection Rate [%]
none		91	173	-
-	cfcss	202	120	43.2
-	rasm	205	121	52.8
-	racfed	250	80	68.1
nzdc	-	268	93	37.6
nemesis	-	282	53	43.9
nzdc	cfcss	374	80	48.0
nzdc	rasm	376	91	53.1
nzdc	racfed	608	26	85.2
nemesis	cfcss	391	66	52.2
nemesis	rasm	421	51	60.9
nemesis	racfed	673	6	85.8
swift		369	178	48.3
CompaSeC		685	0	85.9
select CompaSeC		142	0	32.5

Backup - Statistic Evaluation

Safety vs. Security

Safety:

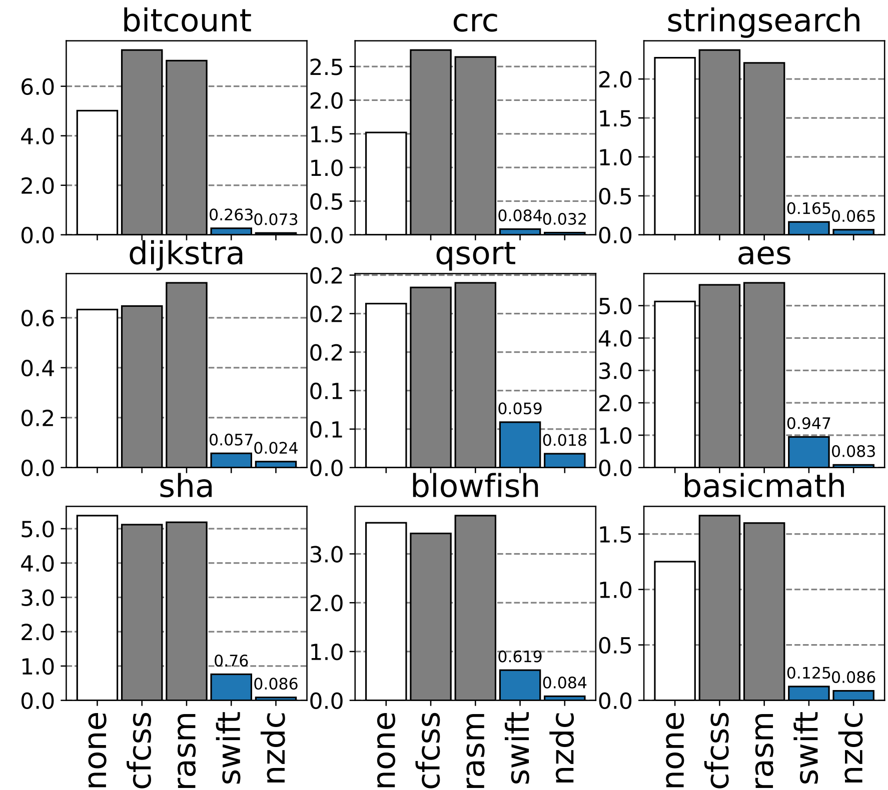
- Fault Tolerance
- Fault Model: **Random**
- Example: Cosmic rays

→ Stochastic Evaluation

Security:

- Fault Detection
- Fault Model: **Targeted**
- Example: Differential Fault Analysis

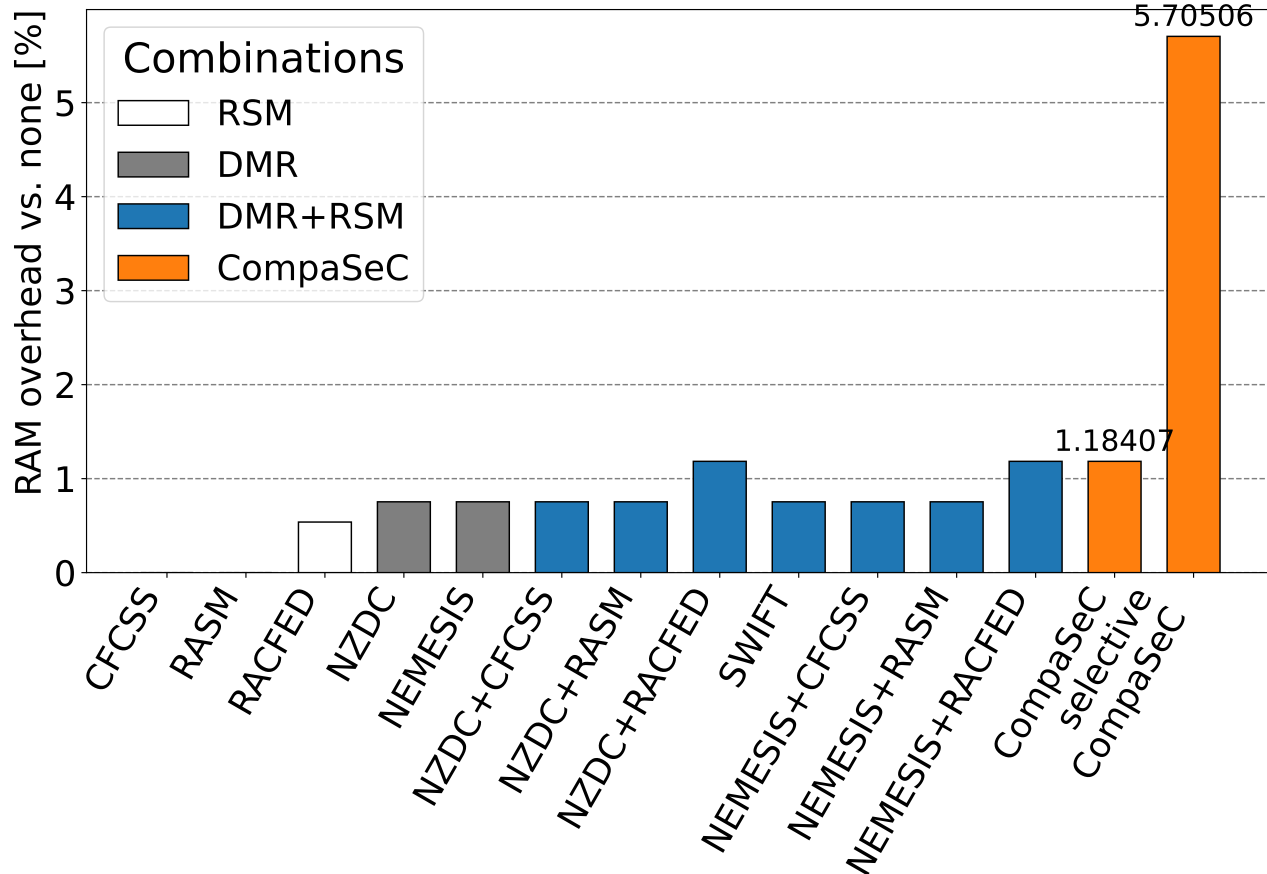
→ Verification



Silent Data Corruption Rates in MiBench programs [10]

Backup - Performance: RAM Size Overhead

Metric: RAM footprint for Secure Boot



Backup - Performance: Memory Traffic Overhead

Metric: Number of RAM memory transactions