Data-Driven Approaches for Process Simulation and Optical Proximity Correction

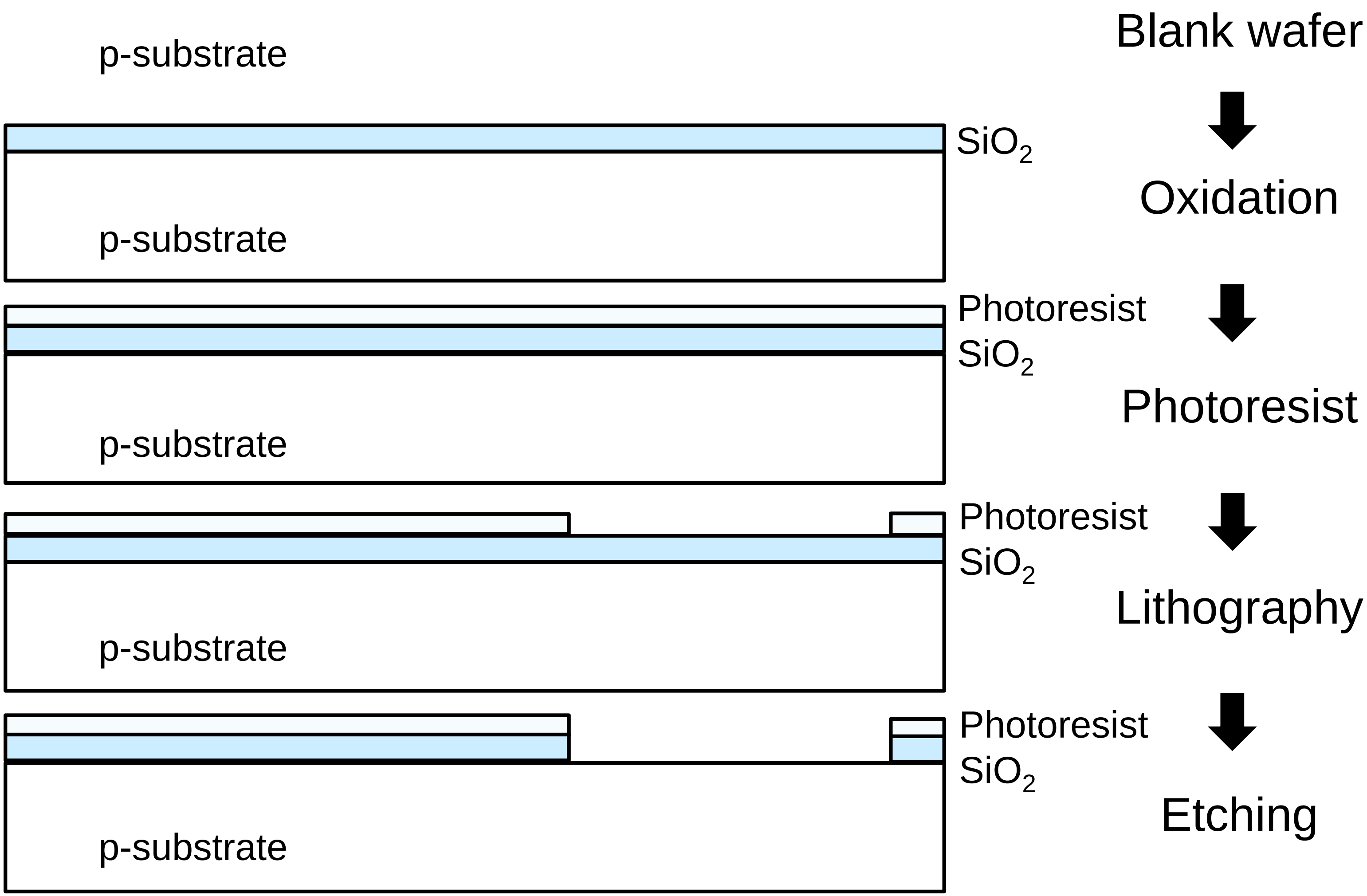
Hao-Chiang Shao[1], Chia-Wen Lin[2], and Shao-Yun Fang[3]

[1] National Chung Hsing University (NCHU), Taichung, Taiwan
[2] National Tsing Hua University (NTHU), Hsinchu, Taiwan
[3] National Taiwan University of Science and Technology (NTUST), Taipei, Taiwan

THE EDA LAB
TAIWAN TECH

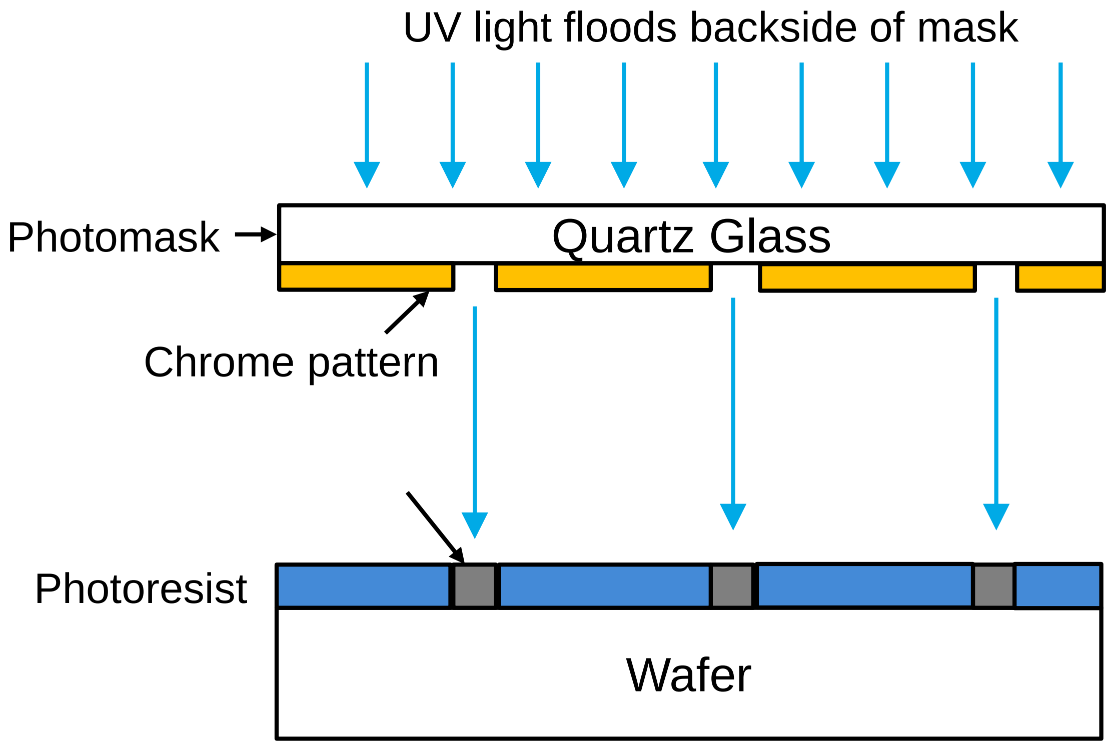
Introduction

IC Fabrication Process



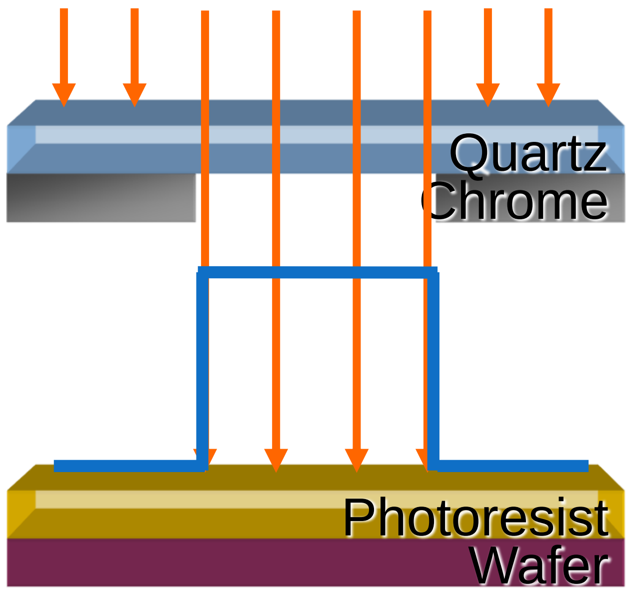
Photolithography

- **Use photomask and photoresist to define where some material will be present or absent**

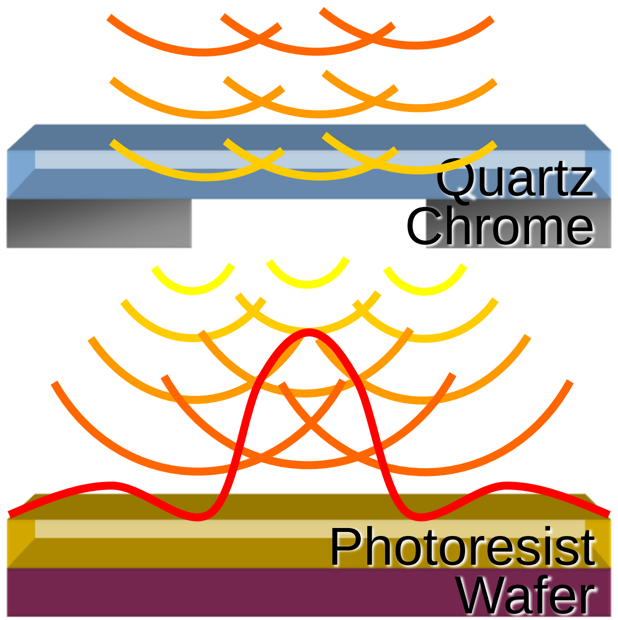


Optical Effect

- **Ideal lithography: light passes through features by a straight path**
- **Real lithography: light behaves like waves when feature size is close to wavelength**



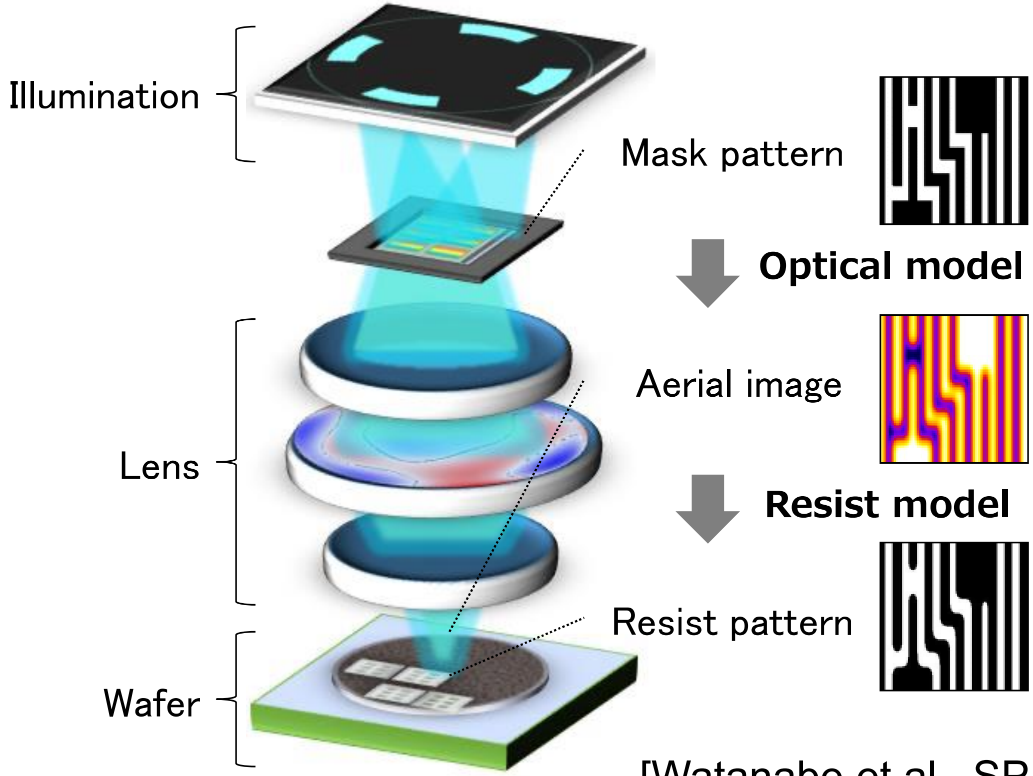
ideal lithography



real lithography

Lithography Simulation

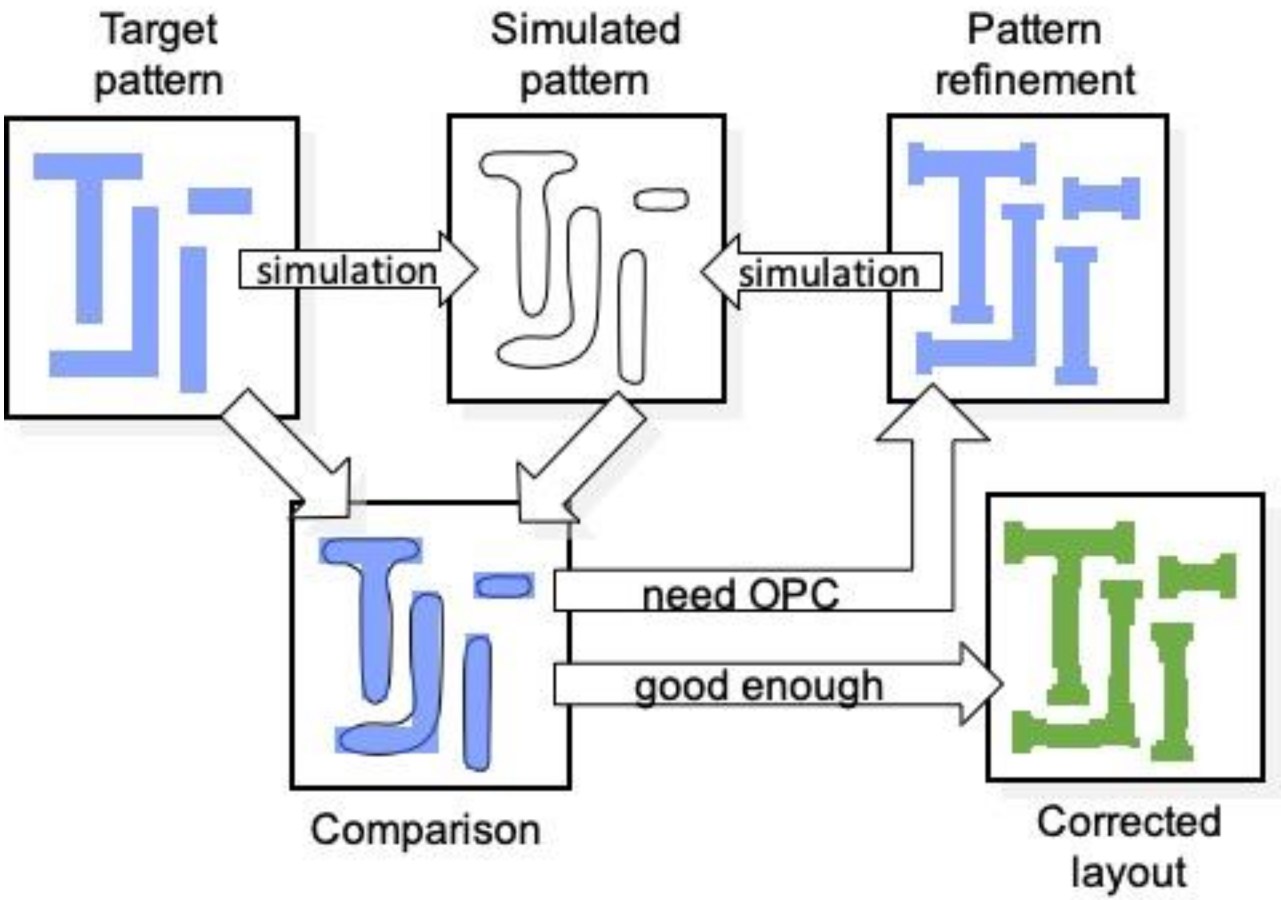
- **Lithography simulation generates simulated wafer patterns in the layout design stage**
  - Require high accuracy
  - Computationally expensive and time-consuming



[Watanabe et al., SPIE'17]

Optical Proximity Correction (OPC)

- One of the most effective and widely adopted RETs
- Model-based OPC is usually adopted and also time-consuming



Data-driven Approaches

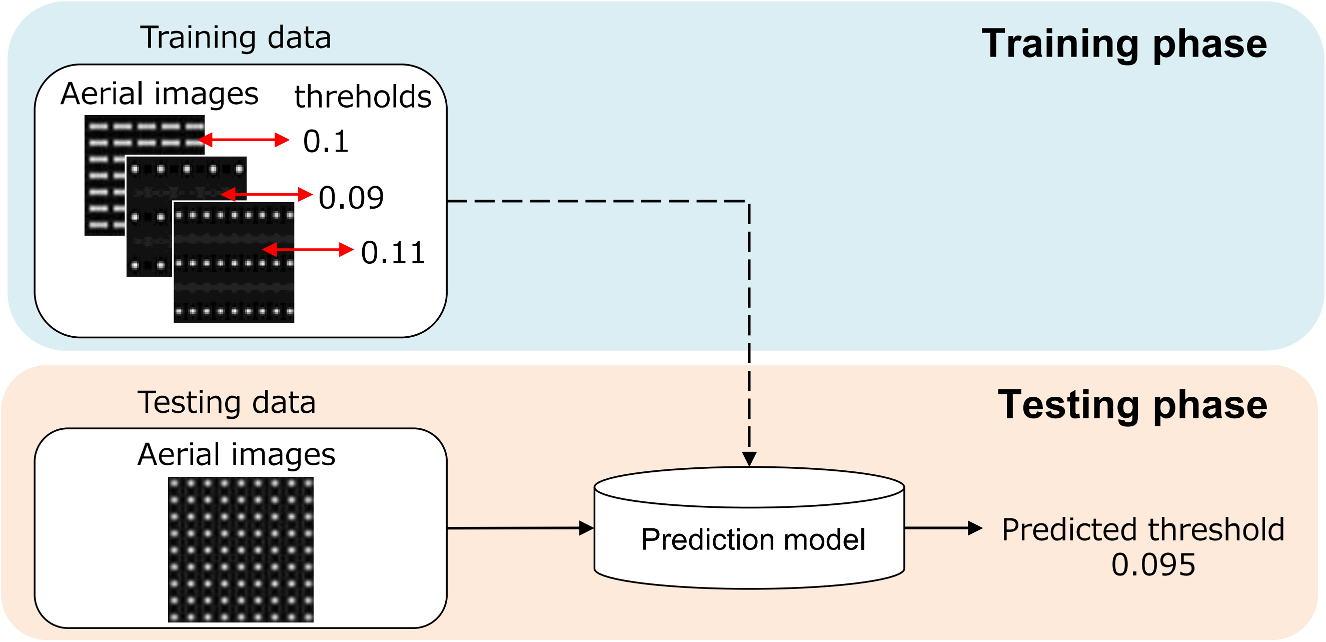
- **Machine learning-based approaches are recently popular**
  - Fast inference time (greatly speed up lithography simulation and OPC)
  - Could handle unseen patterns
  - Require huge data for model training

- **In this talk**
  - Data-driven approaches are reviewed
  - Critical challenges are highlighted
  - Primary technical contributions are summarized
  - Future research directions are suggested

Data-driven Approaches for Lithography Simulation

A Data-driven Resist Model

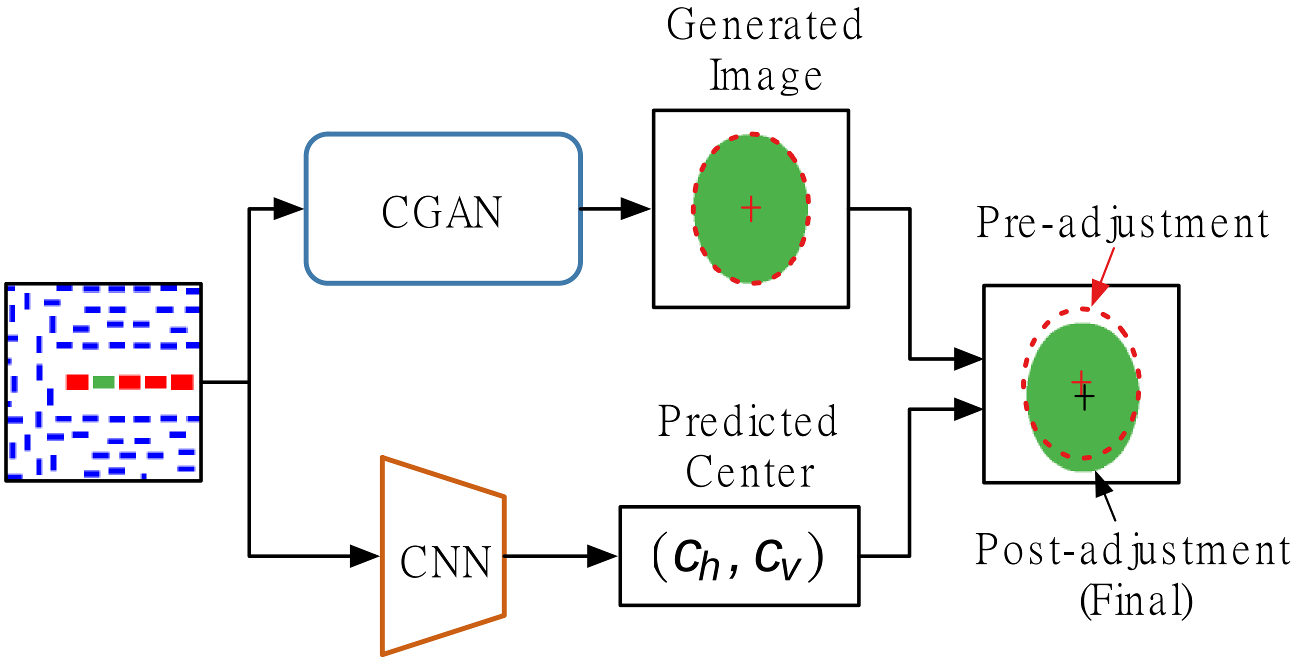
- **Watanabe et al., "Accurate lithography simulation model based on convolutional neural networks," SPIE'17**
  - Convolutional neural network (CNN)-based
  - Automatically extracting features from an aerial image
  - Outperform constant/variable threshold resist models



[Watanabe et al., SPIE'17]

An End-to-End Lithography Model

- **Ye et al., "LithoGAN: end-to-end lithography modeling with generative adversarial networks," DAC'19**
  - Conditional generative adversarial network (CGAN)-based
  - The CGAN generates the simulated image of the target hole
  - The CNN predicts the center coordinate of the hole

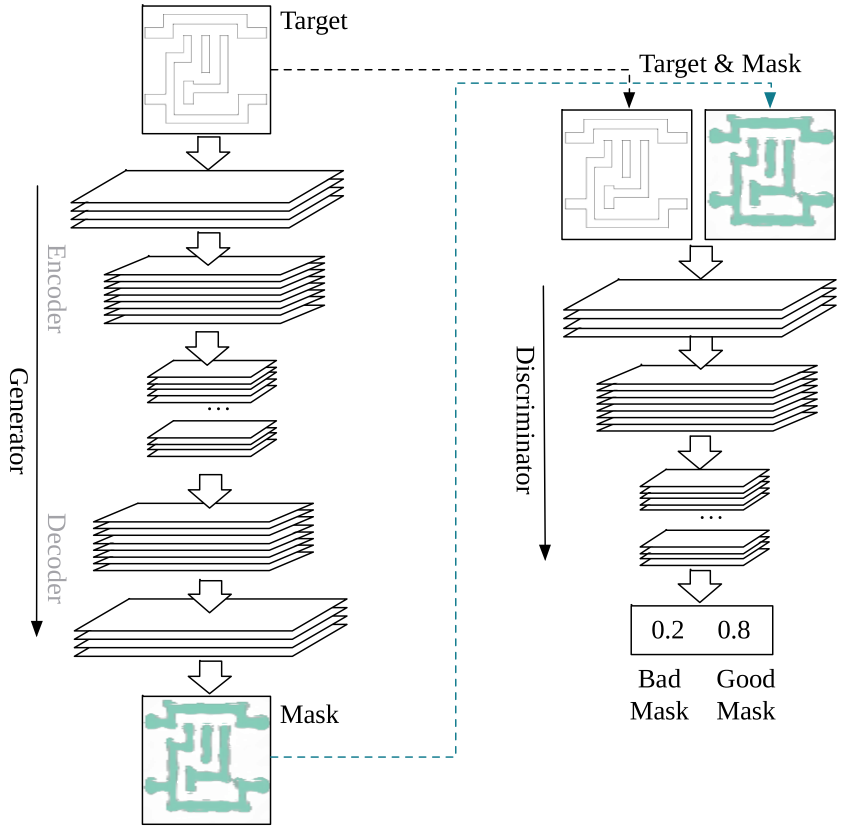


[Ye et al., DAC'19]

Data-driven Approaches for Mask Optimization

A CGAN-based OPC Model

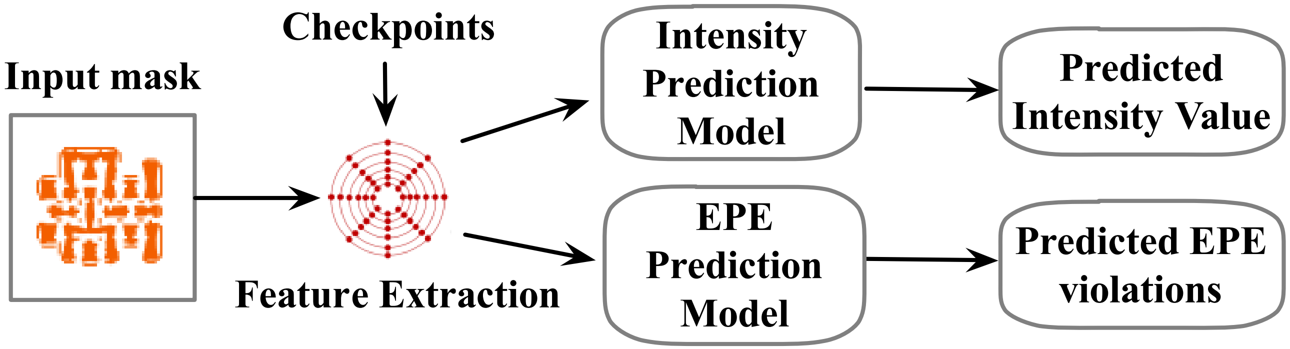
- **Yang et al., “GAN-OPC: Mask optimization with lithography-guided generative adversarial nets,” DAC’18**
  - GAN-based
  - The generator is composed of an auto-encoder
  - The discriminator determines whether the mask pattern is a reference pattern and corresponds to the target pattern



[Yang et al., DAC’18]

OPC Acceleration with ML Prediction

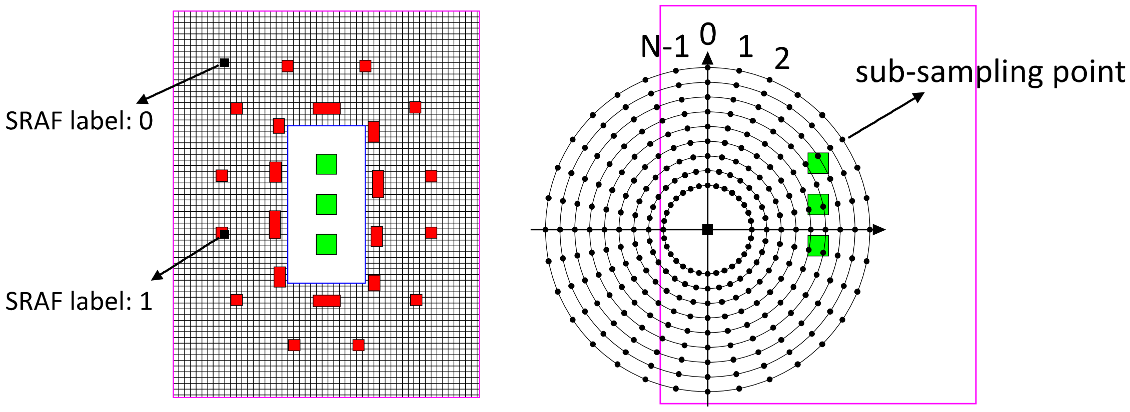
- **Jiang et al., "A fast machine learning-based mask printability predictor for OPC acceleration," ASPDAC'19**
  - Edge fragmentation and SRAF insertion are performed first
  - Two models are used for each checkpoint
    - One predicts whether the EPE exceeds a threshold
    - The other predicts the intensity value to determine edge shifting
  - Could be embedded into industrial OPC flows
  - Comparable to and faster than GAN-based models



[Jiang et al., ASPDAC'19]

SRAF Insertion with Binary Classification

- **Sub-resolution assist feature (SRAF) insertion**
  - Non-printable auxiliary patterns to enhance neighboring layout features
- **Xu et al., "A machine learning based framework for sub-resolution assist feature generation," ISPD'16**
- **Geng et al., "SRAF insertion via supervised dictionary learning," TCAD'20**
  - Concentric circle area sampling (CCAS) for feature extraction
  - Predict whether a grid is an SRAF grid

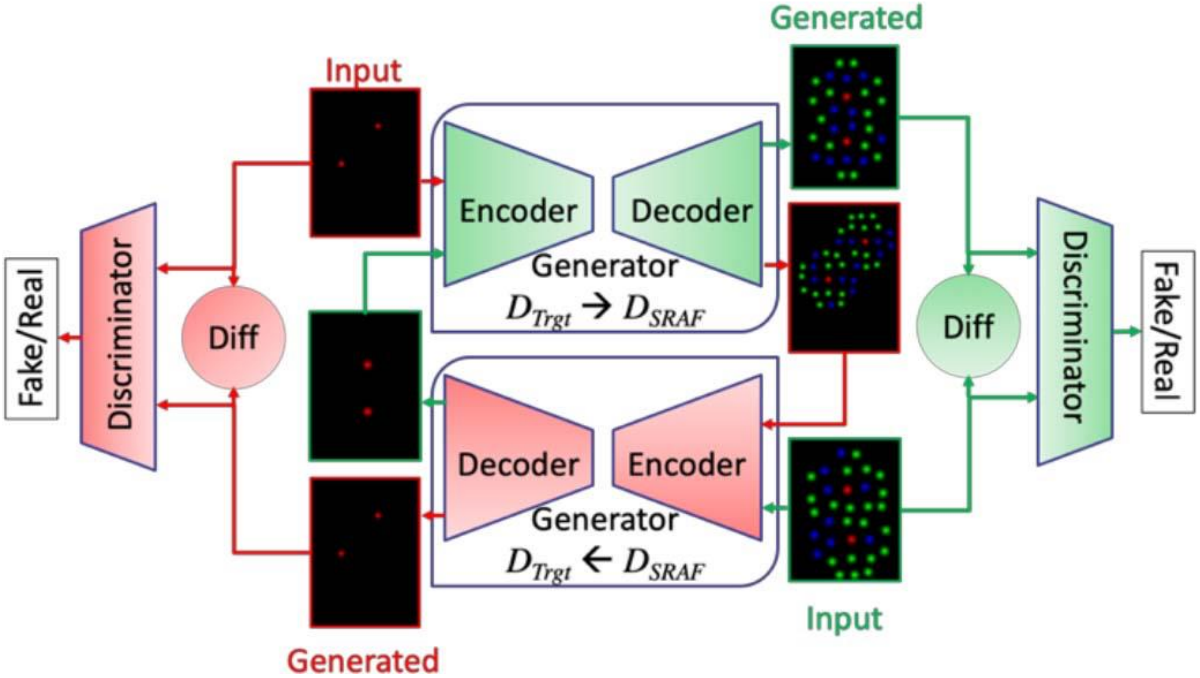


(a) (b)

[Xu et al., ISPD'16]

Image-based SRAF Insertion

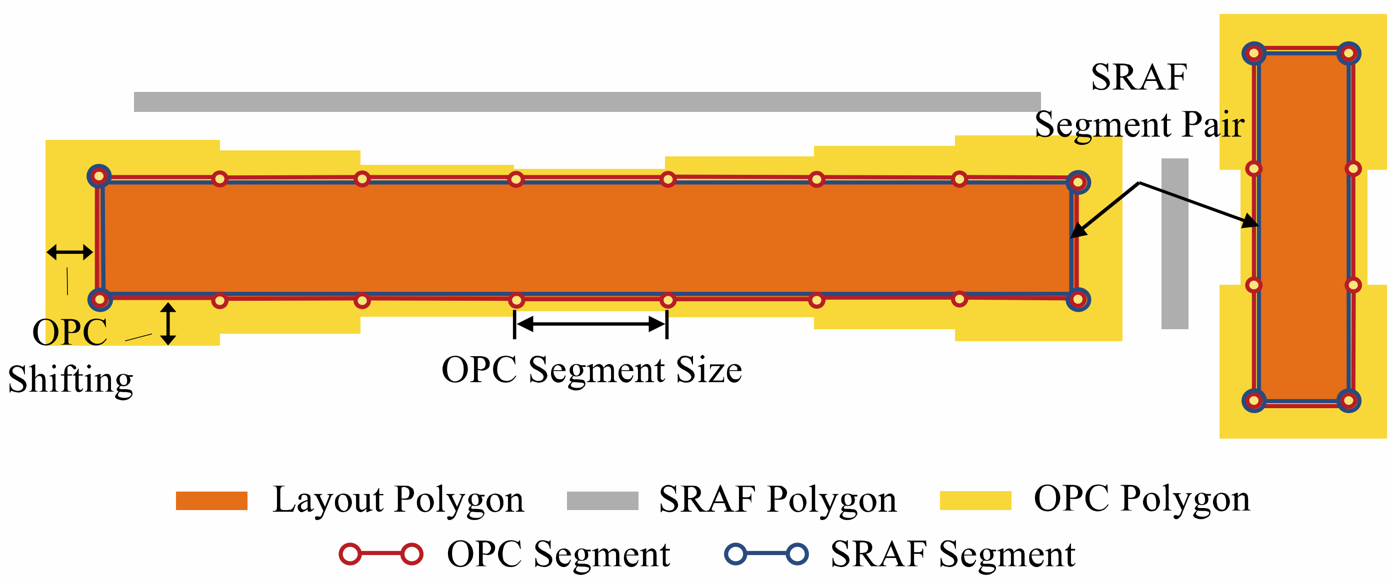
- **Alawieh et al., "GANSRAF: sub-resolution assist feature generation using conditional generative adversarial networks," TCAD'21**
  - CGAN-based
  - A CycleGAN architecture is adopted for training with unpaired data



[Alawieh et al., TCAD'21]

Mask Rule-Compliant Optimization

- **Yu et al., “Deep learning-based framework for comprehensive mask optimization,” ASPDAC’19**
  - Deep neural network (DNN)-based
  - ML models for both OPC and SRAF insertion
  - Edge-based OPC approach
  - Only consider limited numbers of SRAFs and SRAF dimensions



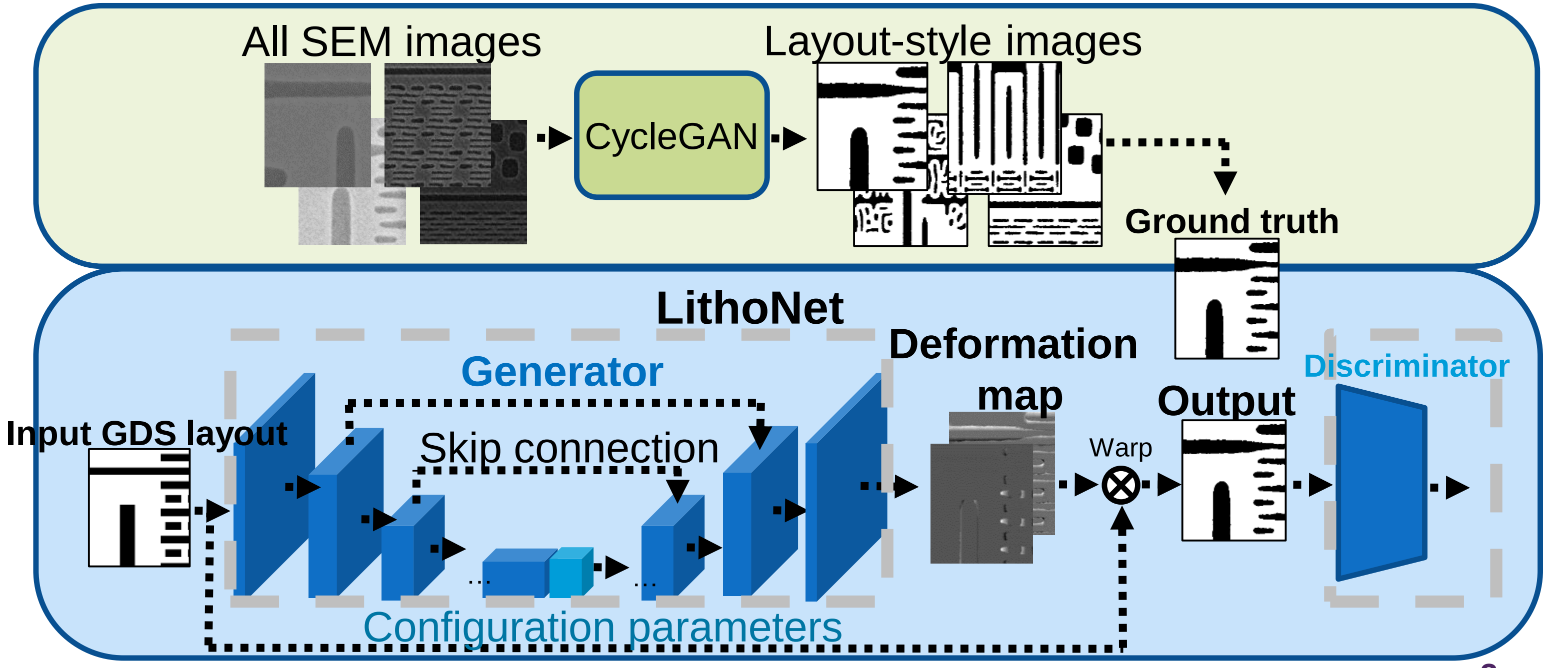
[Yu et al., ASPDAC’19]

THE EDA LAB
TAIWAN TECH

Data-driven Approaches from Simulation to Mask Optimization

LithoNet: A SEM Simulator

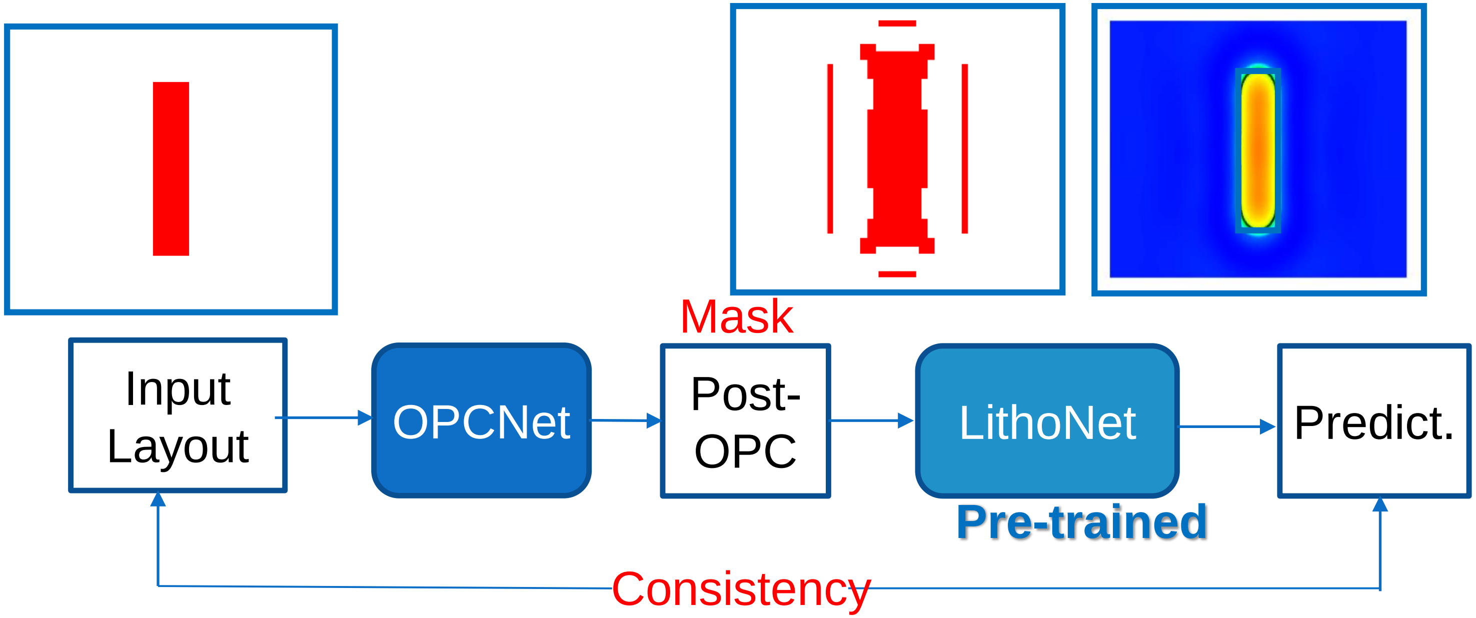
- **Shao et al., "From IC layout to die photograph: a CNN-based data-driven approach," TCAD'21**
- **LithoNet: GAN-based SEM simulator**
  - A CycleGAN extracts pattern contours of SEM images
  - The generator outputs a deformation map



[Shao et al., TCAD'21]

OPC with Self-Supervised Learning

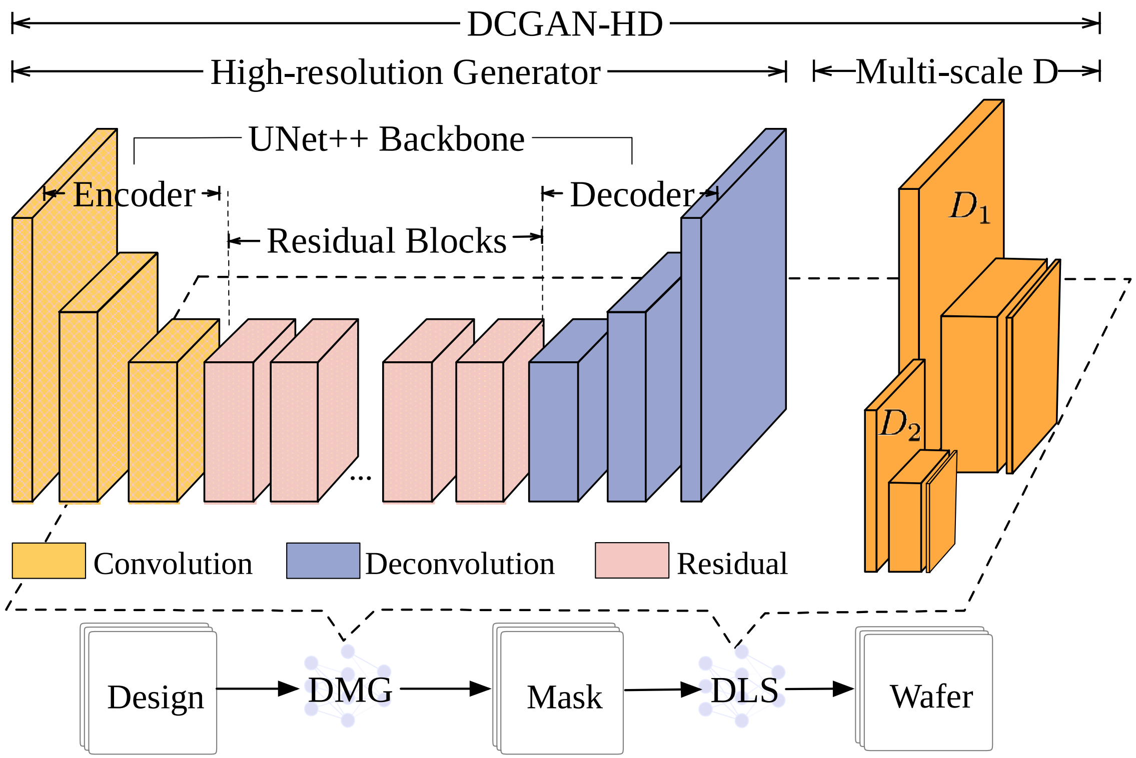
- **Shao et al., “From IC layout to die photograph: a CNN-based data-driven approach,” TCAD’21**
- **OPCNet: GAN-based OPC engine**
  - Self-supervised learning with the help of LithoNet
  - Optimized by using the input–output consistency loss



[Shao et al., TCAD’21]

DAMO with Enhanced DCGAN

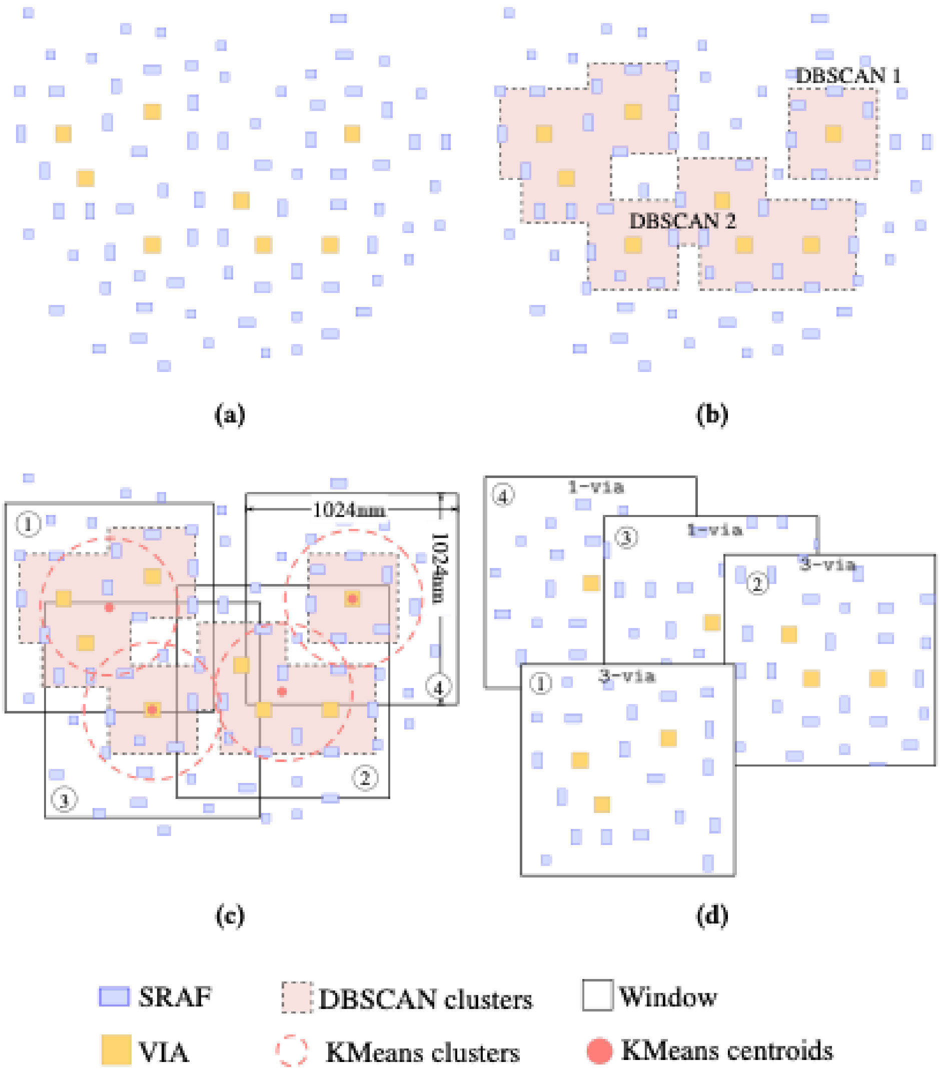
- **Chen et al., "DAMO: Deep agile mask optimization for full chip scale," TCAD'22**
  - DCGAN-HD: perform high-resolution feature extraction and high-resolution image synthesis



[Chen et al., TCAD'22]

Optimization for Full Chip

- **Chen et al., "DAMO: Deep agile mask optimization for full chip scale," TCAD'22**
  - Layout splitting for full-chip application
    - Identify high-via-density clusters
    - Assign each via to a specific window
    - Simulate/correct each window separately



[Chen et al., TCAD'22]

Future Research Directions

Future Directions

- **Data-driven approaches for complicated layouts**
  - Existing studies only consider contact/via hole layouts or simple and few layout clips
  - Complicated layouts are required to verify existing models
  - More sophisticated models and design strategies may be required
- **Simultaneous OPC and SRAF insertion with GAN-based models**
  - Unified models are desirable for both SRAF insertion and OPC
  - A GAN-based model may be developed
- **Full-chip simulation/mask optimization for complicated layouts**
  - The stitching problem of layout patterns emerges among windows


YUKO.FANG
THANKS
POPAPC@2015