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Mixed-Type Wafer Failure Pattern Recognition (Invited Paper)

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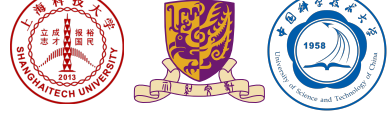
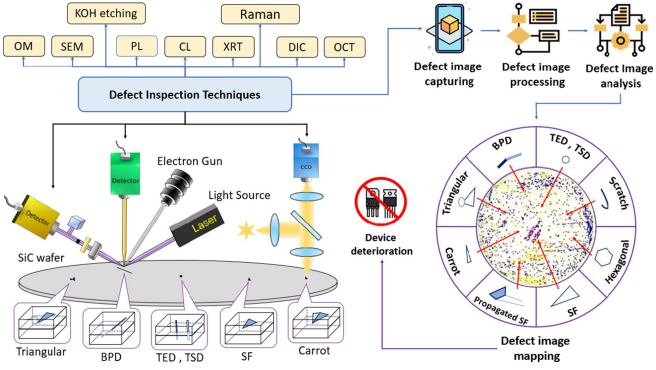
Jan. 18, 2023



Introduction

Wafer Defect Inspection

- Technology nodes shrinks, smaller but more complex circuits are etched on wafers
- Recognizing wafer defects is vital

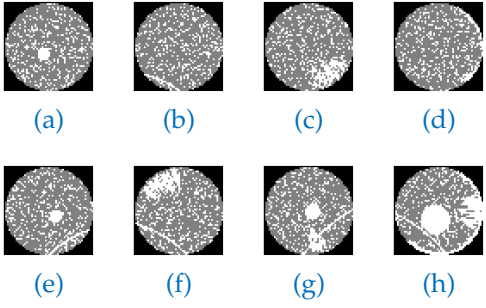


The defect inspection technologies in wafer manufacturing. [1]

[1] P.-C. Chen et al., "Defect Inspection Techniques in SiC," Nanoscale Research Letters, 2022.

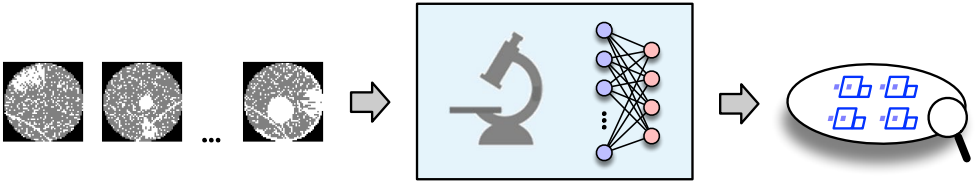
Some Wafer Defect Patterns

- Single-type defect patterns emerge and are coupled and shaped mixed-type patterns



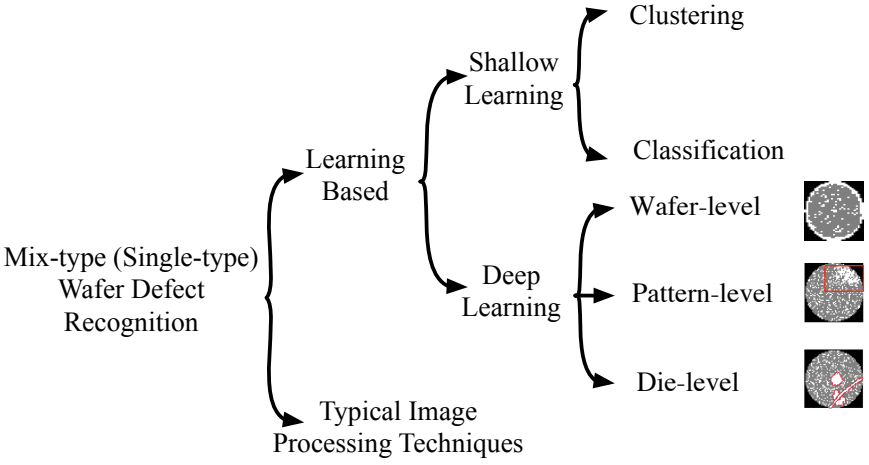
Some wafer map patterns in `MixedWM38` benchmark:
(a) Center; (b) Scratch; (c) Location; (d) Edge-Location;
(e) **2** single-type defects mixed (Center, Scratch);
(f) **2** single-type defects mixed (Scratch, Location);
(g) **3** single-type defects mixed (Center, Scratch, and Location);
(h) **4** single-type defects mixed (Center, Scratch, Location, and Edge-Location).

Wafer Defect Pattern Recognition Flow



The General Wafer Defect Pattern Recognition Flow.

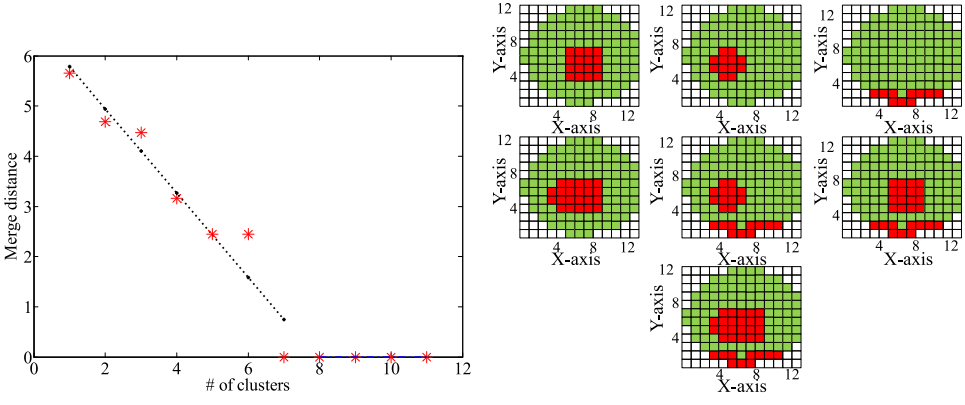
Current Methods For Wafer Defect Pattern Recognition



The taxonomy of prior arts.

Shallow Learning-based Recognition Paradigm

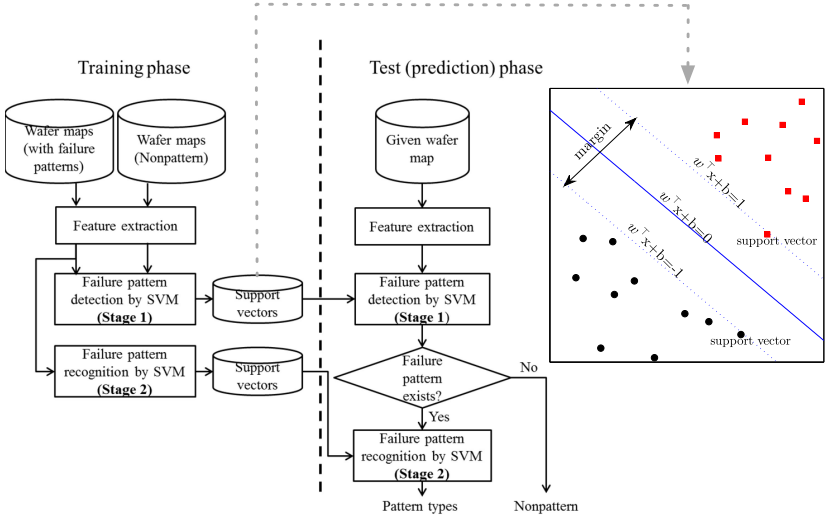
Clustering-based Methods



An example of clustering-based method. [1]

[1] M. B. Alawieh et al., "Identifying wafer-level systematic failure patterns via unsupervised learning," IEEE TCAD, 2017.

Typical Classification-based Methods

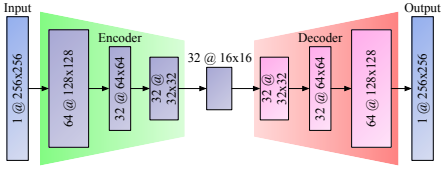


An example of typical classification-based method. [1]

[1] M.-J. Wu et al., "Wafer map failure pattern recognition and similarity ranking for large-scale data sets," IEEE TSM, 2015.

Deep Learning-based Recognition Paradigm

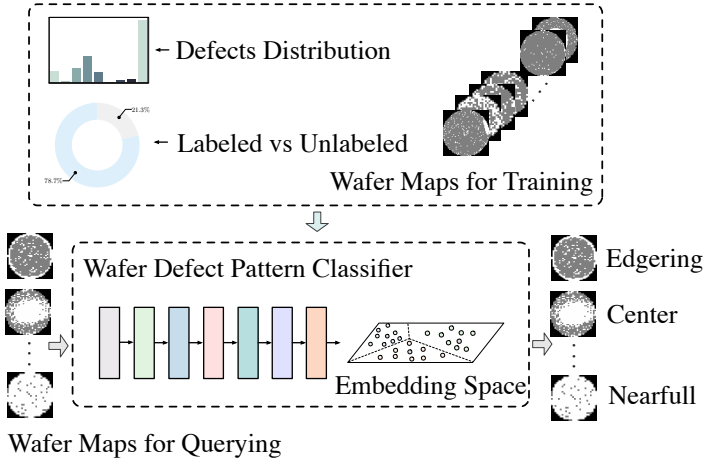
Wafer-level Frameworks (i)



The illustration of the data augmentation and selective wafer defect recognition network. [1]

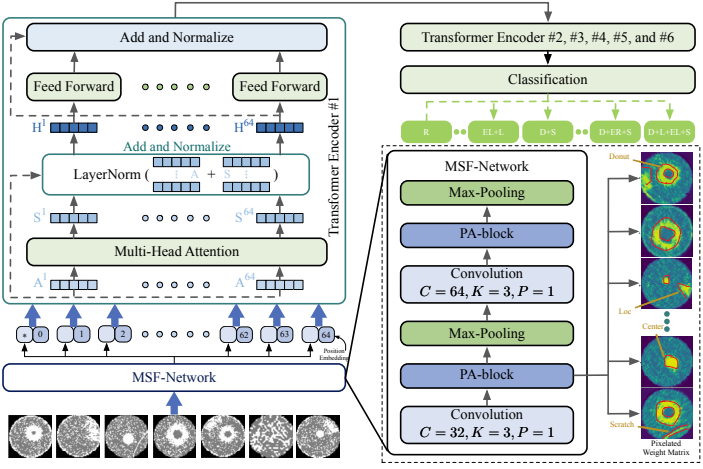
[1] M. B. Alawieh et al., "Wafer map defect patterns classification using deep selective learning," DAC, 2020.

Wafer-level Frameworks (ii)



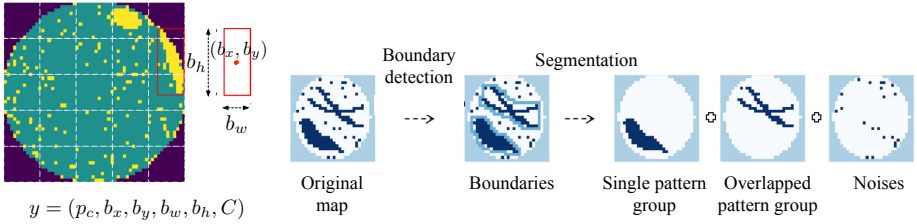
The proposed semi-supervised wafer failure pattern classifier. [1]

[1] H. Geng et al., "When wafer failure pattern classification meets few-shot learning and self-supervised learning," ICCAD, 2021.



The architecture of the transformer-based defect recognition. [1]

[1] Y. Wei et al., "Mixed-type wafer defect recognition with multi-scale information fusion transformer," IEEE TSM, 2022.



(a) An example of pattern-level recognition. [1]
(b) The segmentation example for the wafer defect detection. [2]

[1] P. P. Shinde et al., "Wafer defect localization and classification using deep learning techniques," IEEE Access, 2022.
[2] Y. Kong et al., "Qualitative and quantitative analysis of multi-pattern wafer bin maps," IEEE TSM, 2020.

Conclusion & Future Directions

Conclusion & Future Directions

- A survey of recent line of arts in wafer failure pattern recognition
- The conflict between the security of wafer information and the development of a learning-based method
- Rethinking deep learning-based algorithms: susceptible to perturbations, prior information incorporation, ...
- Considering extracting and fusing multi-level features from wafer-level to die-level
- ... ...

THANK YOU!