AutoFlex: Unified Evaluation And Design Framework for Flexible Hybrid Electronics

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Outline

1 Introduction

2 Unified Evaluation Framework for Flexible Hybrid Electronics

3 Quantitative Studies for Flexible Technologies

4 System Demonstration of Flexible Hybrid Electronics

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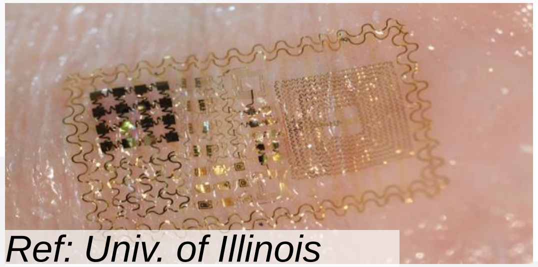
1. Introduction
2. Unified Evaluation Framework for Flexible Hybrid Electronics
3. Quantitative Studies for Flexible Technologies
4. System Demonstration of Flexible Hybrid Electronics

➢ Progress of Wearable Applications


Ref: Univ. of Illinois

Medical

Ref: The Medical Futurist

Fitness


Ref: NextFlex

Industrial/Military

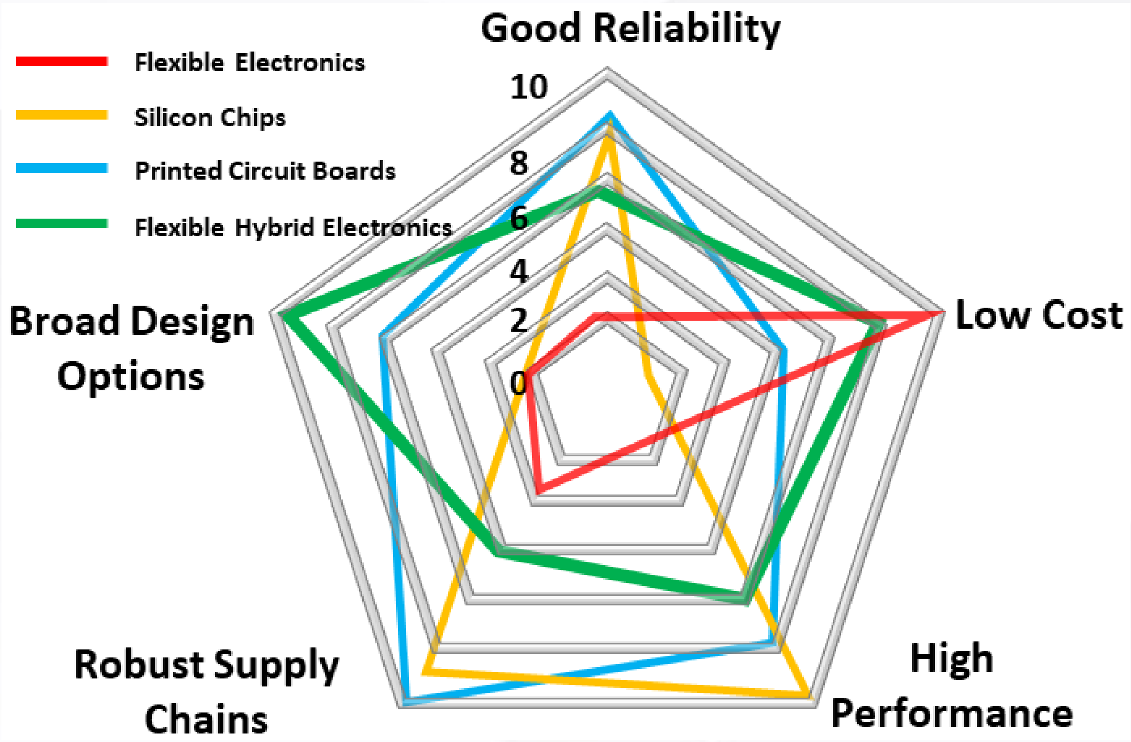
Source: Transparency Market Research & IDTechEx Report

- **Comparison between silicon and flexible technologies**

Traditional Silicon IC	**High Performance/Reliability; Small Variation**
	Poor Wearability; Limited Functionality; High Cost
Emerging Flexible Electronics	**Great Wearability; Diverse Functionality; Low Cost**
	Low Performance/Reliability; Large Variation

Flexible Hybrid Electronics(FHE) = Flexible Electronics +Silicon IC

➢ Advantages and challenges of FHE system



Challenges:

- Lack of standardized evaluation framework
- Fair comparison between various flexible technologies

Unified Evaluation Framework for Flexible Hybrid Electronics(FHE)

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1 Introduction

2 **Unified Evaluation Framework for Flexible Hybrid Electronics**

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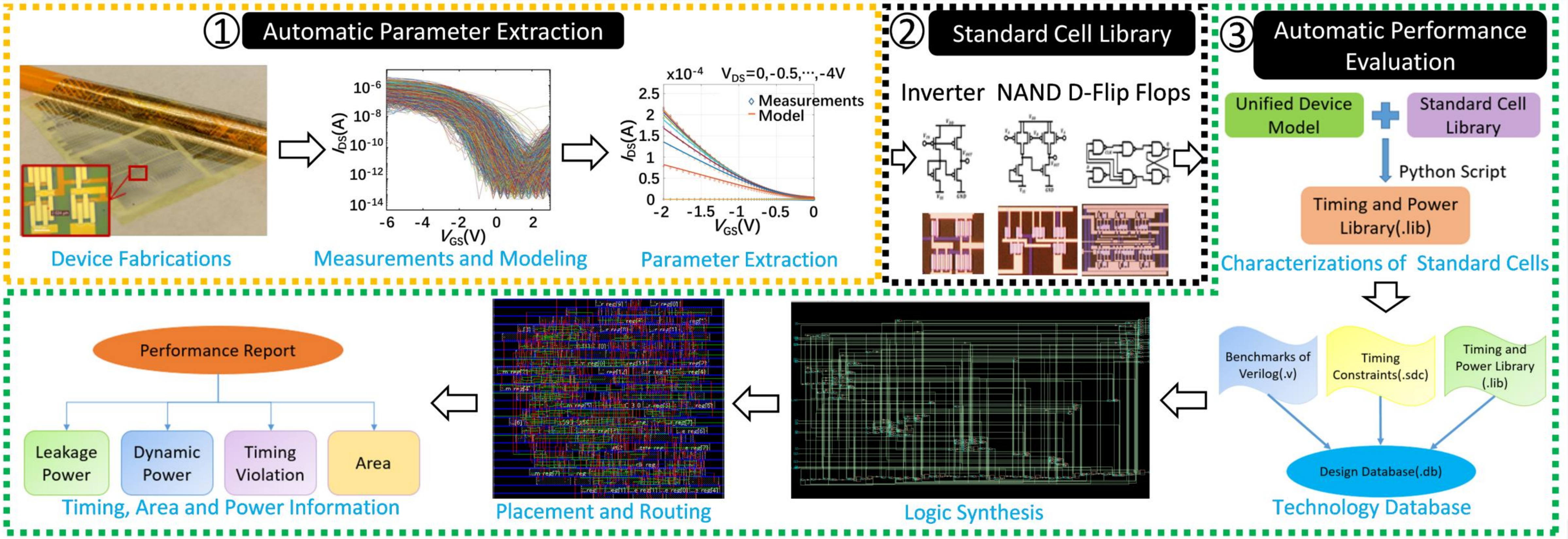
Unified Evaluation Framework for Flexible Hybrid Electronics

- **AutoFlex: Design Automation Flow for Flexible Hybrid Electronics**

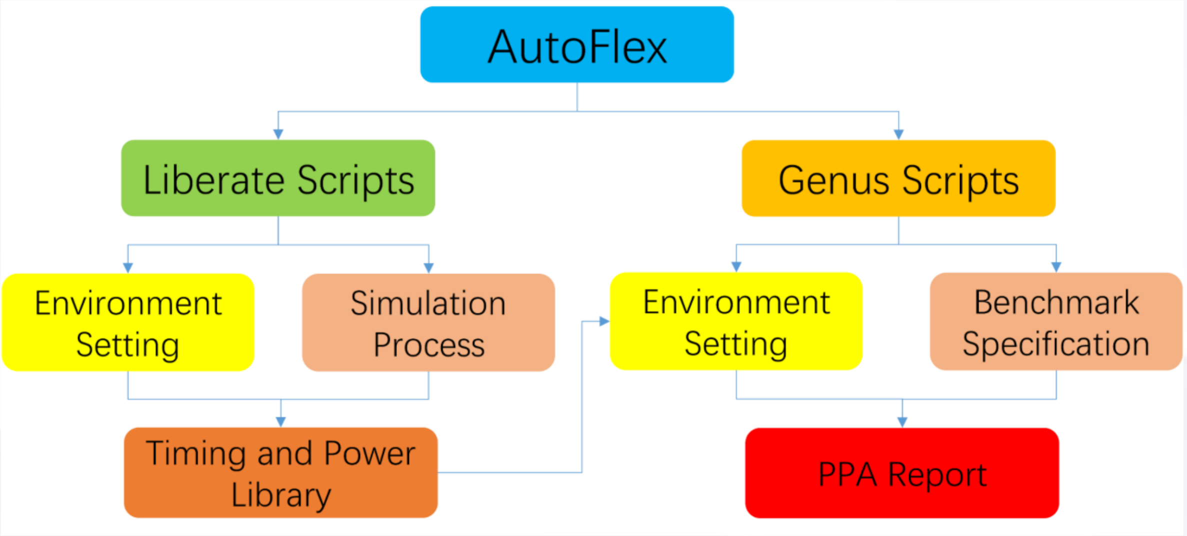


Unified Evaluation Framework for Flexible Hybrid Electronics

➢ AutoFlex Code Structure

► Inputs
- Key parameters of flexible transistor
- Netlists of standard cell library
- Evaluation benchmarks
- Environmental settings of working conditions and EDA tools

► Outputs
- Leakage power
- Dynamic power
- Maximum frequency
- Minimum chip area

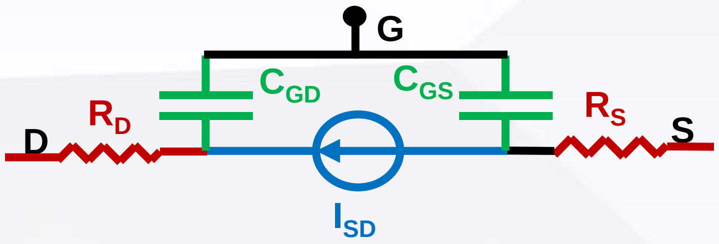


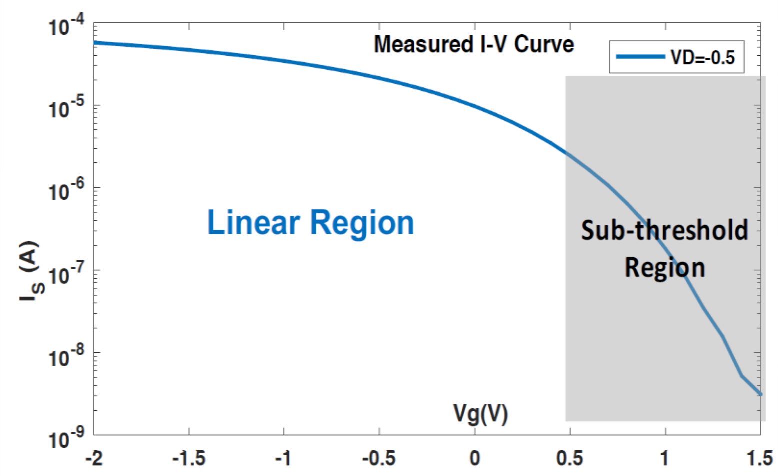
https://github.com/mtl2236/AutoFlex

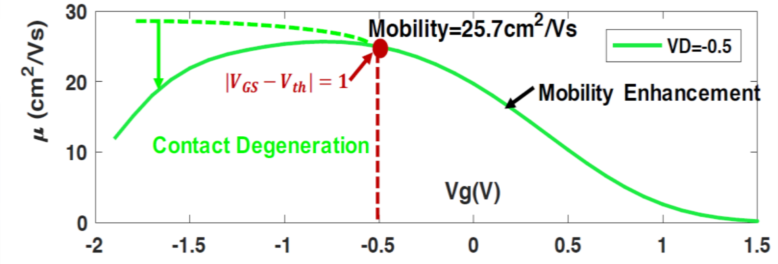
Unified Evaluation Framework for Flexible Hybrid Electronics

➢ Unified Compact Model for Various Flexible Devices

Charge Drift Model







Traditional CMOS Model: Linear Region

$$I_D \approx \frac{W}{L}\mu C_{ox}(V_{GS} - V_T - \frac{V_{DS}}{2})V_{DS}$$

Mobility Enhancement

$$\mu = \begin{cases} \mu_0(V_G - V_{th})^{\gamma}, & \text{N-type TFT} \\ \mu_0(V_{th} - V_G)^{\gamma}, & \text{P-type TFT} \end{cases}$$

Mobility Degeneration

$$\frac{\tilde{\mu}}{\mu} = \frac{1}{1 + kR_C(V_{th} + V_{SG})}; \quad k = \frac{W}{L}C_{ox}\mu$$

Unified Compact Model

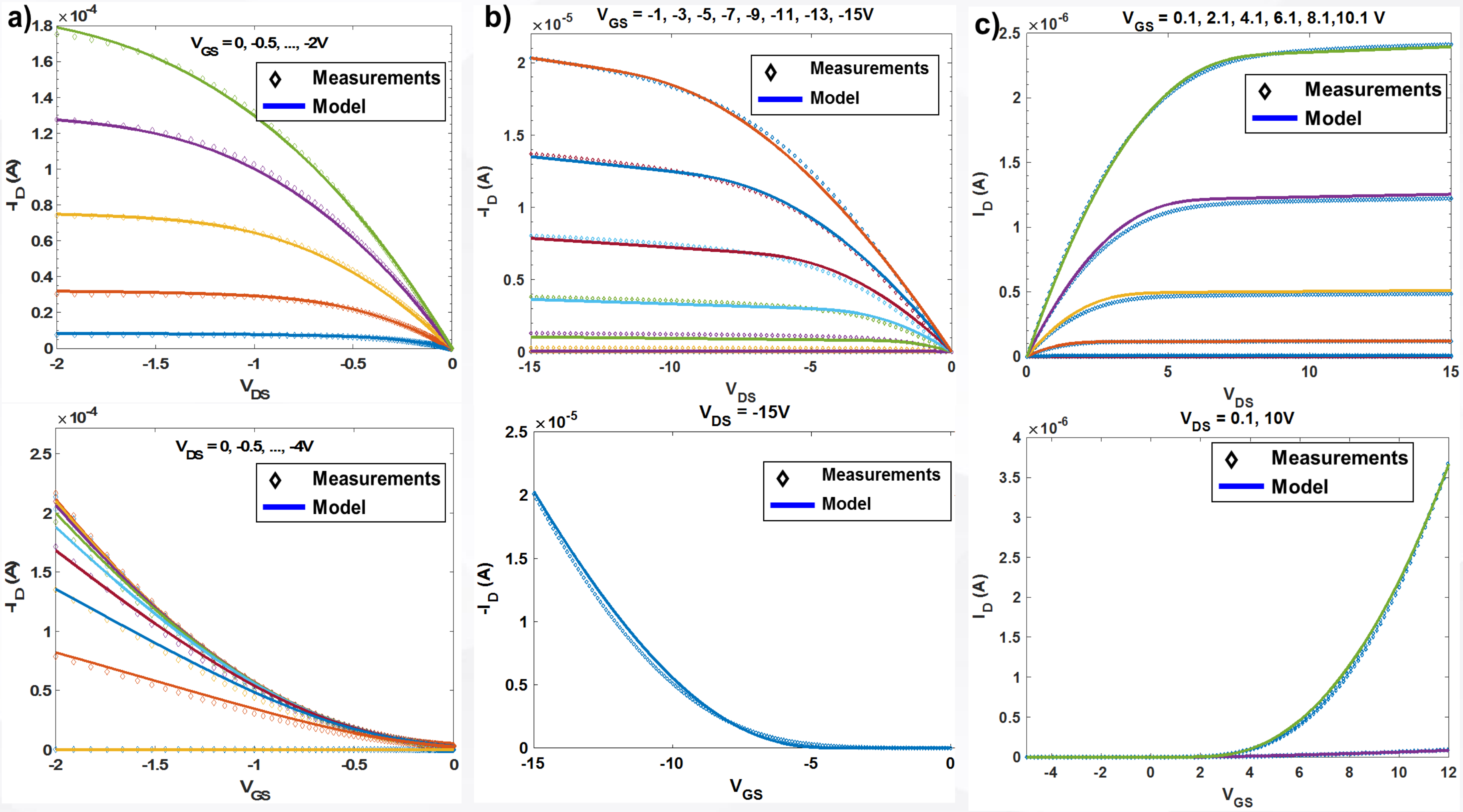
$$I_{SD} \approx \begin{cases} k'\{(V_{th} - V_{GS}) - \frac{1+\gamma}{2}V_{SD}\}V_{SD}, & V_{DS} > V_{GT} \\ \frac{k'}{(\gamma+2)}(V_{th} - V_{GS})^2, & V_{DS} \le V_{GT} \end{cases}$$

$$k' = k(V_{th} - V_{GS})^{\gamma}; \quad V_{GT} = V_{GS} - V_{th}$$

Ref: **L. Shao** et al, DATE, 2018, (**Best Paper Award Nominations**) **DOI:** 10.23919/DATE.2018.8342058

Unified Evaluation Framework for Flexible Hybrid Electronics

➢ Unified Compact Model for Various Flexible Devices



CNT TFT　　Organic TFT　　IGZO TFT

Ref: **L. Shao** et al, DATE, 2018, (**Best Paper Award Nominations**) **DOI:** 10.23919/DATE.2018.8342058

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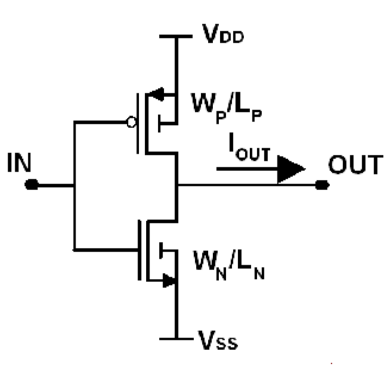
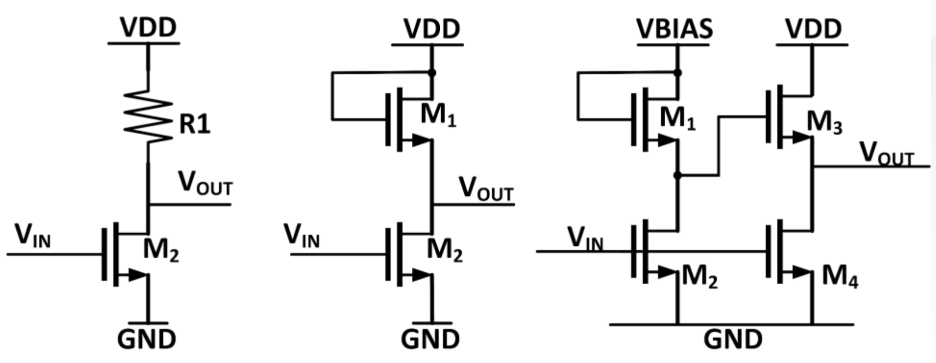
Quantitative Studies for Flexible Technologies

➢ Circuit Topology Comparisons



CMOS

VS



Resistive-Load | Diode-Load | Pseudo-E

Table 3: Performance Comparisons of Different Mono-type Inverters

Mono-type Structures	Diode-Load	Resistive-Load	Pseudo-E
Output High Voltage(V)	2.54	3.30	3.30
Output Low Voltage(V)	0.56	0.22	0.05
Output Rise Time(ns)	76.10	27.88	45.26
Output Fall Time(ns)	53.31	23.70	37.89

Minimum output voltage loss

Minimum transition time

Table 4: Leakage Power Comparison of CMOS and Mono-type Structures

Benchmarks	Leakage Power consumption(nW)			
	CMOS	Pseudo-E	Diode-Load	Resistive-Load
encoder_8to3bit	0.24	1.55e+7	4.56e+6	1.09e+6
adder_16bit	4.70	1.58e+8	7.27e+7	1.37e+7
multiplier_8bit	10.52	5.86e+8	1.93e+8	3.72e+7

CMOS structure has absolute advantages in reducing leakage power

Quantitative Studies for Flexible Technologies

➢ Parameters Extraction And Standard Cell Library Characterization

Table 1: Parameters for Emerging Flexible Technologies

Device Type	CNT	IGZO	OTFT	2D/MoS_2	Silicon
Device Width (μm)	5	5	5	5	5
Channel Length (μm)	0.6	0.6	0.6	0.6	0.6
Gate Unit Capacitance(nF/cm^2)	110	55	55	150	
Threshold Voltage(V)	0.5	0.9	-0.5	0.4	
Sub-threshold Swing($Vdec^{-1}$)	0.18	0.26	0.062	0.074	
Effective Mobility($cm^2V^{-1}s^{-1}$)	55	74	5.7	55	
Contact Resistance R_C (Ω)	1000	2500	1450	2900	
λ (V^{-1})	0.064	0.002	0.028	0.055	
γ (-)	0.20	0.3	0.5	0.19	

Table 2: Standard Cell Library

Logic Cells	Drive Strengths
AND2, OR2, NAND2, NOR2	X1,X2,X4
AND3, OR3, NAND3, NOR3	X1
AOI21, AOI22, AOI221, AOI222	X1
OAI21, OAI22, OAI221, OAI222	X1
ADDF, ADDH	X1
DFFQ/R, MUX2/4, XOR2, XNOR2	X1, X2
INV, BUF	X1,X2,X4,X8,X16,X32

Key parameters of flexible technologies extracted from published data

Flexible standard cell library

Ref:

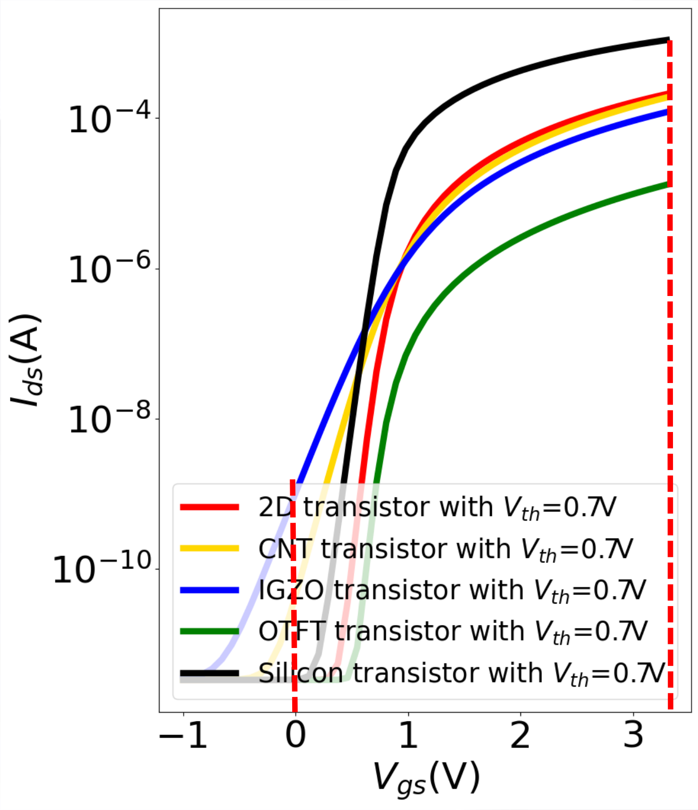
Jianshi. Tang et al, Nature Electronics, 2018, **DOI:**10.1038/s41928-018-0038-8

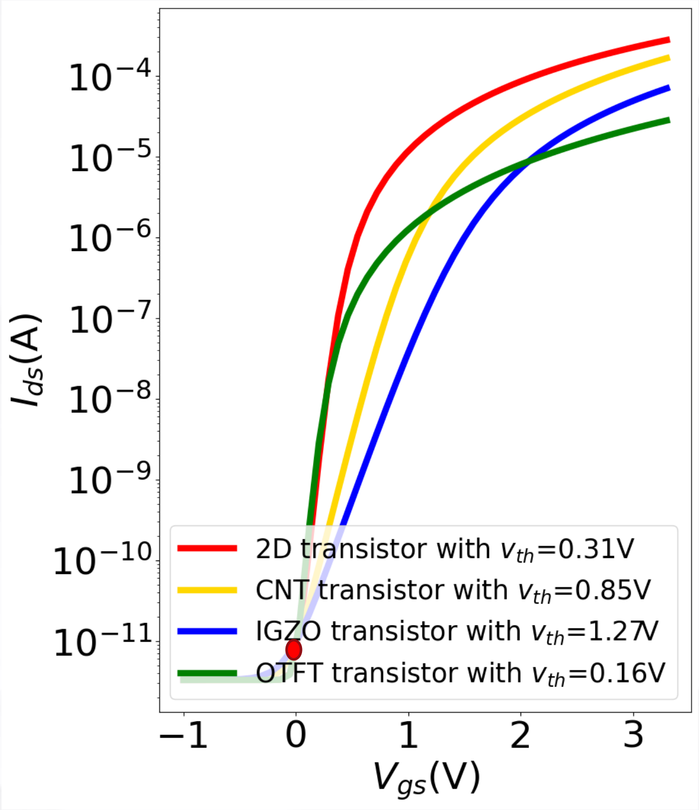
Jiazhen. Sheng et al, ACS Applied Materials & Interfaces, 2019, **DOI:**10.1021/acsami.9b14310

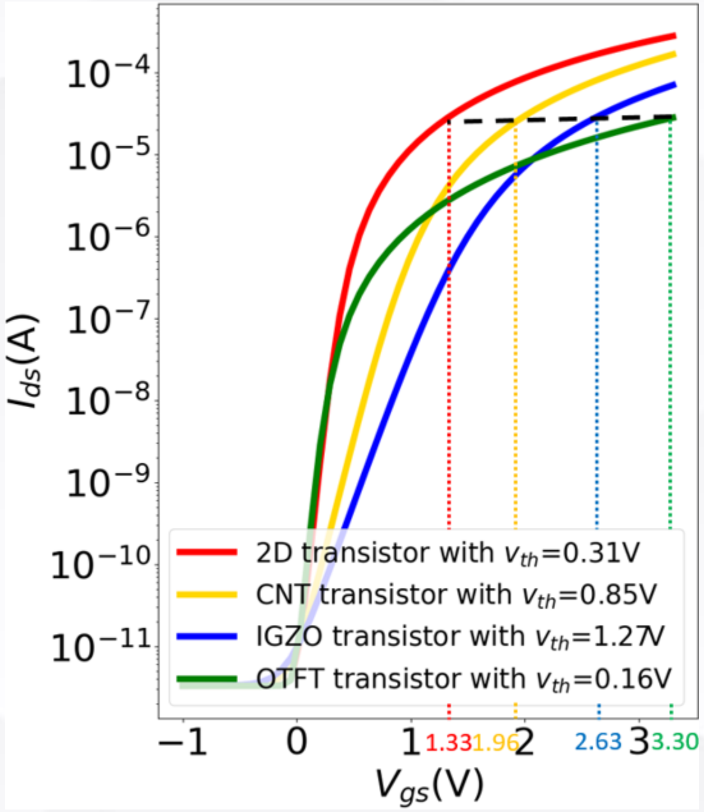
James W. Borchert et al, Nature Communications, 2019, **DOI:**10.1038/s41467-019-09119-8

Na. Li et al, Nature Electronics, 2020, **DOI:**10.1038/s41928-020-00475-8

➢ Transistor Level Evaluations







Config.1: same V_{DD} and V_{th}

Config.2: same V_{DD} and variable V_{th} to get same I_{off}

Config3: variable V_{DD} and V_{th} to get same I_{on}

Quantitative Studies for Flexible Technologies

➢ System Level Power And Performance Evaluations

Table 5: Power Comparisons Between Different Flexible Technologies at 5MHz with Device Configurations in Fig. 4(c)

Benchmarks(f = 5MHz)	Leakage Power consumption(nW)				Dynamic Power consumption(μW)			
	CNT	IGZO	OTFT	2D/MoS_2	CNT	IGZO	OTFT	2D/MoS_2
s820	5.08	7.67	10.49	2.55	75.18	59.42	117.75	43.13
s1196	10.75	16.98	22.92	5.49	186.59	168.70	288.70	117.91
s1423	23.80	33.09	50.43	11.40	553.91	498.70	842.28	345.11
RFID Tag Logic	79.84	115.80	169.38	41.75	754.63	670.16	1159.96	480.88
darkriscv	862.92	873.42	1713.18	377.10	7231.58	6423.86	11103.2	4536.70

Minimum leakage power

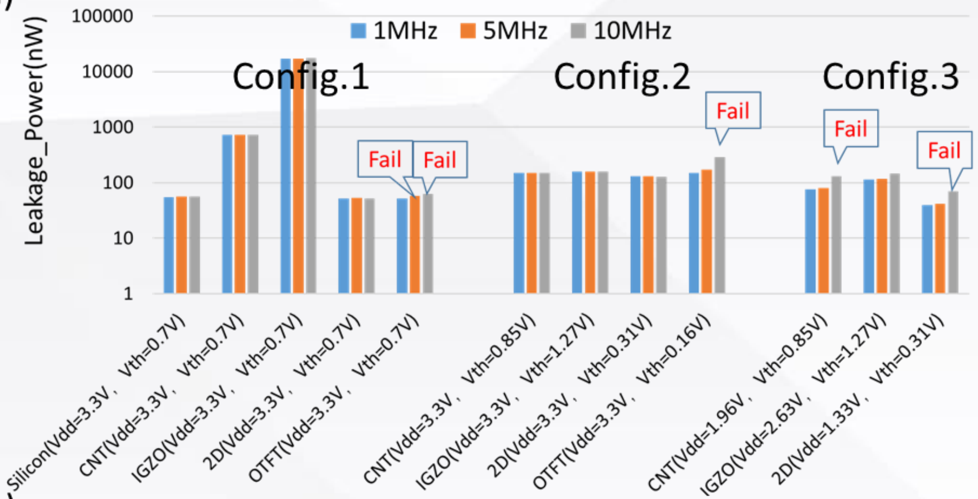
Minimum dynamic power

High mobility and low SS device → Low working voltage → Reducing dynamic and leakage power

Quantitative Studies for Flexible Technologies

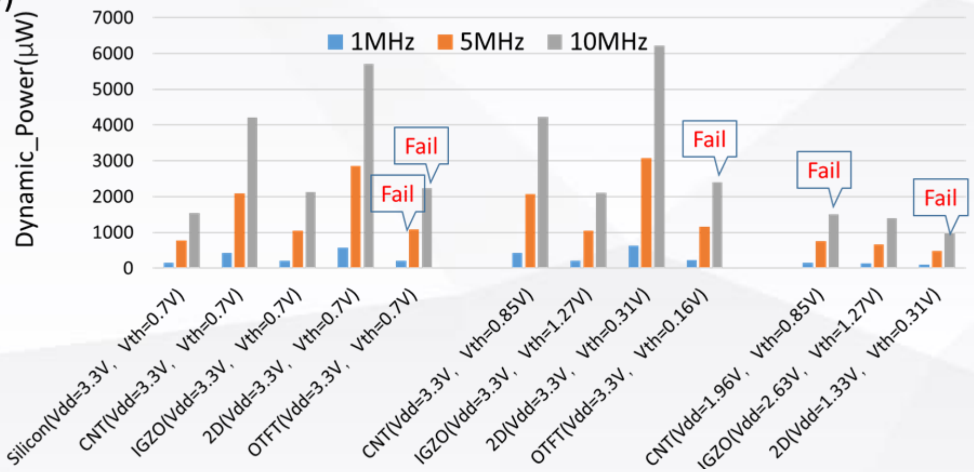
➤ System Level Power And Performance Evaluations

a)



Similar leakage power as silicon designs by adjustment of Vth

b)



Large difference in dynamic power because of difference in gate capacitance and parasitics

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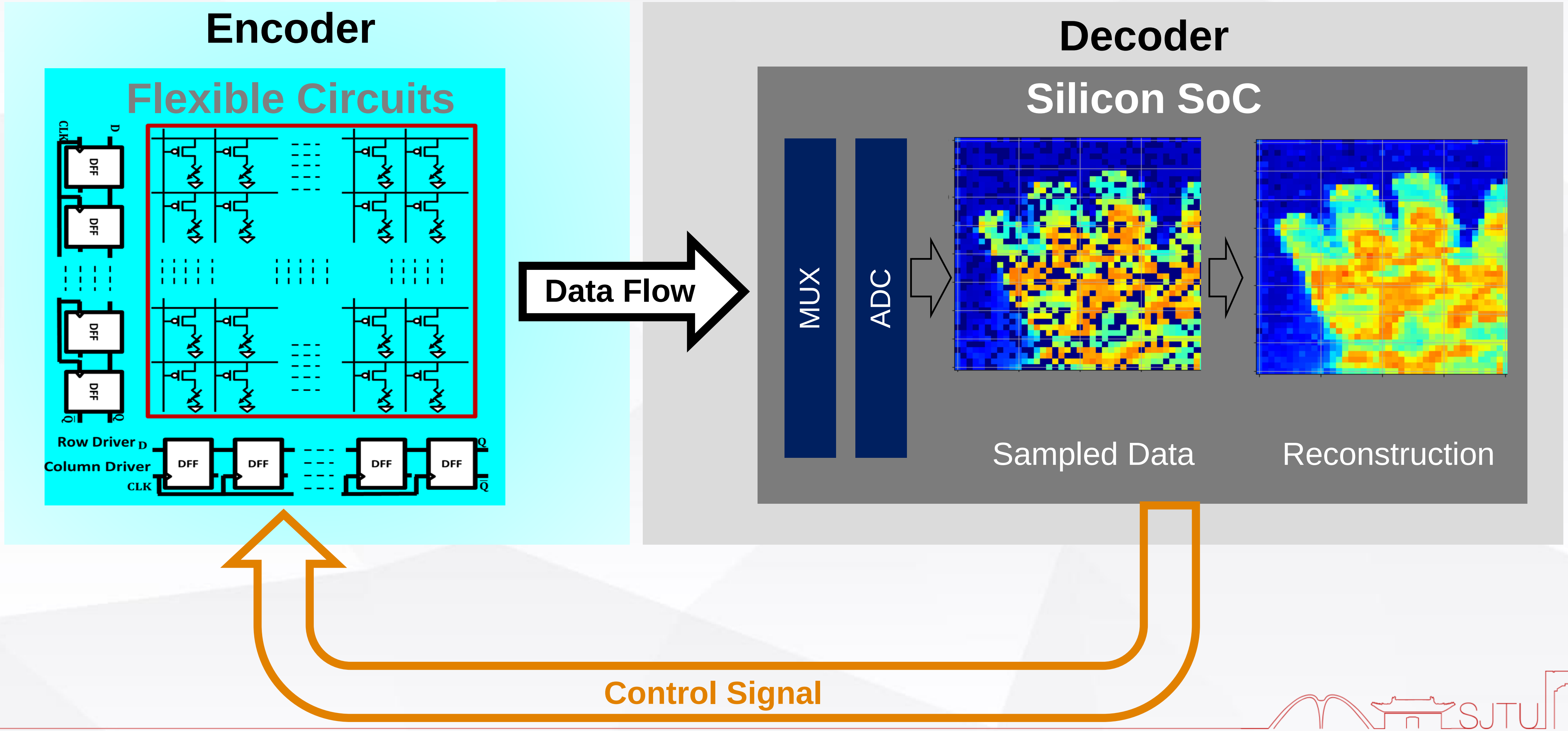
System Demonstrations of Flexible Hybrid Electronics

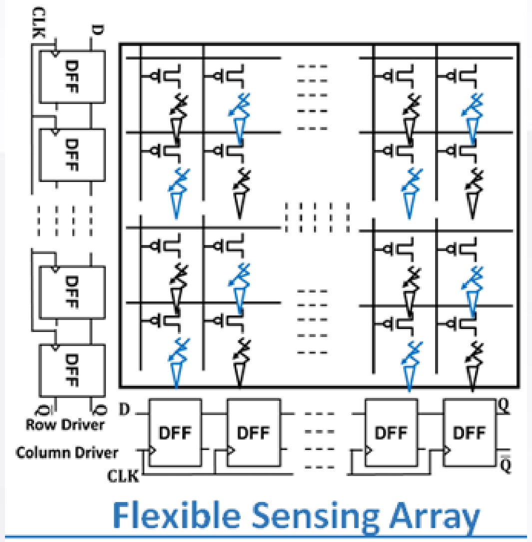
- **Structure of Demonstration**

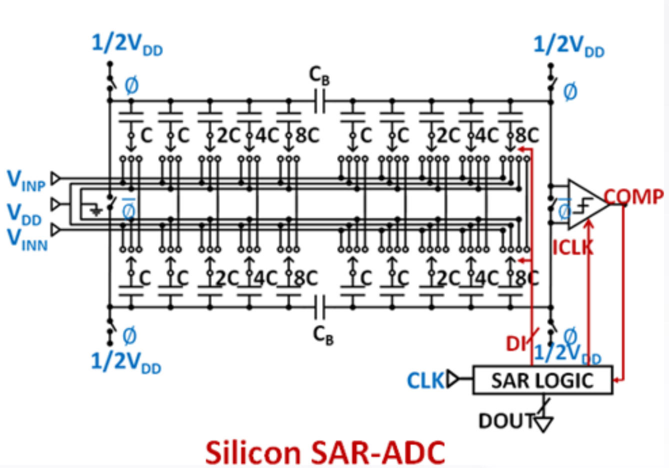


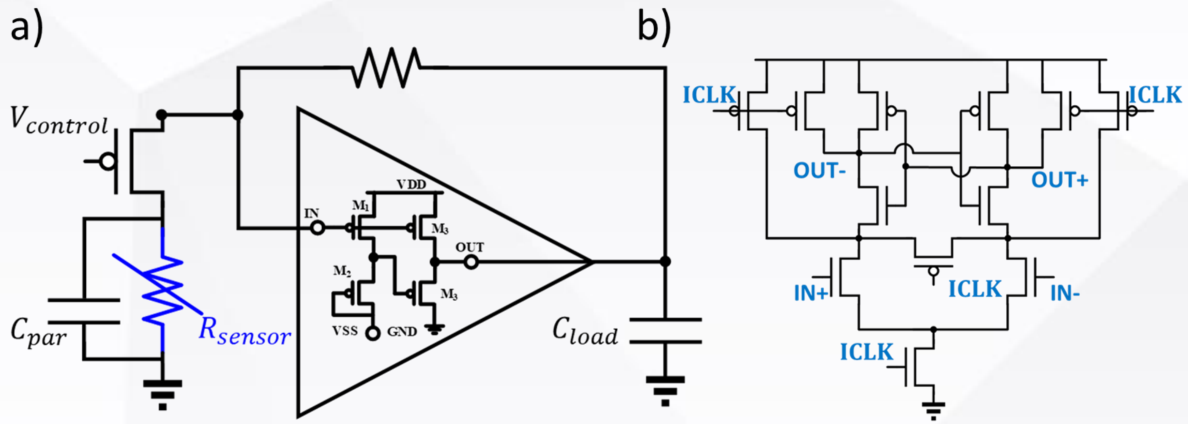
Ref: **L. Shao** et al, DAC, 2020, **DOI:** 10.1109/DAC18072.2020.9218570

System Demonstrations of Flexible Hybrid Electronics

➢ Details of Demonstration







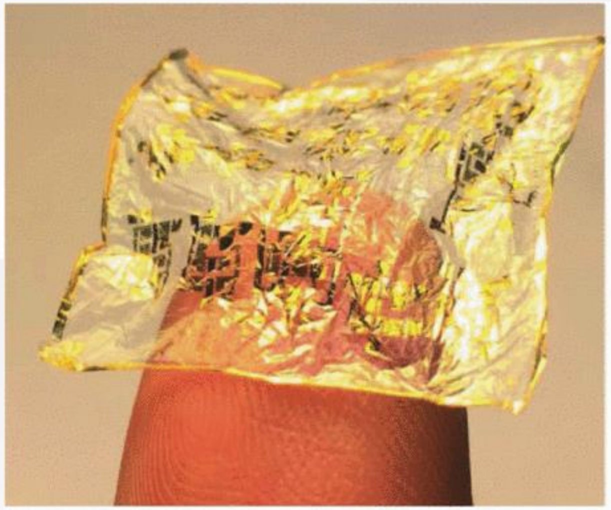
Active Matrix Sensor Array

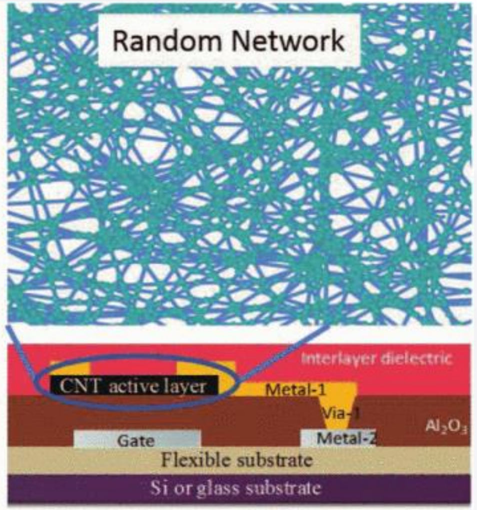
Silicon Analog-to-Digital Converter

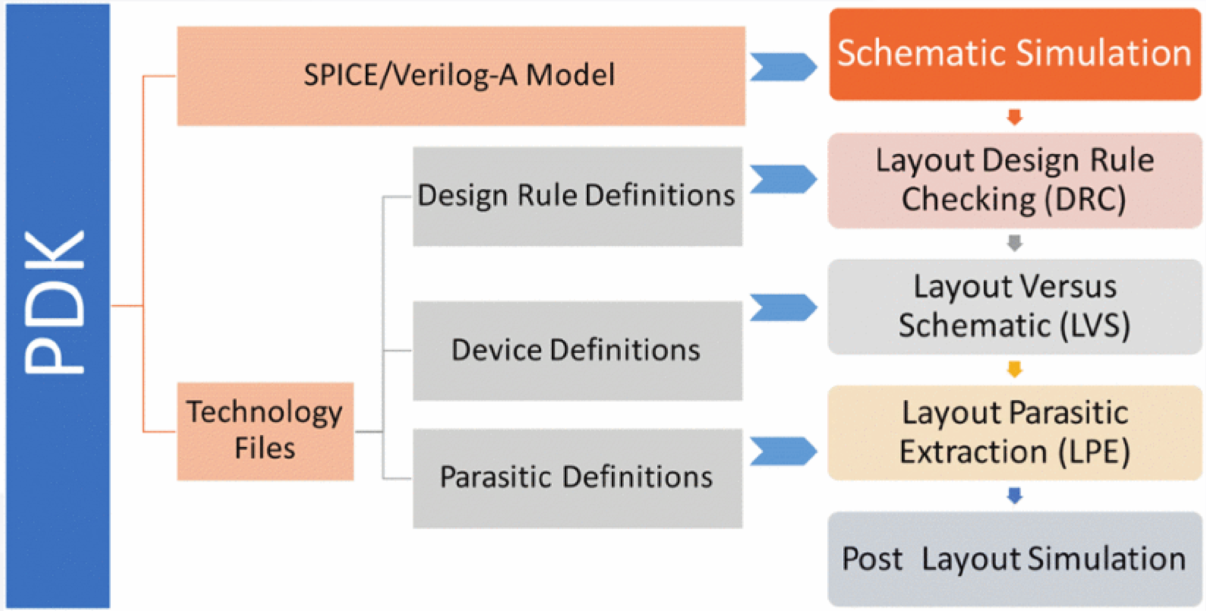
Transimpedance Amplifier

Ref: **L. Shao** et al, DAC, 2020, **DOI:** 10.1109/DAC18072.2020.9218570

Process design kit for flexible hybrid electronics







Load Technology files: {
Layer Assignments;
Define Material Properties;
Define Physical Constraints}
DRC Statements : {
Local Layer Definitions;
Layer Derivations;
Rule Check Comments}
LVS Statements : {
Device Recognition;
Layout Netlist Generating;
Netlists Equivalent Checking}
LPE Statements: {
Parasitic Recognition;
Parasitic Netlist Generating}

Ref: **L. Shao** et al, ASP-DAC, 2018, **DOI:** 10.1109/ASPDAC.2018.8297396

Conclusion And Future Work

➢ Contributions

- Unified evaluation framework for flexible hybrid Electronics
- Quantitative studies for flexible technologies
- System demonstration of flexible hybrid electronics

https://github.com/mtl2236/AutoFlex

➢ Future Work

- Power and signal integrity analysis of FHE system
- Make “AutoFlex” adapt to more open-sourced EDA tools
- Physical on-chip validation about the simulation result

➢ Acknowledgement

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- Mr. Zhihui Deng

Thank you and Q&A