BoCNT: A Bayesian Optimization Framework for Global CNT Interconnect Optimization

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January 22th, 2024

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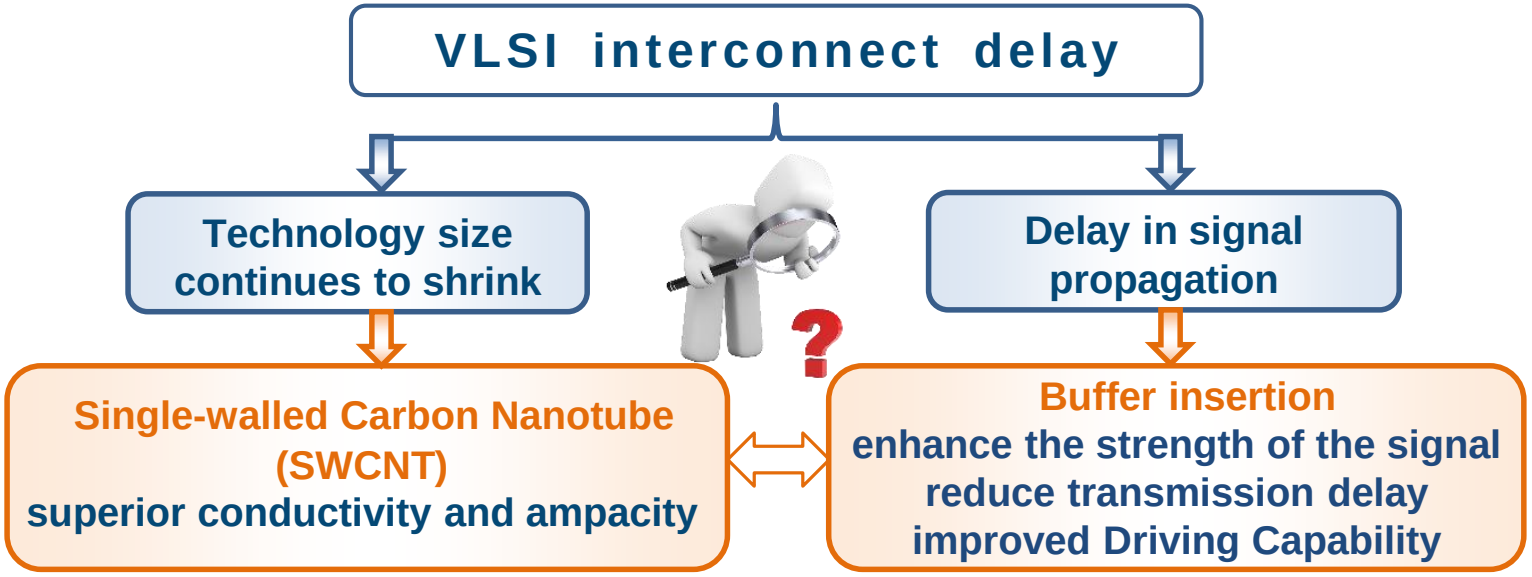
Outline

- Introduction
- Problem Formulation
- The Proposed Framework
  - Overview
  - CNT interconnect model
  - Bayesian co-optimization
  - Acquisition function
- Experimental Results and Summary

Introduction (1/6)
Background



Introduction (2/6)
CNT Interconnect

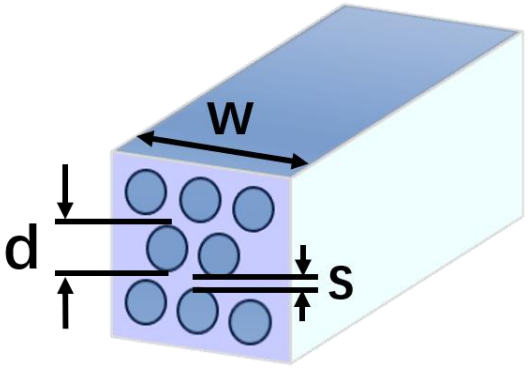


Fig. 1. SWCNT Bundle Section

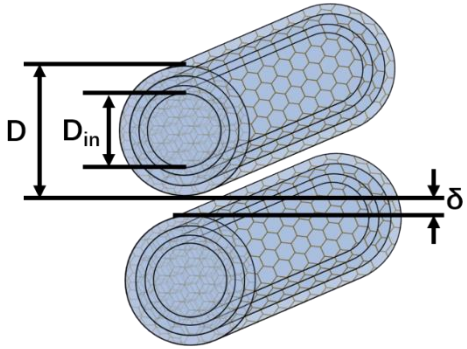


Fig. 2. MWCNT Bundle Section

- **Advantage**
- High mechanical strength
- Friendly preparation process
- **Disadvantage**
- Structural inhomogeneity

- **Advantage**
- Stability structures
- High conductivity
- **Disadvantage**
- Complex preparation process

Introduction (3/6)
Motivation

(1) The design parameters of CNT interconnect will have a complex impact on the delay of CNT interconnect
(2) Only perform buffer insertion optimization is not enough to obtain the optimal CNT interconnect performance

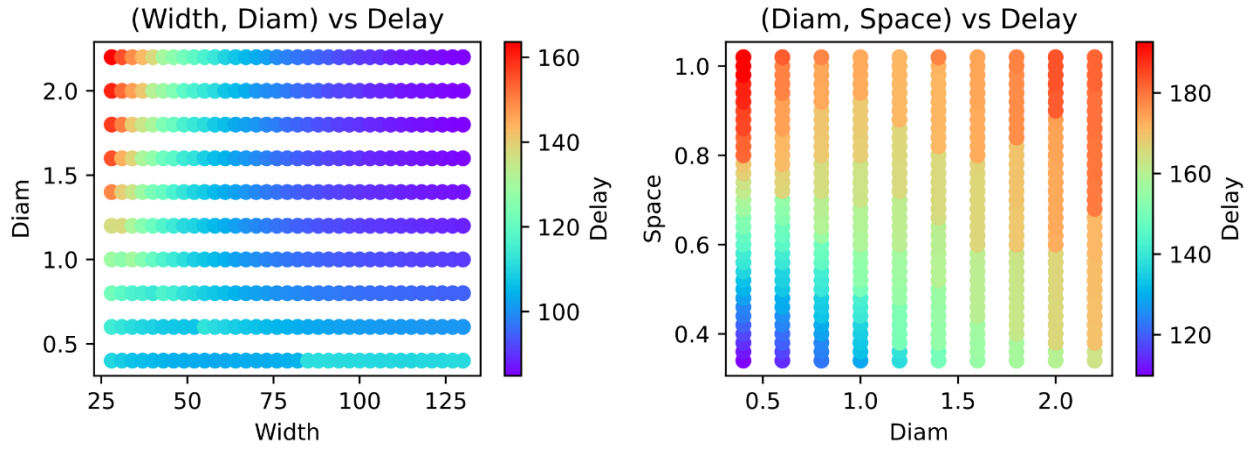


Fig. 3. Delay distributions with different CNT geometric parameters

Introduction (4/6)
Bayesian Optimization

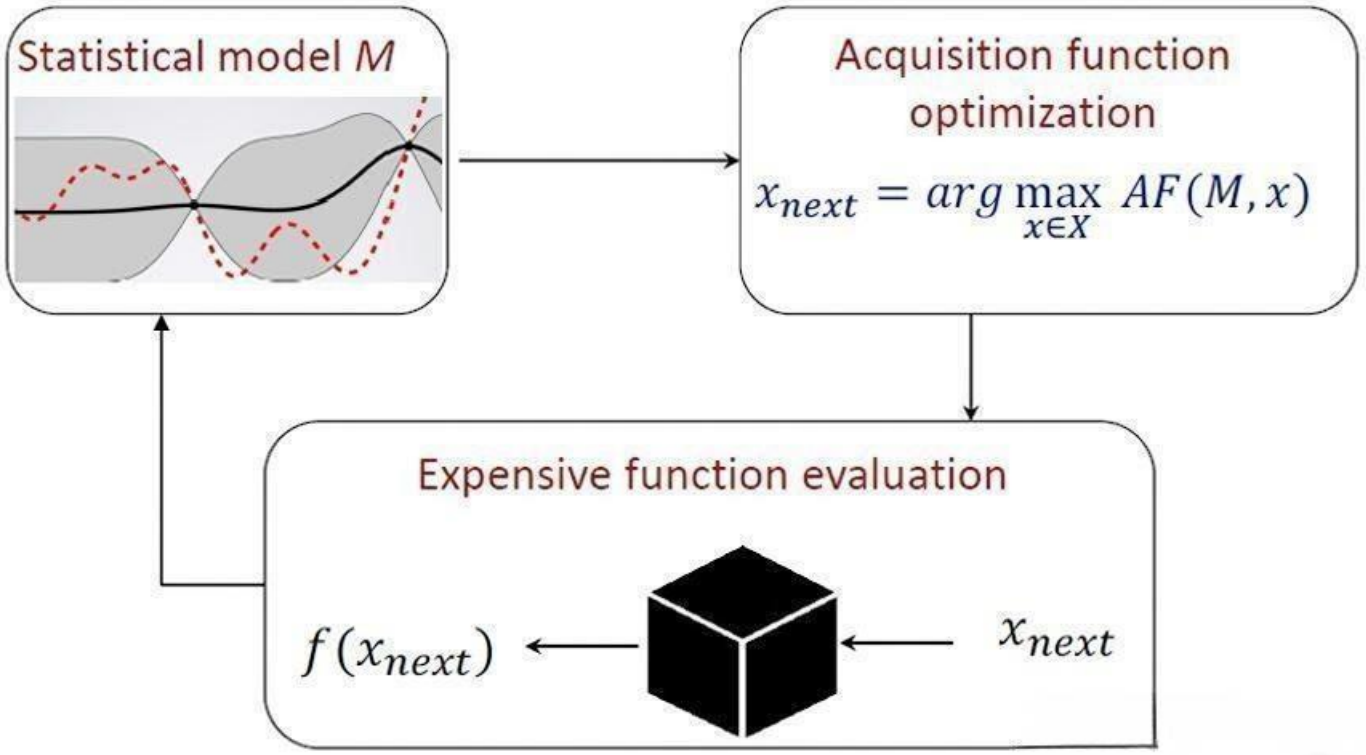


Fig. 4. The Three Elements of Bayesian Optimization

Introduction (5/6)
Related Work

- **Buffer insertion algorithm**
  - SWCNT interconnection for VLSI physical design.

    ➡The first CNT buffering technique based on the VGDP[1]
  - Selecting the buffer positions in a wiring tree such that the "Elmore delay" is minimal.➡ Depth-first search[2]
  - Accelerate the optimal buffer insertion process.

    ➡Predictive pruning, candidate tree, fast redundancy check[3]
- **CNT interconnection model**
  - Practical applicability of carbon nanotube bundles as VLSI circuit interconnects. ➡The equivalent circuit model of CNT bundle[4]

[1] L. Liu and S. Hu, "Buffering single-walled carbon nanotubes bundle interconnects for timing optimization," ISVLSI, pp.362-367, 2014.
[2] LPPP V. Ginneken, "Buffer placement in distributed RC-tree networks for minimal Elmore delay," IEEE ISCAS, pp.865-868, 1990.
[3] W. Shi and Z. Li, "A fast algorithm for optimal buffer insertion," IEEE TCAD, pp. 879-891, 2005.
[4] N. Srivastava and K. Banerjee, "Performance analysis of carbon nanotube interconnects for VLSI applications," IEEE ICCAD, pp. 383-390, 2015.

Introduction (6/6)
Contributions

- Contributions
  - Establish a parameter-dependent model of bundled SWCNT interconnects.
  - Propose a Bayesian optimization framework for CNT interconnect optimization considering interconnect design parameters and buffer insertion simultaneously.
  - The power delay product (PDP) can be improved by 17% on average compared with the-state-of-art work

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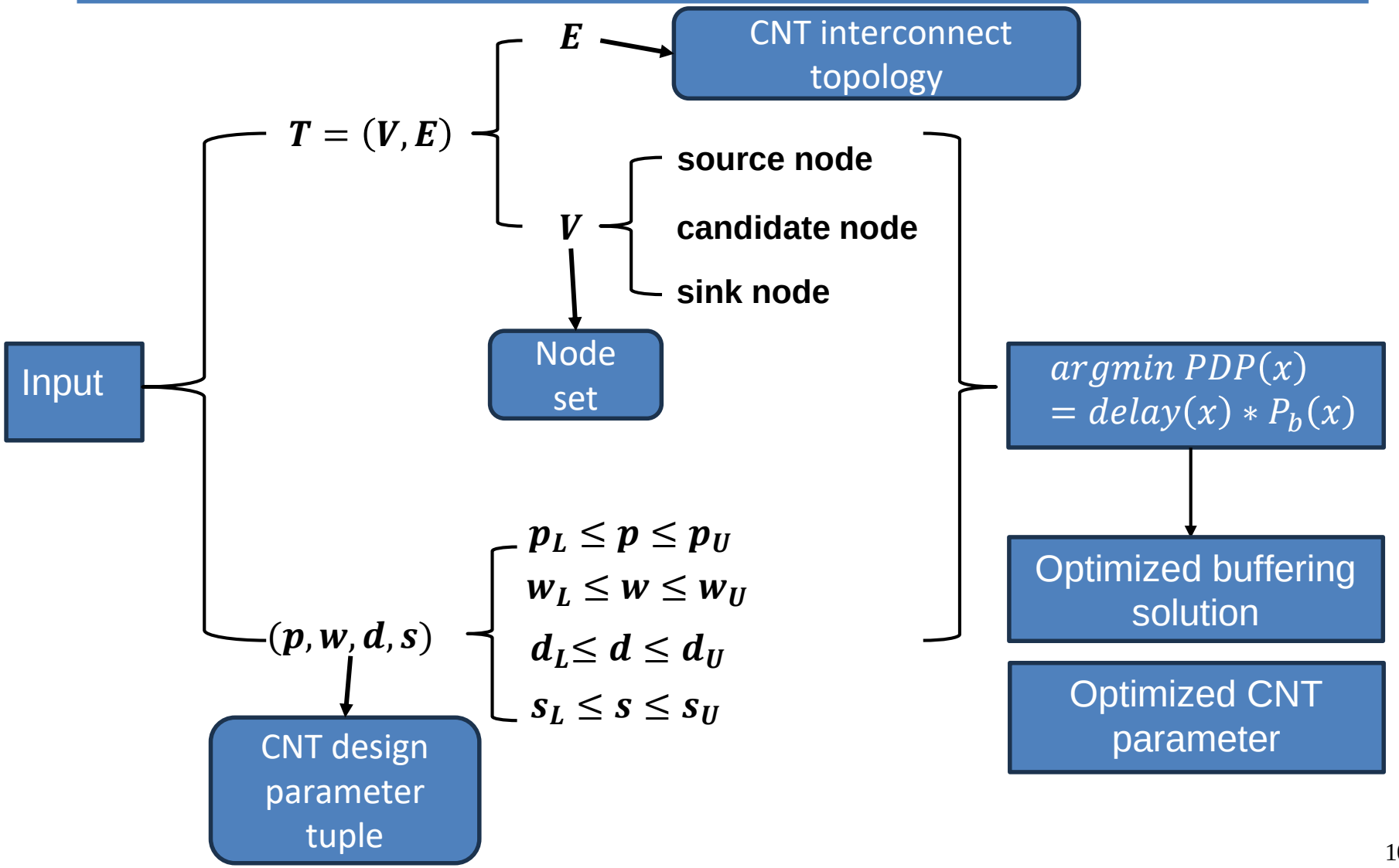
Problem Formulation



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The Proposed Framework (1/7)

Overview

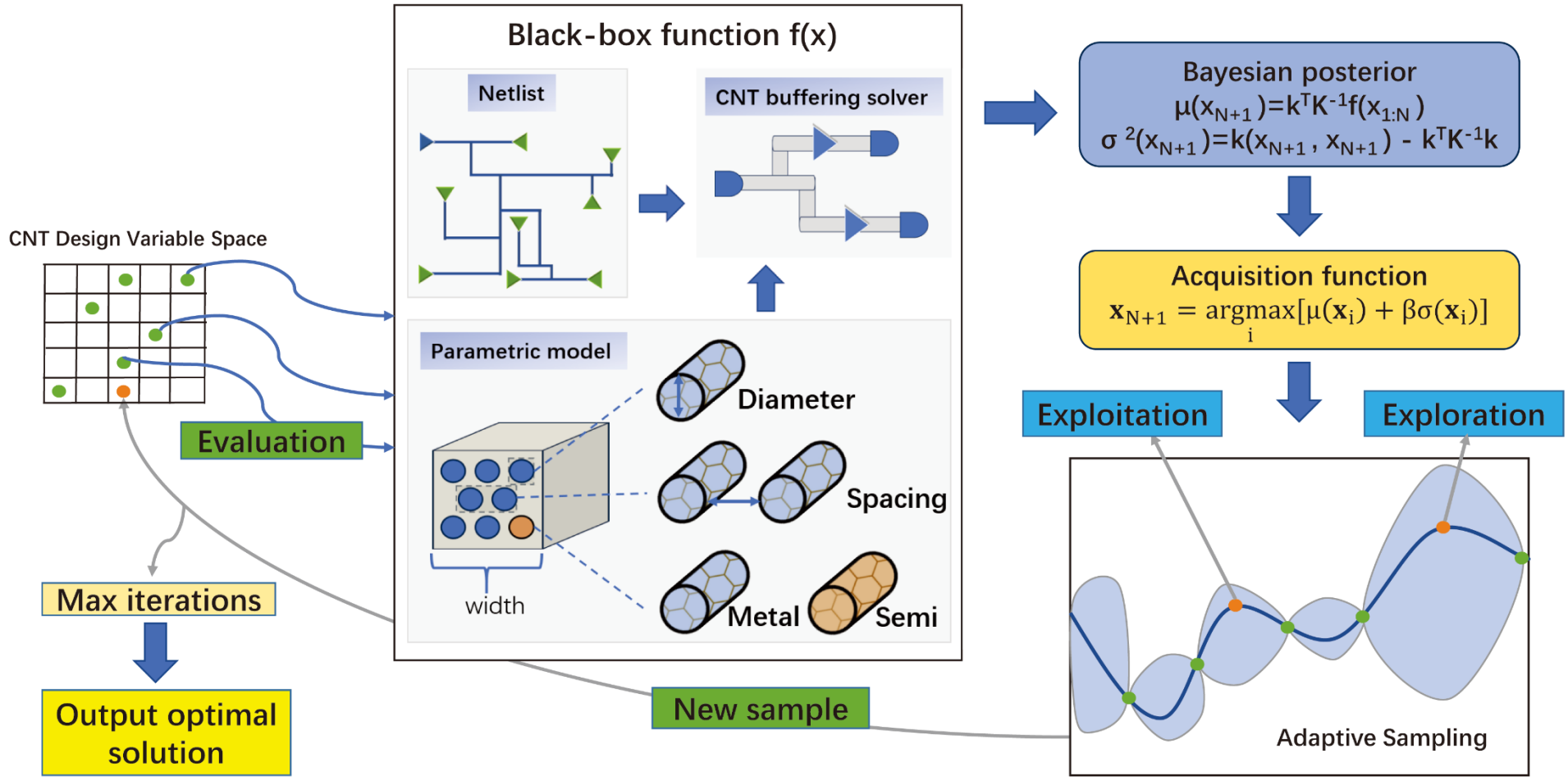


Fig. 5. The Proposed Framework

The Proposed Framework (2/7)
CNT Interconnect Model

CNT space = CNT diameter
wire-to-substrate distance 1μm

Res

$$R = R_Q + R_S \cdot L + R_C = \frac{h}{4c^2}\left(1 + \frac{L}{\lambda_{CNT}}\right) + R_C$$

$$\lambda_{CNT} = 1000d$$

$$N_{CNT} = p \cdot \left(N_W N_H - Inter\left[\frac{N_H}{2}\right]\right)$$

$$N_W = Inter[\frac{w-d}{d+s}]$$

$$N_H = Inter\left[\frac{H-d}{\left(\frac{\sqrt{3}}{2}\right)(d+s)}\right] + 1$$

$$R_b = \frac{R}{N_{CNT}}$$

The Proposed Framework (3/7)
CNT Interconnect Model

CNT space = CNT diameter
wire-to-substrate distance 1μm

Cap

$$C_b = 2C_{En} + \frac{N_W - 2}{2} C_{Ef} + \frac{3(N_H - 2)}{5} C_{En}$$

$$C_{En} = \frac{2\pi\epsilon}{\ln(\frac{w}{d})}$$

$$C_{Ef} = \frac{2\pi\epsilon}{\ln(\frac{2w}{d})}$$

The Proposed Framework (4/7)
CNT Interconnect Model

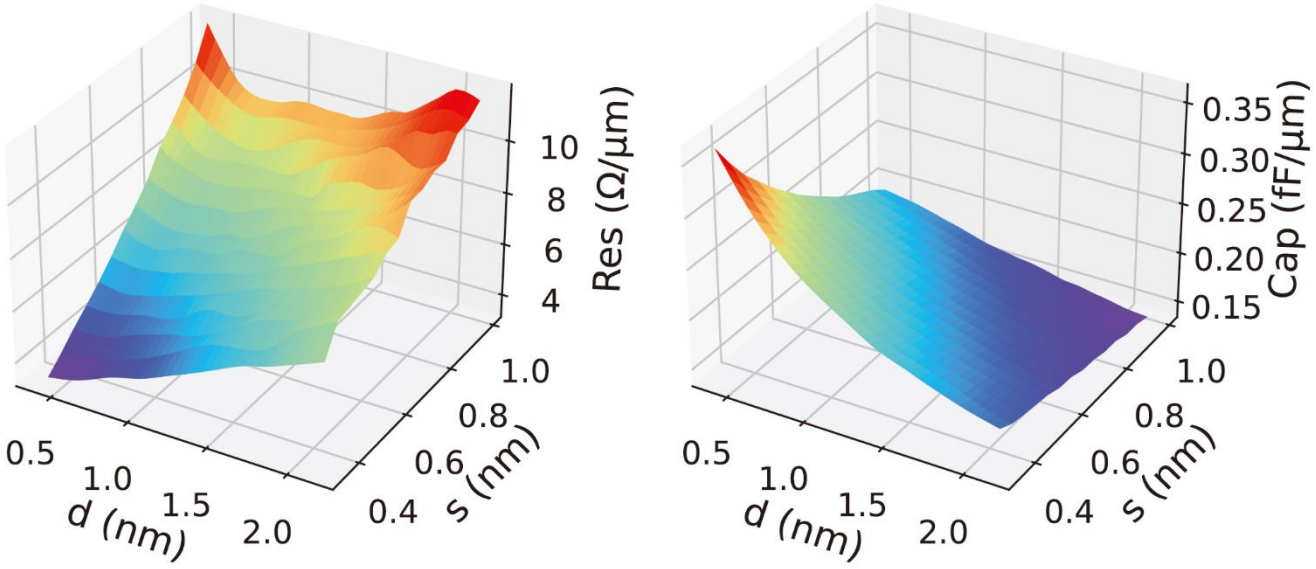
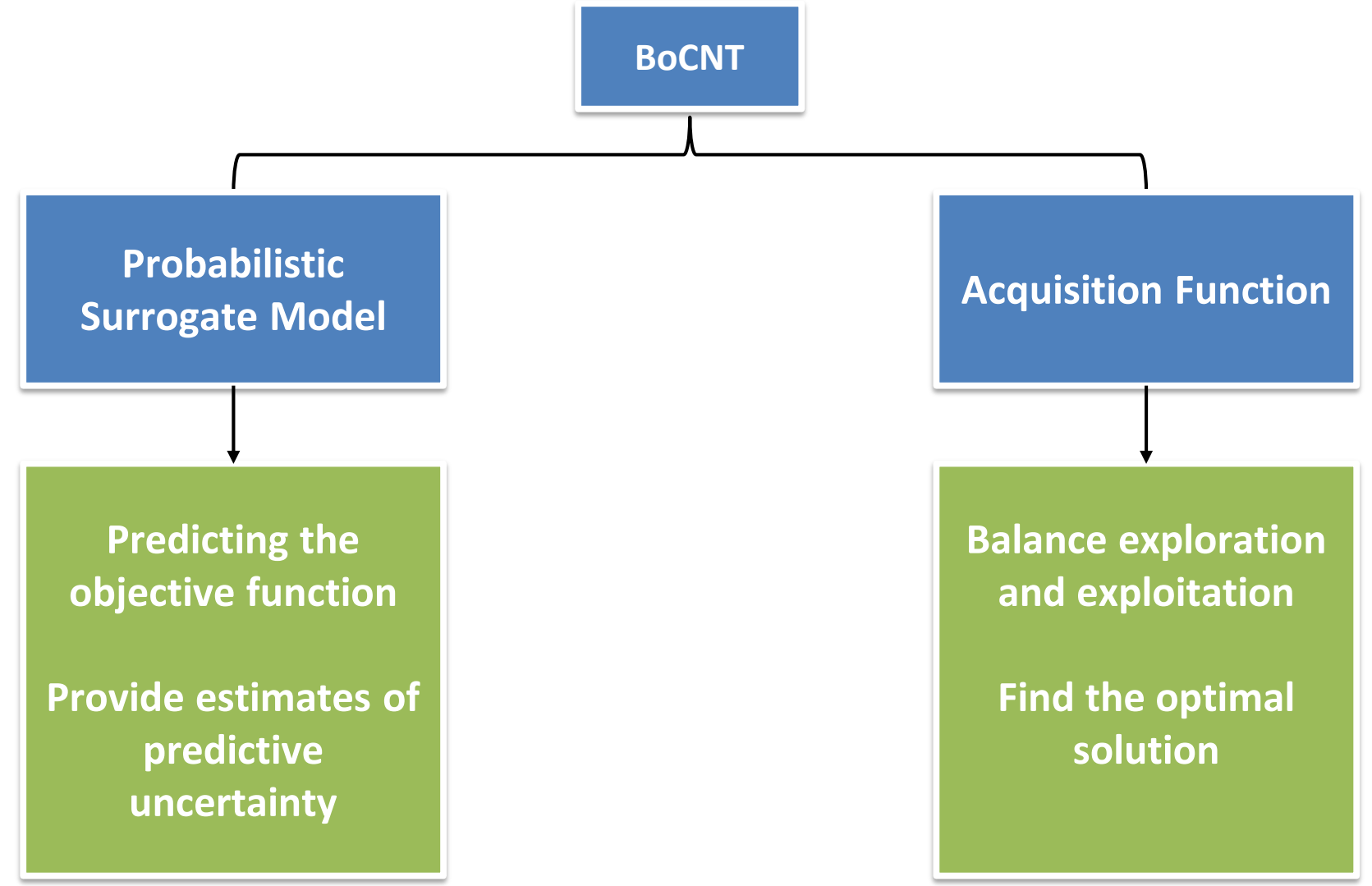


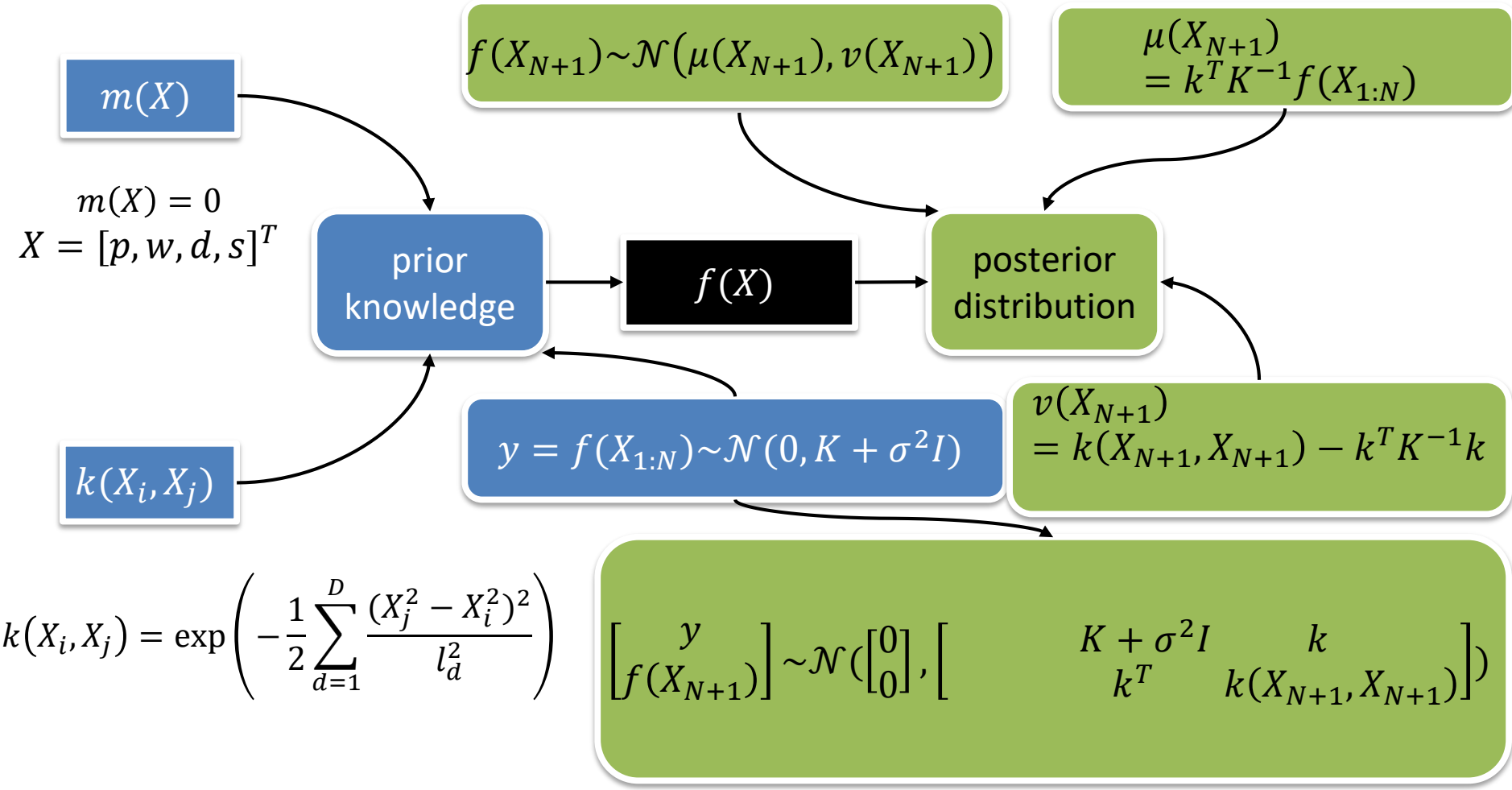
Fig. 6. Resistance and capacitance of bundled SWCNT with different design parameters.

The Proposed Framework (5/7)
Bayesian Co-optimization



The Proposed Framework (6/7)
Probabilistic Surrogate Model

Gaussian Process (GP)



The Proposed Framework (7/7)
Acquisition Function

Upper confidence bound

$$X_{N+1} = \underset{X}{argmax}\left(\mu(X) + \beta v(X)\right)$$

$$\beta = (2\ln\left(\frac{2\pi N^2}{10\eta}\right))^{\frac{1}{2}},$$

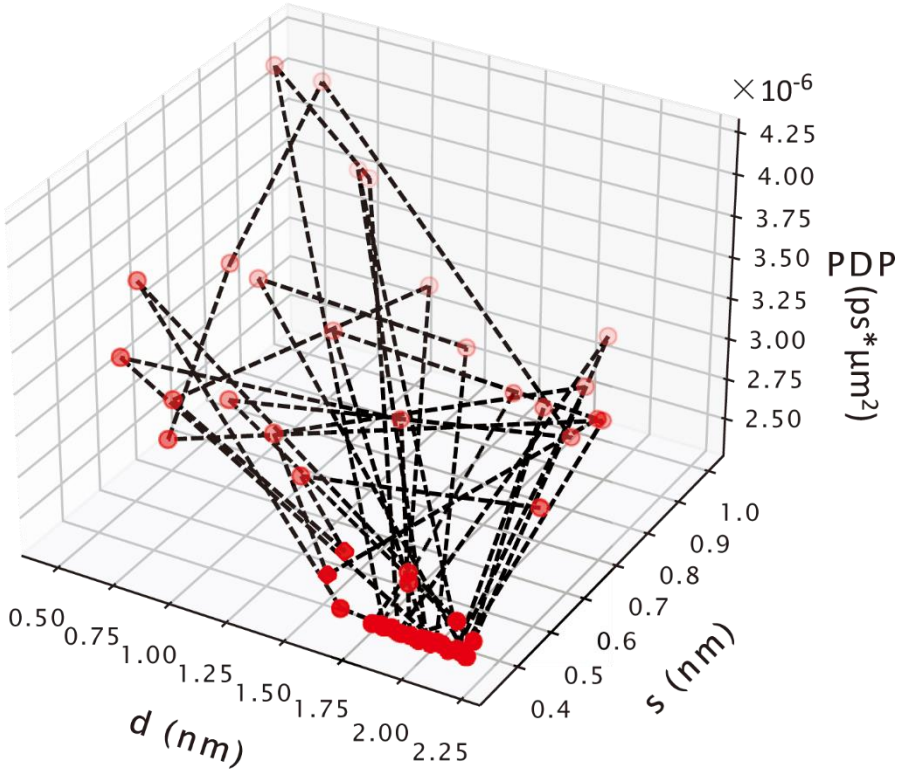


Fig. 7. The design space search trajectory of the proposed BoCNT technique.

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Experimental Results (1/5)
Setup

- Programming with C/C++ language
- BoCNT framework is built with the BoTorch package
- A computer with a 3.7GHz AMD Ryzen CPU and 32GB memory
- Benchmark
  - Five types of buffers and five types of inverters from are used for buffer insertion.[L. Liu and S. Hu, “Buffering single-walled carbon nanotubes bundle interconnects for timing optimization,” ISVLSI, pp.362-367, 2014.]
  - The parameters of copper interconnects. [ITRS 2013]

Experimental Results (2/5)

Comparisons with Fixed CNT Design Parameters

	Fixed CNT buffering[1]	BoCNT technique
Parameters		
Probability of m-CNT		33%~100%
SWCNT bundle width		28nm~84nm
CNT diameter	1nm	0.4nm~2.2nm
Adjacent CNT spacing	0.66nm	0.34nm~1.02nm

TABLE Ⅰ CNT DESIGN PARAMETERS RANGE AT 22NM TECHNOLOGY NODE

[1] L. Liu and S. Hu, “Buffering single-walled carbon nanotubes bundle interconnects for timing optimization,” ISVLSI, pp.362-367, 2014.

Experimental Results (3/5)

Comparisons with Fixed CNT Design Parameters

Test cases		p1	p2	r1	r2	r3	r4	Avg.
Number of sink nodes		269	603	267	598	862	1903	750
Number of connections		537	1205	533	1195	1723	3805	1500
Fixed CNT buffering[4]	Delay(ps)	94.5	172.4	953.5	1338.8	1532.2	2181.8	1045.5
	Buffer Area(μm^2)	32.3	77.2	231.4	476.2	647.9	1345.3	468
	PDP($ps * \mu m^2$)	3052	13309	220640	637536	992712	2935175	800404
The proposed BoCNT technique	Delay(ps)	86.5	157.3	837.2	1167	1351.9	1925.4	920.9
	Buffer Area(μm^2)	30.3	69.1	219.1	448.2	601.3	1245.2	435.5
	PDP($ps * \mu m^2$)	2623	10873	183438	526429	813113	2415970	658741
Delay Improvement(%)		8.5	8.7	12.2	12.8	11.8	11.7	11.0
BufArea Improvement(%)		6.2	10.5	5.3	5.9	7.2	7.4	7.1
PDP Improvement(%)		14.1	18.3	16.7	17.4	18.1	17.7	17.0

TABLE Ⅱ OPTIMIZATION RESULTS OF DIFFERENT NETS AT 22NM TECHNOLOGY NODE

Result

- Our proposed BoCNT framework can achieve PDP improvement by **17%** on average
- With the optimized design parameters, the interconnect delay and buffer area can be improved by **11%** and **7.1%** on average respectively

Experimental Results (4/5)
Comparisons with Cu Interconnects

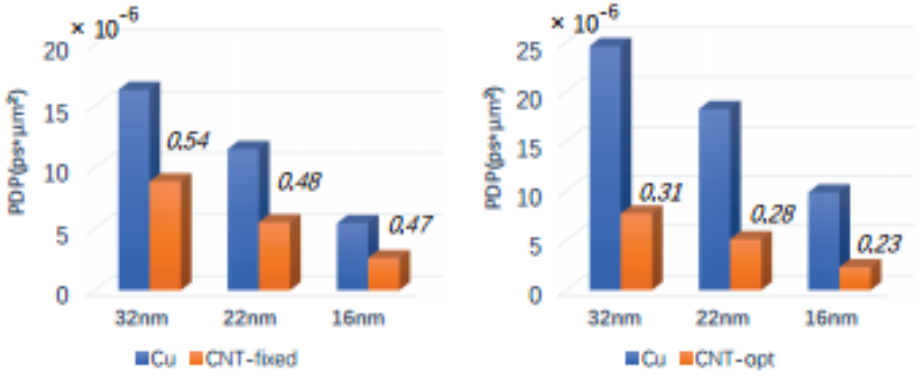

Fig. 8. PDP comparison between CNT and copper

Result

- CNT with fixed geometric parameters, the delay and PDP ratio is **38%** and **49.7%** on average.
- While with BoCNT optimizations, these values are **24.7%** and **27.3%**.
- Reduce delay and PDP by **35%** and **45%** on average.

Test cases		p	w(nm)	d(nm)	s(nm)	Delay(CNT/Cu)	Radio
CNT opt	32nm	0.73	76	0.4	0.34	(3550,11833)	0.3
	22nm	0.86	58	0.4	0.34	(2443,9396)	0.26
	16nm	0.94	32	0.4	0.34	(1179,6552)	0.18
CNT fixed	32nm	1	84	1	0.66	(3883,8263)	0.47
	22nm	1	67	1	0.66	(2621,6720)	0.39
	16nm	1	42	1	0.66	(1382,4935)	0.28

TABLE Ⅲ DELAY COMPARISONS OF OPTIMIZED CNT AND FIXED-PARAMETER CNT OVER COPPER AT DIFFERENT TECHNOLOGY NODES

Experimental Results (5/5)
Summary

- Proposed a Beyasian optimization framework to co-optimize the bundled SWCNT geometric parameters and buffer insertion synergistically.
- Compared to the state-of-the-art work, our proposed BoCNT technique can reduce PDP by **17%.**
- Compared to SOTA method, BoCNT can further delay and PDP of SWCNT interconnect by **35%** and **45%.**

Thank You !
Q&A

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