# TransPlace: A Scalable Transistor-Level Placer for VLSI Beyond Standard-Cell-Based Design

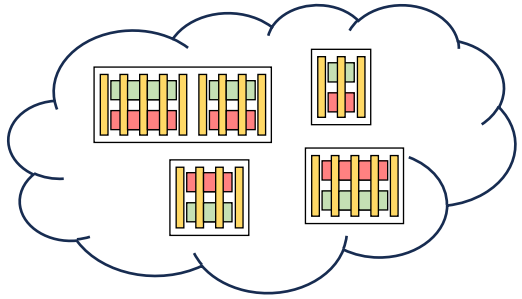
**Chen-Hao Hsu**[1], Xiaoqing Xu[2], Hao Chen[2], Dino Ruic[2], David Z. Pan[1]

[1] ECE Department, UT Austin
[2] X, the moonshot factory


# Introduction | Standard-Cell-Based Design Flow

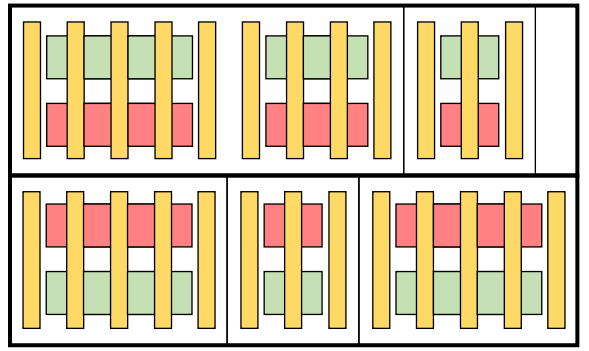
- Standard cell (SDC) library
  - A collection of low-level logic cells
  - Specific to a technology node
  - Fixed physical implementation
- Optimization of overall wirelength and area is limited

RTL design



Standard cell library

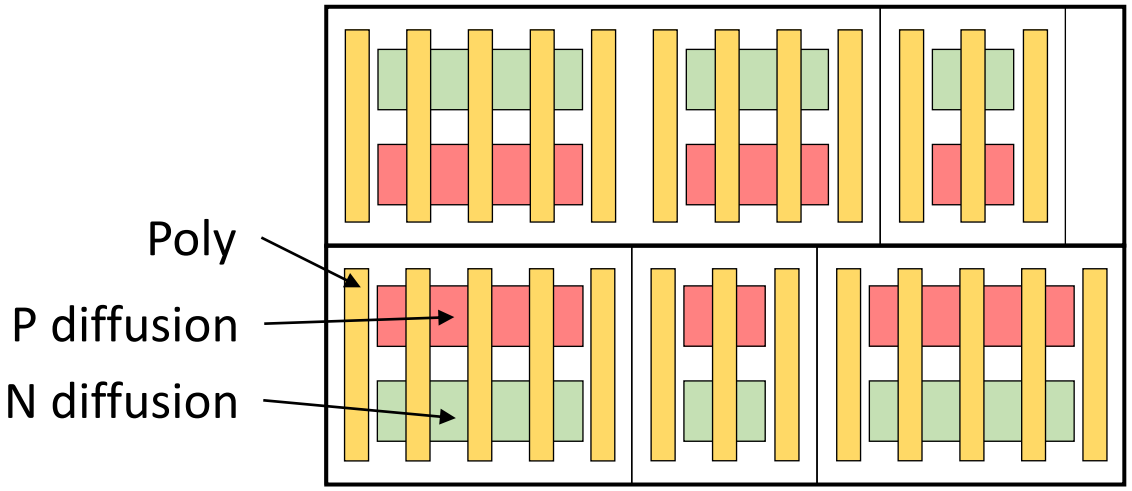
**Can we directly place transistors?**



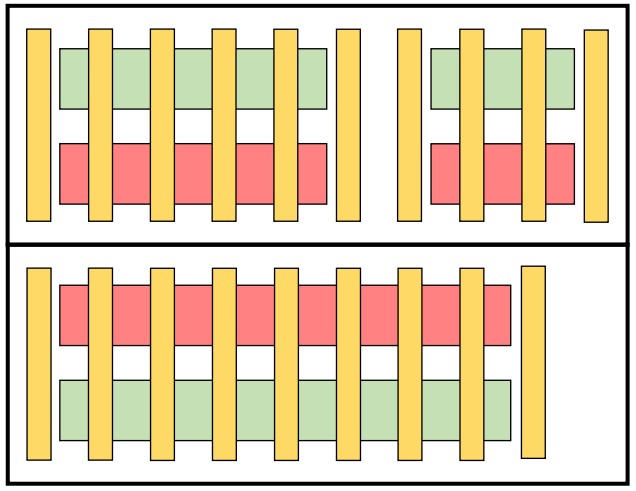
Standard-cell-based design

# Motivation for Transistor-Level Design

- Break the “abstraction” of standard cells
- Directly place transistors instead of standard cells
  - Offer greater flexibility, explore more diffusion sharing
  - Achieve potentially better PPA



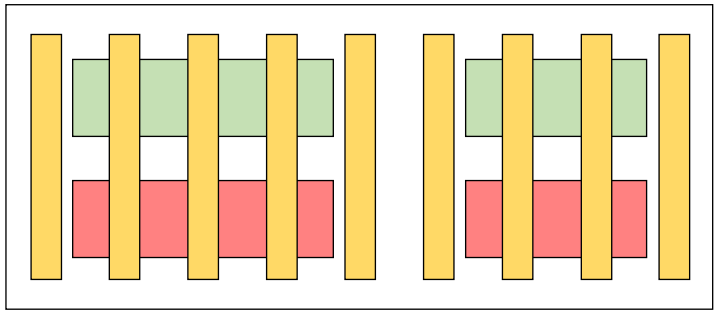

**Standard-cell-based design**
2 (rows) x **13** (poly pitch)



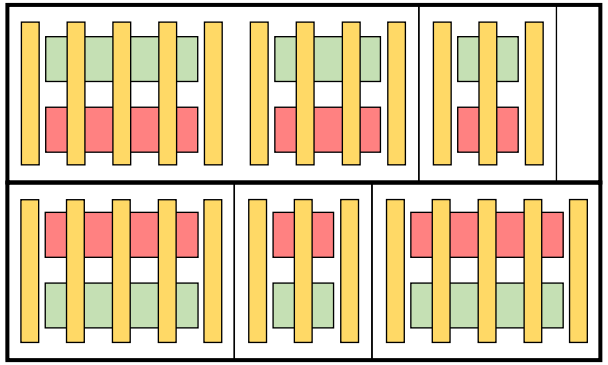
**Transistor-level design**
2 (rows) x **10** (poly pitch)

# Transistor-Level Placement Challenges

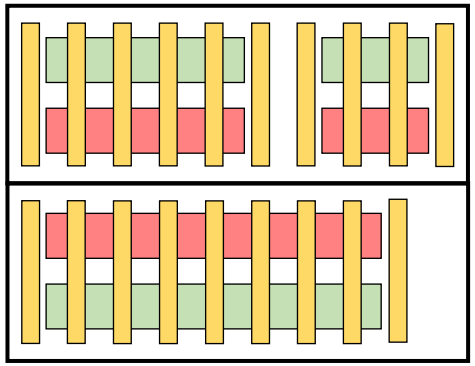
- Previous work
  - SAT-based [Cardoso, *et al.*, ISCAS'20], SMT-based [Lee *et al.*, TCAD'20]
  - Transistor placement within a standard cell (<50T)
  - Not scalable, long runtime
- Challenges
  - Scalability: how to handle hundreds of transistors or more
  - Diffusion sharing



Standard cell



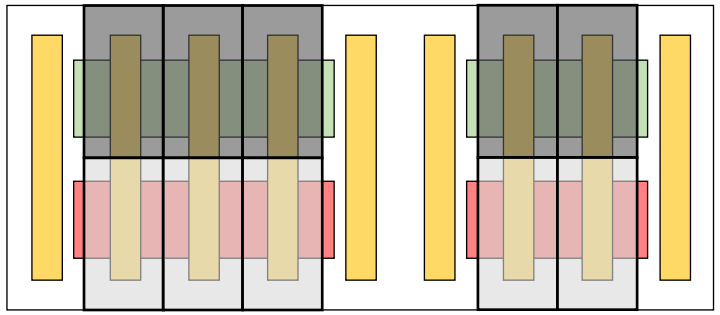
Standard-cell-based design



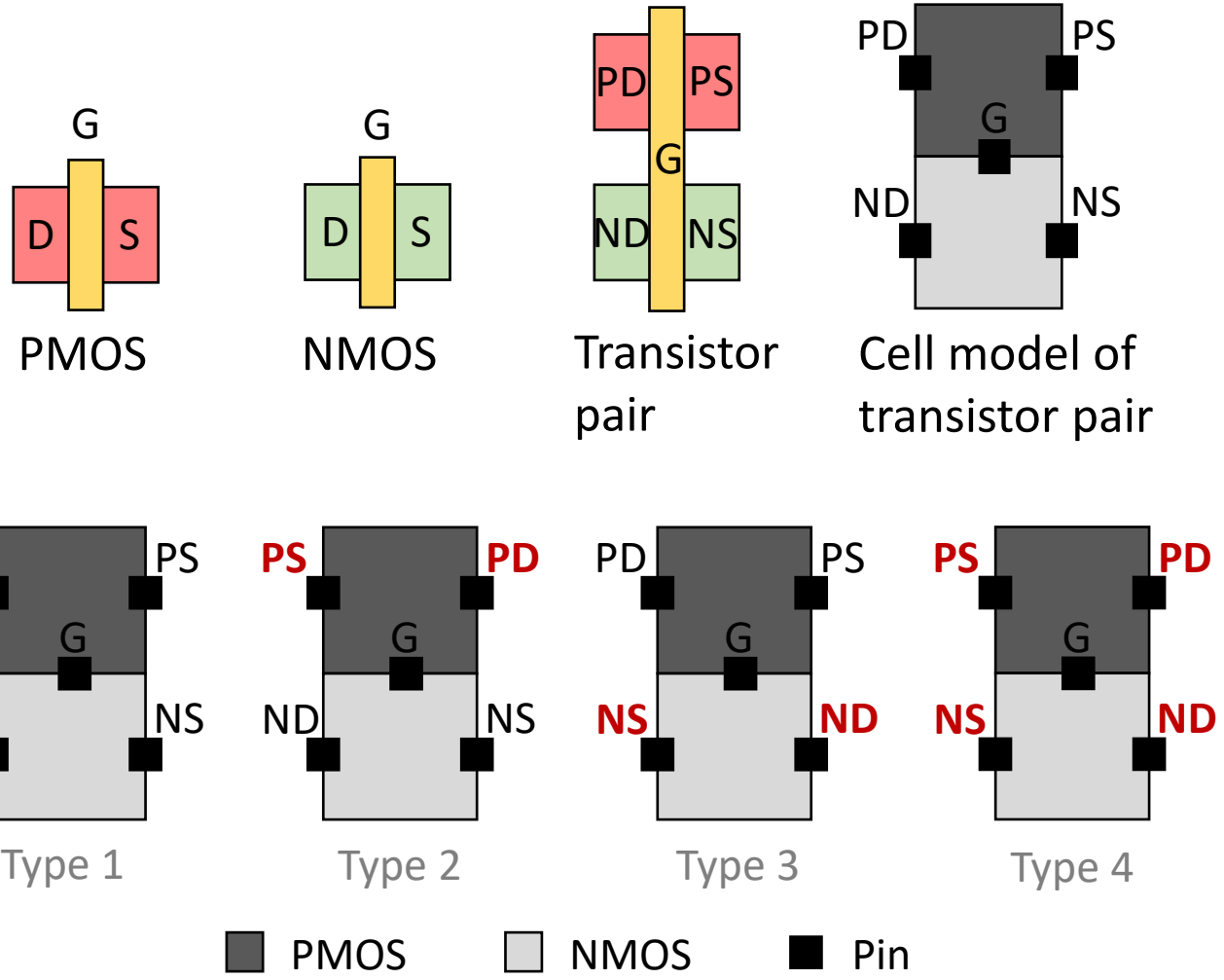
Transistor-level design

# Transistor Modeling

- Transistor pair
  - One PMOS, one NMOS
  - Share the same gate nets
  - Avoid poly misaligned transistors for routability

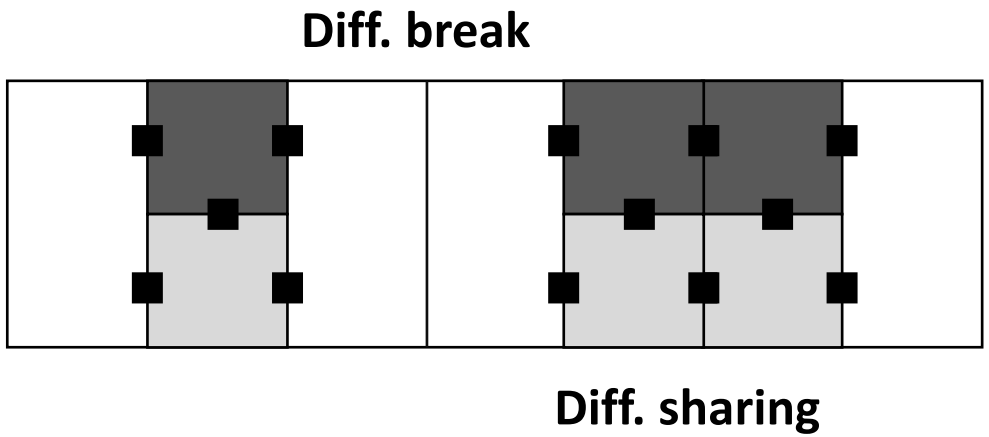


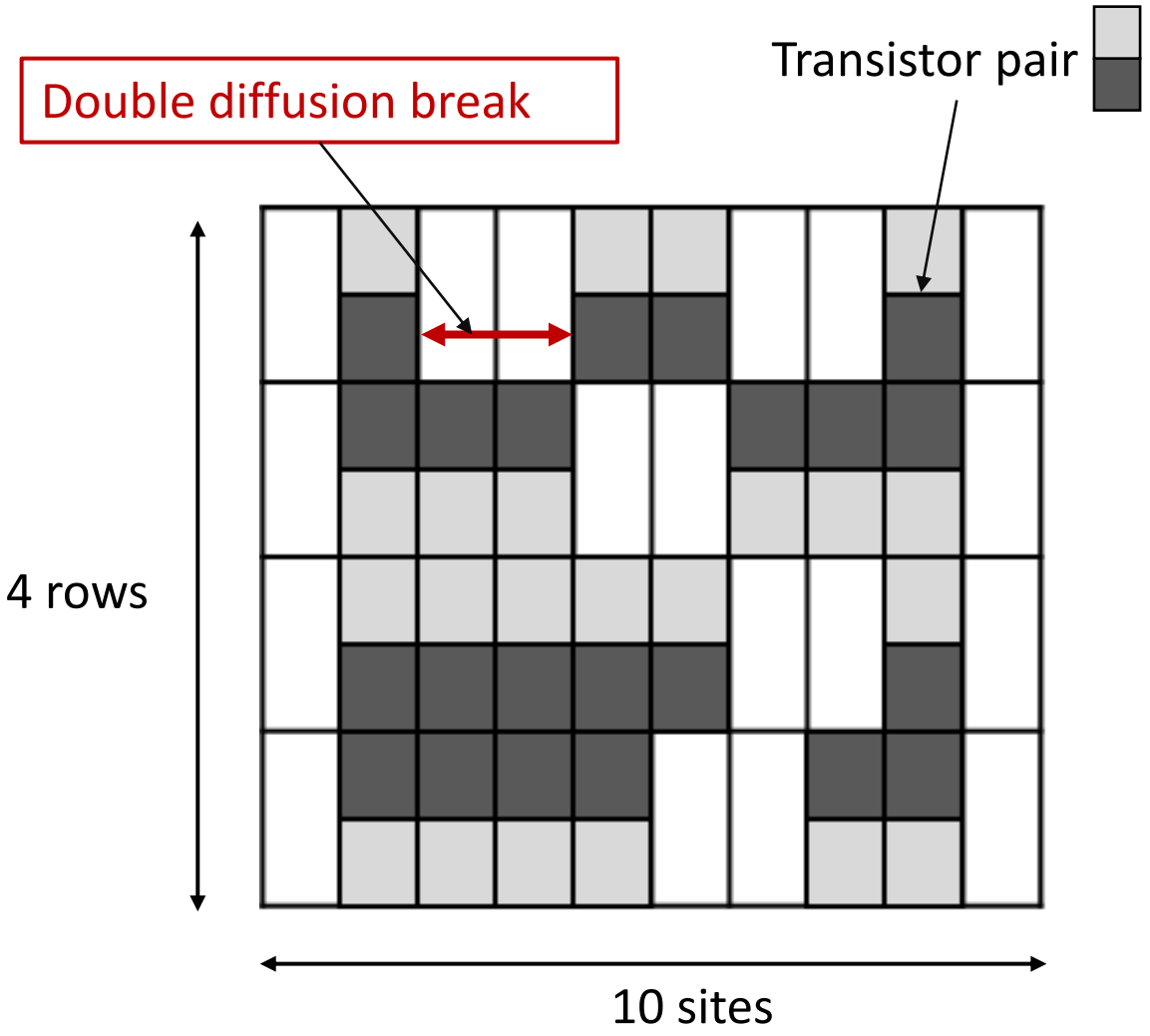
- Four flip types
  - Flip PMOS/NMOS or not



# Design Canvas & Diffusion Sharing/Break

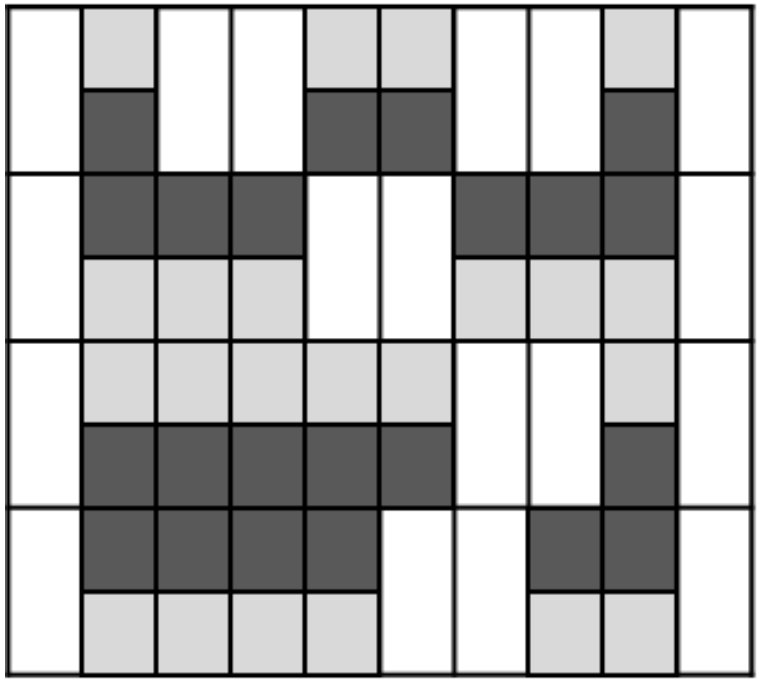
- Design canvas
  - Rows × Sites
- Diffusion sharing
  - No space needed
- Diffusion break
  - Space needed
  - ASAP7: double diffusion break



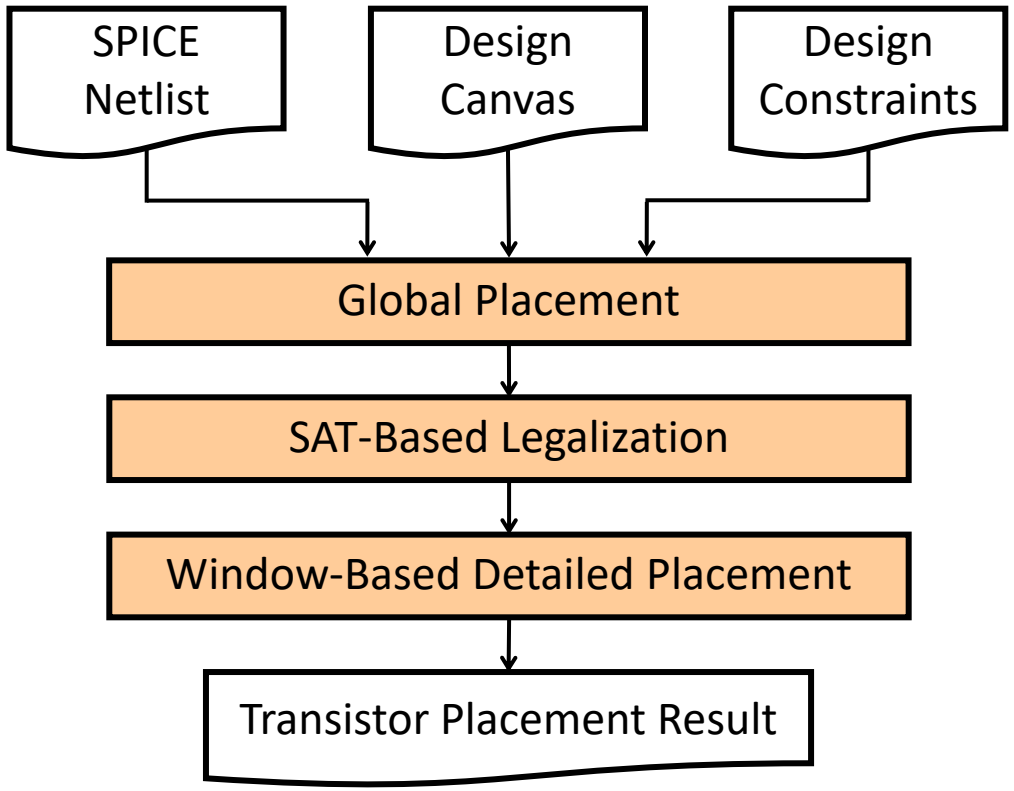
# Problem Formulation | Transistor Placement

- Given
  - Transistor-level netlist (SPICE)
  - Design canvas
  - Design constraints
- Output
  - Transistor placement result within the given design canvas
- Objective
  - Minimize total wirelength (HPWL)
  - (Minimize design area)
- Constraint
  - Legal diffusion sharing/break



Transistor placement

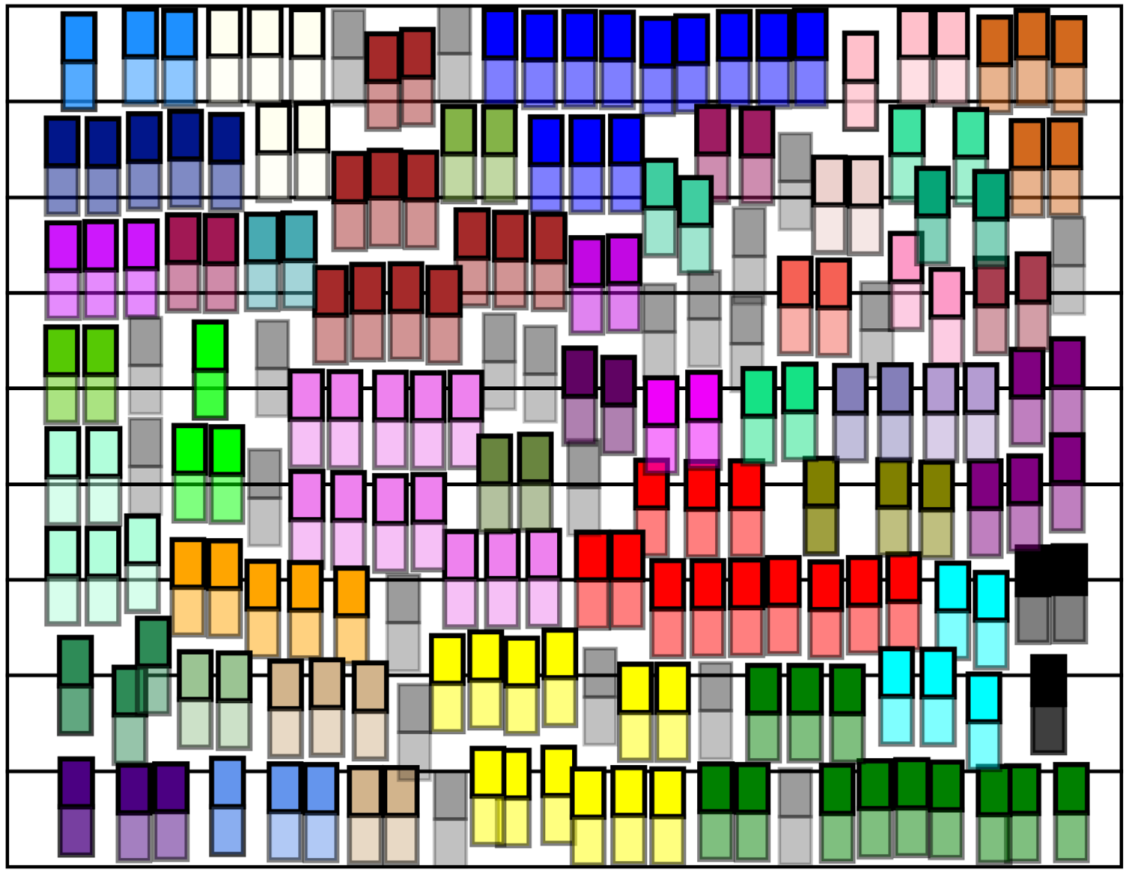
# TransPlace Flow




- Global placement (GP)
  - Generate a rough placement solution
  - Maintain a global view of the whole netlist
- SAT-based legalization (LG)
  - Remove transistor overlapping
  - Place each transistor to sites
  - **Ensure legal diffusion sharing/break**
- Window-based detailed placement (DP)
  - Refine placement solution **locally**
  - Improve total wirelength

# Global Placement (GP)

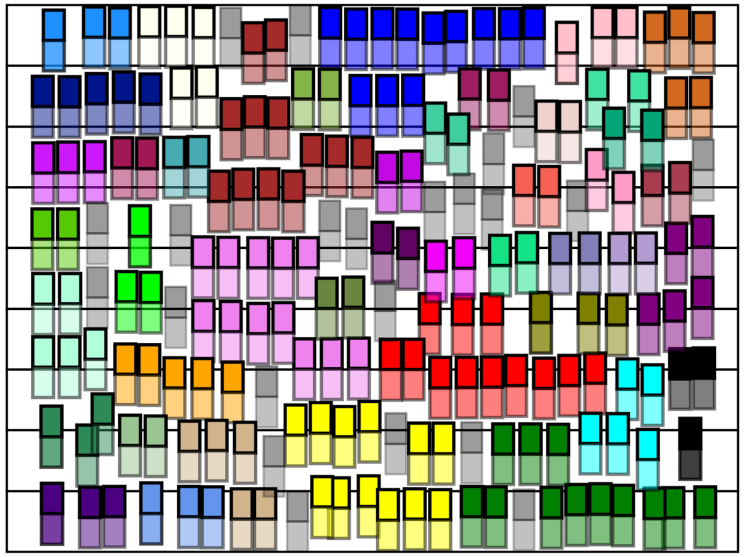
- Adopt DREAMPlace
  - Analytical GPU-accelerated placer
  - Very fast and high quality
  - Set low target bin density (e.g., 0.5) for even cell distributions on canvas
- Transistors belonging to the same original standard cell are **colored the same**
  - DREAMPlace naturally clusters them together
  - But they are not in the same row like in standard cells



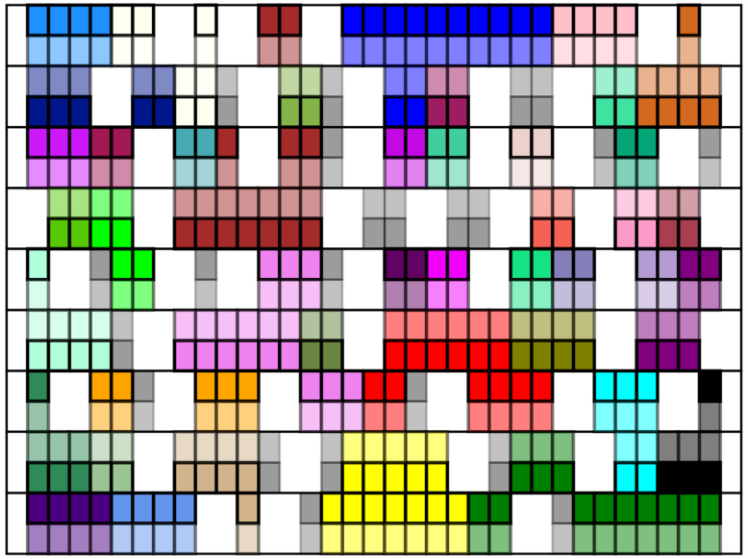
Mul4 (418T)

# SAT-Based Legalization (LG)

- Key idea
  - Candidate locations of a transistor pair: **locations near its GP location**
- Set up SAT formulation for **entire design**
- Variables (for each transistor pair)
  - Location variables: candidate locations
  - Flip type variables: four types
- Constraints
  - Cell constraint: location & flip type
  - Location constraint
  - Diffusion sharing constraint
  - Double diffusion break constraint



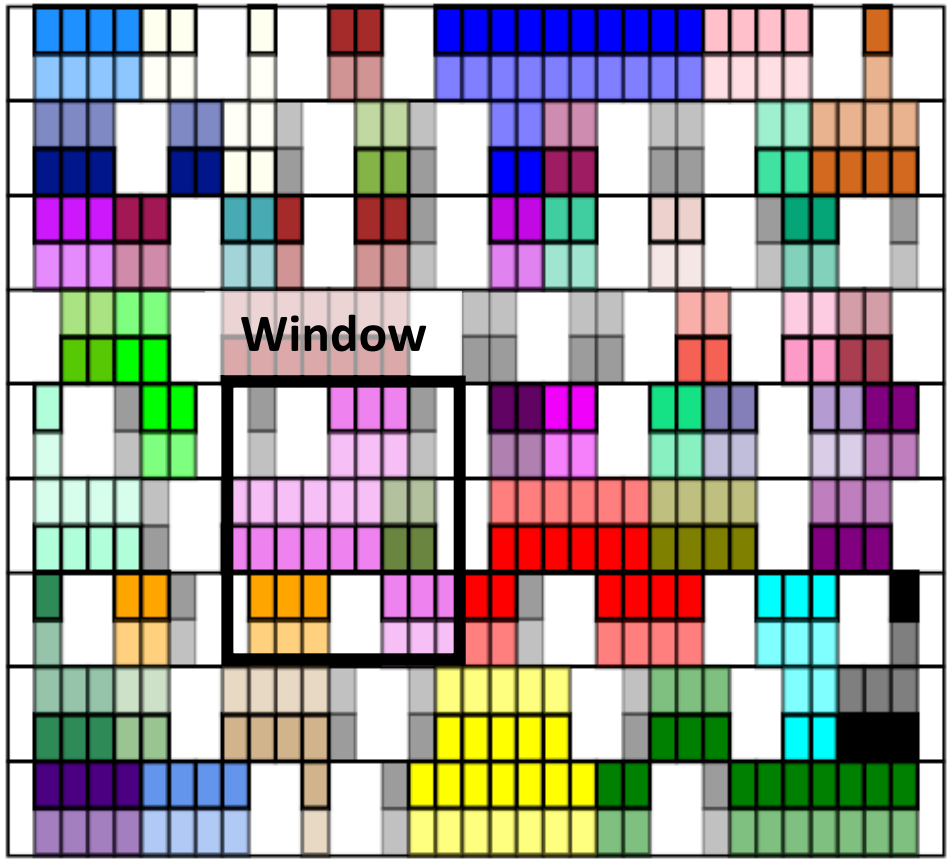
GP result



LG result

# Window-Based Detailed Placement (DP)

- Enumerate solutions within a window
  - Set up SAT formulation for a window
  - Only re-place transistor pairs in the window
  - Use **incremental SAT solving**
- **Iteratively** optimize total HPWL
  - Accept solutions with less HPWL
- Fast and effective



# Benchmarks

- Created benchmarks by flattening standard cell (SDC) based designs
  - ASAP7 PDK
- Largest design: *adder16* with **448** transistors and **257** nets

| Benchmark | #SDC | SDC Area | #PMOS | #NMOS | #Transistors | #Intra-cell Nets | #Inter-cell Nets | #Nets |
|---|---|---|---|---|---|---|---|---|
| mul2 | 10 | **47** | 25 | 25 | **50** | 13 | 14 | **27** |
| adder4 | 13 | **95** | 55 | 55 | **110** | 39 | 21 | **60** |
| adder8 | 24 | **160** | 112 | 112 | **224** | 82 | 47 | **129** |
| adder12 | 36 | **240** | 168 | 168 | **336** | 122 | 71 | **193** |
| mul4 | 65 | **355** | 209 | 209 | **418** | 130 | 79 | **209** |
| adder16 | 48 | **320** | 224 | 224 | **448** | 162 | 95 | **257** |

# Standard-Cell-Based Design vs. Transistor-Level Design

- Design Area: **18%** reduction
- Total HPWL: **5%** reduction

| | Standard-Cell-Based Design | | | | | Transistor-Level Design | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Benchmark | Intra. WL | Inter. WL | Total WL | #Sharing | Area | Intra. WL | Inter. WL | Total WL | #Sharing | Area | Time (sec) |
| mul2 | 20.5 | 101.0 | **121.5** | 14 | **54** | 28.0 | 87.5 | **115.5** | 18 | **39** | 7 |
| adder4 | 86.5 | 225.5 | **312.0** | 35 | **108** | 107.0 | 200.5 | **307.5** | 41 | **84** | 646 |
| adder8 | 106.0 | 440.5 | **546.5** | 88 | **186** | 88.0 | 410.0 | **498.0** | 96 | **150** | 76 |
| adder12 | 154.0 | 653.0 | **807.0** | 132 | **259** | 134.0 | 670.0 | **804.0** | 144 | **224** | 428 |
| mul4 | 194.0 | 1082.5 | **1276.5** | 136 | **387** | 218.0 | 940.0 | **1158.0** | 161 | **315** | 54 |
| adder16 | 202.0 | 888.5 | **1090.5** | 176 | **344** | 170.0 | 862.0 | **1032.0** | 188 | **312** | 209 |
| **Avg. Ratio** | 1 | 1 | 1 | 1 | 1 | **1.04** | **0.93** | **0.95** | **1.15** | **0.82** | |

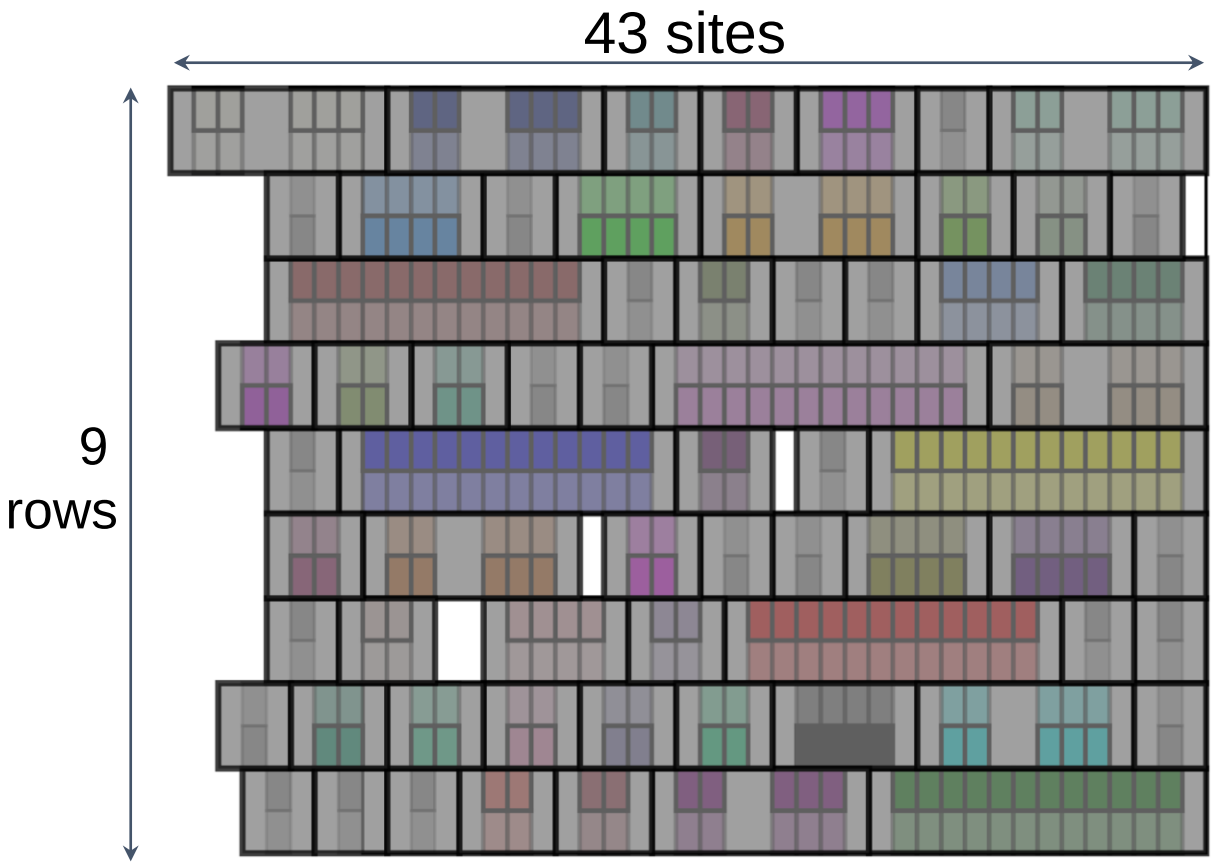
# Area Reduction from Standard Cell Area

- **9%** area reduction from standard cell area (not design area)

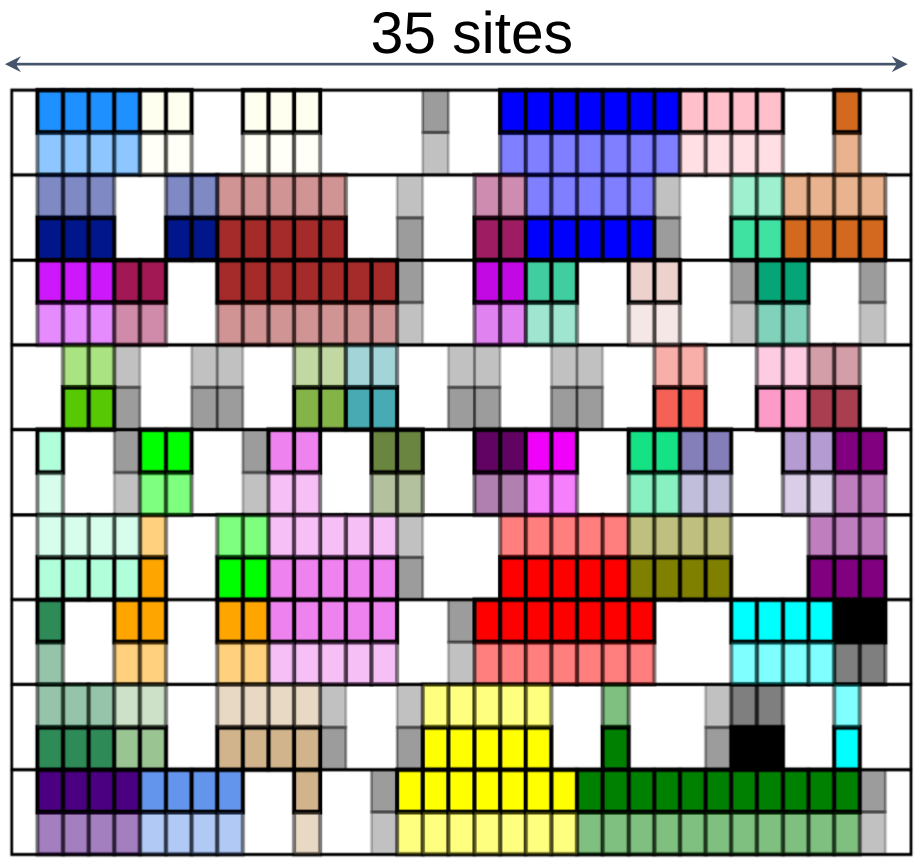
| Benchmark | Standard-cell-based Design Area | Standard Cell Area | Transistor-level Design Area |
|---|---|---|---|
| mul2 | 54 | 47 | **39** |
| adder4 | 108 | 95 | **84** |
| adder8 | 186 | 160 | **150** |
| adder12 | 259 | 240 | **224** |
| mul4 | 387 | 355 | **315** |
| adder16 | 344 | 320 | **312** |
| **Avg. Ratio** | 1.12 | 1 | **0.91** |

# Layout Visualization | Mul4

Standard-cell-based design
**Area 9 x 43**

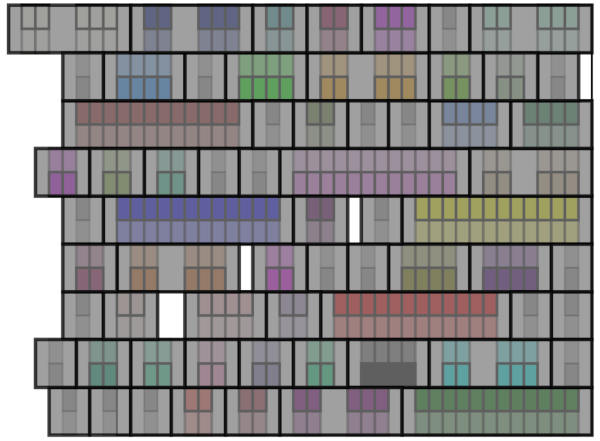



Transistor-level design
**Area 9 x 35**

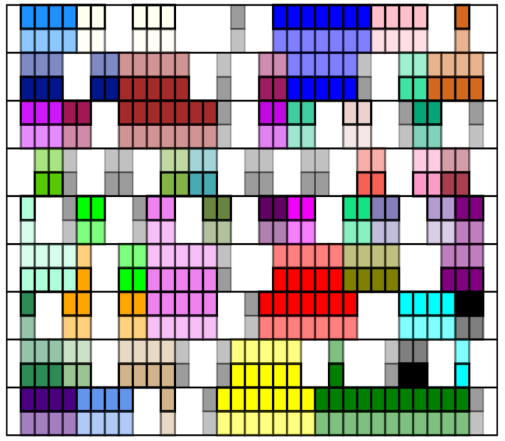


# Conclusion

- We have presented TransPlace
  - Propose a novel framework: GP, LG, DP
  - Optimize overall wirelength and area
  - Consider diffusion sharing between different SDCs
- Transistor-level designs can achieve significantly **less total wirelength and design area** than SDC-based designs
- TransPlace is the first attempt to “break” the SDC abstraction in large macros
  - More design-technology co-optimization (DTCO) shall be explored to unleash the full potential of DTCO



Standard-cell-based design



Transistor-level design

# THANK YOU!