MACRO: Multi-agent Reinforcement Learning-based Cross-layer Optimization of Operational Amplifier

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1 Background

- **Complicated circuit design flow**

Topology design → Transistor sizing → Placement & routing

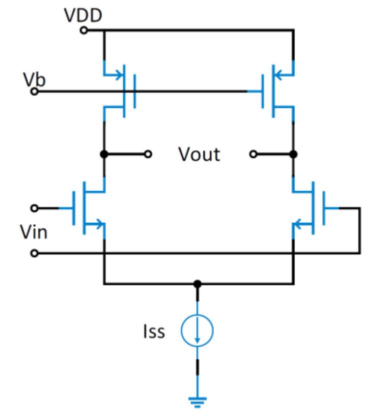
Tedious manual design

Automated opamp synthesis

- **Related works**

Small-scale sizing: BO [1] & RL [2] state-of-the-art

Topology synthesis: GA [3] / BO [4][5] / RL [6]

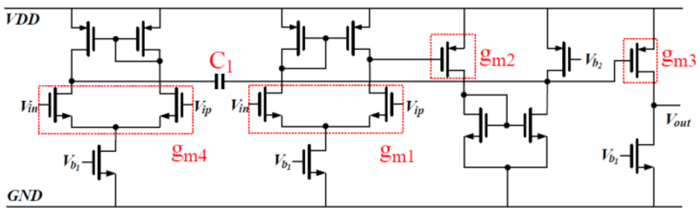


[1] W. Lyu, et al. "An efficient bayesian optimization approach for automated optimization of analog circuits", IEEE TCAD, 2017.
[2] H. Wang, et al. "Gcn-rl circuit designer: Transferable transistor sizing with graph neural networks and reinforcement learning", DAC 2022.
[3] C. Mattiussi, et al. "Analog genetic encoding for the evolution of circuits and networks", IEEE TEC, 2007.
[4] J. Lu, et al. "Automated compensation scheme design for operational amplifier via bayesian optimization", DAC 2021.
[5] J. Lu, et al. "Topology optimization of operational amplifier in continuous space via graph embedding." DATE 2022
[6] Z. Chen, et al. "TOTAL: Topology Optimization of Operational Amplifier via Reinforcement Learning", ISQED 2023.

2 Challenges

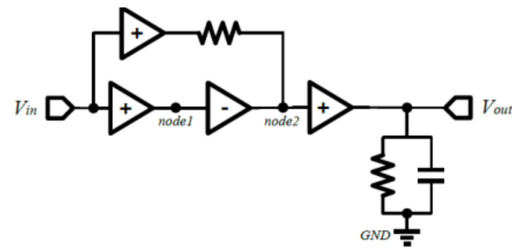
- **High dimensionality**

$\sim 25^{10}$ candidates [5]

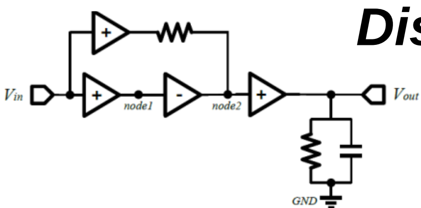


Simplify to

Behavior-level



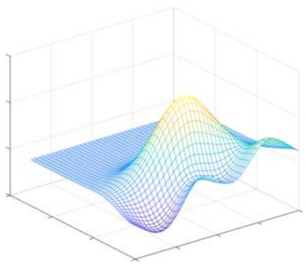
- **Heterogeneity**



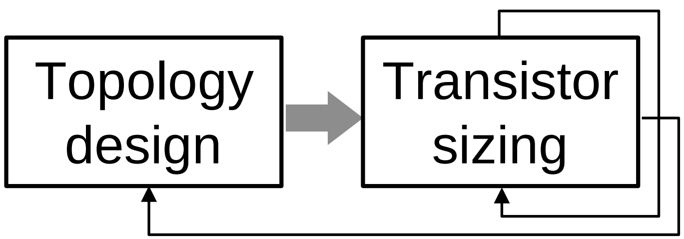
Discreteness of topological space

v.s.

Continuity of parametric space



- **Co-evolution**

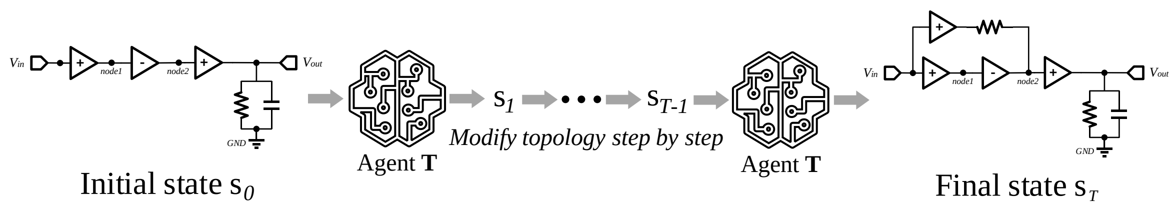


Inner loop: parameter iteration [5][6]

Outer loop: topology iteration [5][6]

3 Core Idea of MACRO

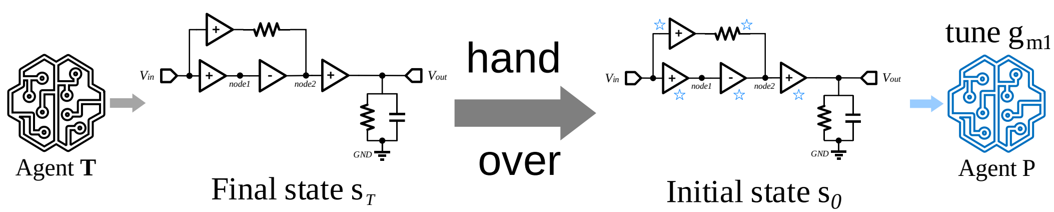
- **Decomposed Multi-step process**



Vast design space

Finite actions each step

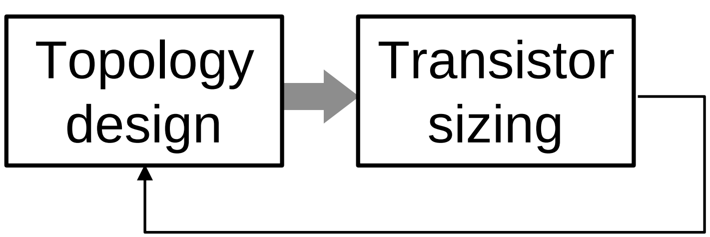
- **Multi-agent-based task allocation**



Customize agents T & P

when performing TD and PT

- **Gradient-based agent co-evolution**



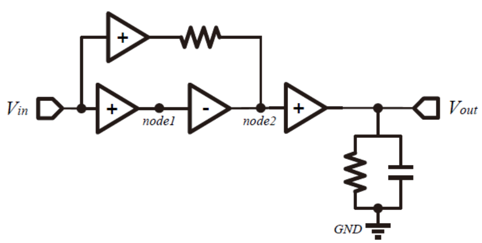
Inner loop canceled

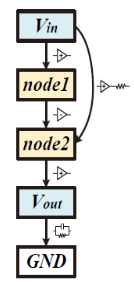
Outer loop generates the feedback

4 Topology Design Task

- **State & action design**

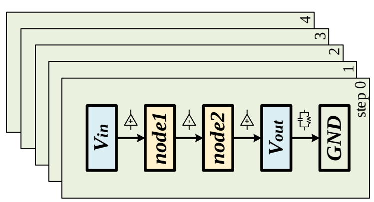
Nodes: VIN, VOUT, GND, NODE1, NODE2
Edges: Sample from 25 options below [5]





An opamp example DAG

Connection types	Directions	Total number
R/C	+	2
g_m (> 0 or < 0)	+/-	4
R&C in parallel/serial	+	2
g_m, R/C in parallel/serial	+/-	8
g_m, R&C in parallel/serial	+/-	8
disconnection	null	1



Gain $> c_{th}^{0}$
PM $> c_{th}^{1}$
GBW $> c_{th}^{2}$
1/Power $> c_{th}^{3}$

Topological state + Spec state

Design state

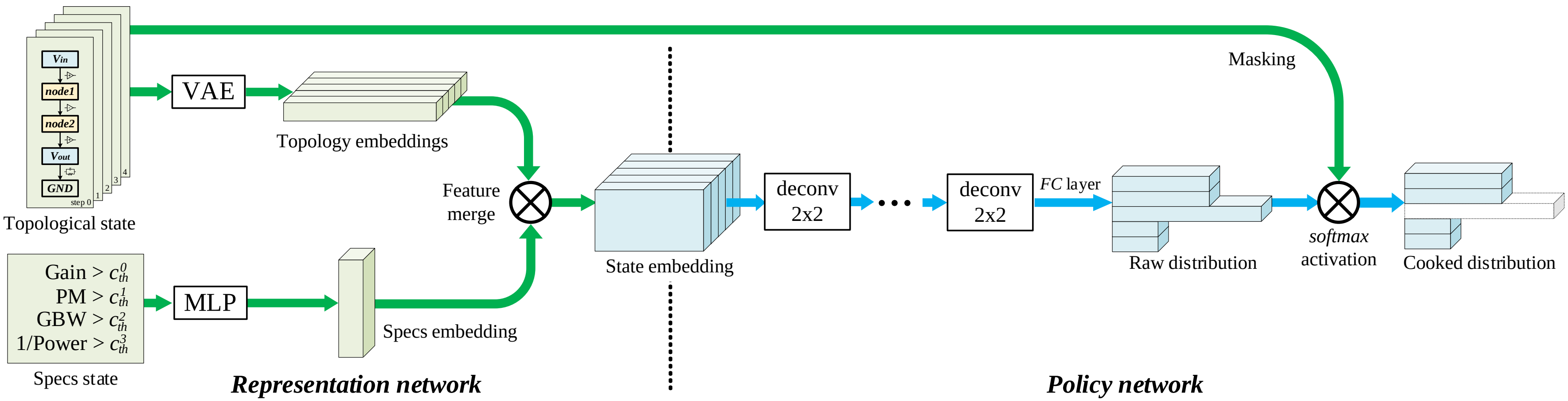
Fix three-stage cascode skeleton

Remain 5 edges to tune

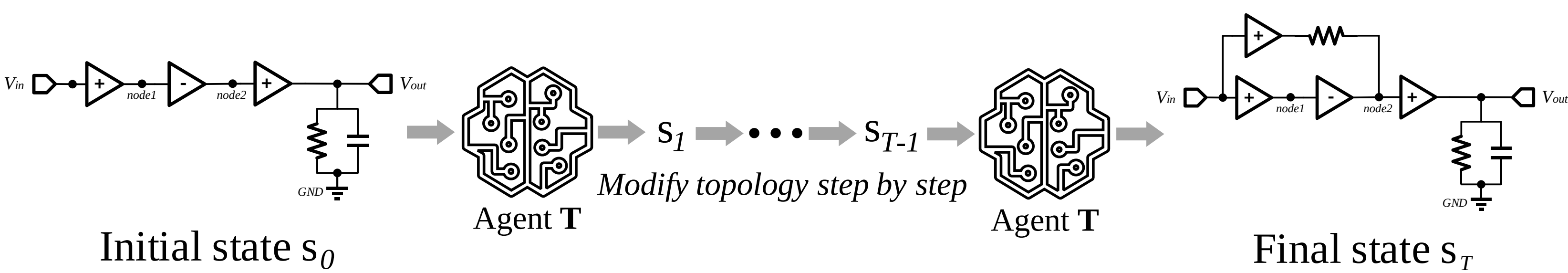
5x25 **action options** each step

4 Topology Design Task

- **Agent T design**

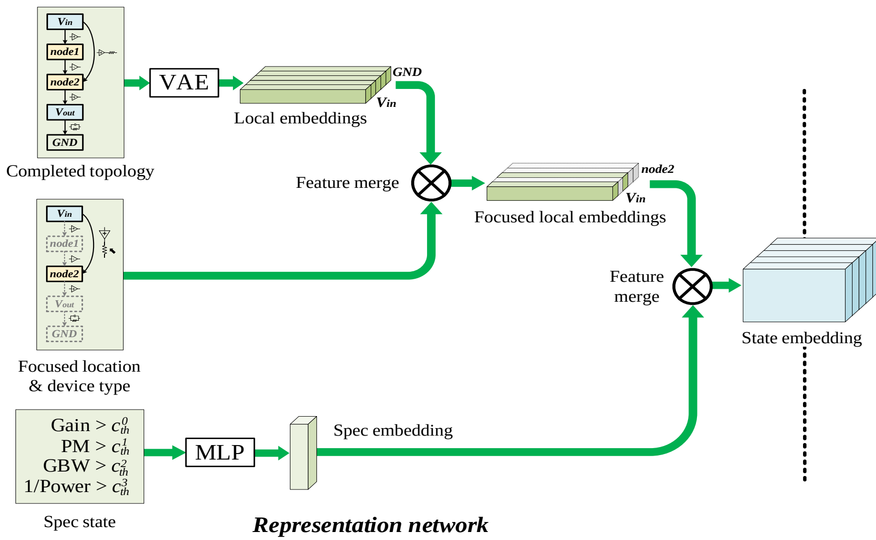


- **TD process**



5 Parameter Tuning Task

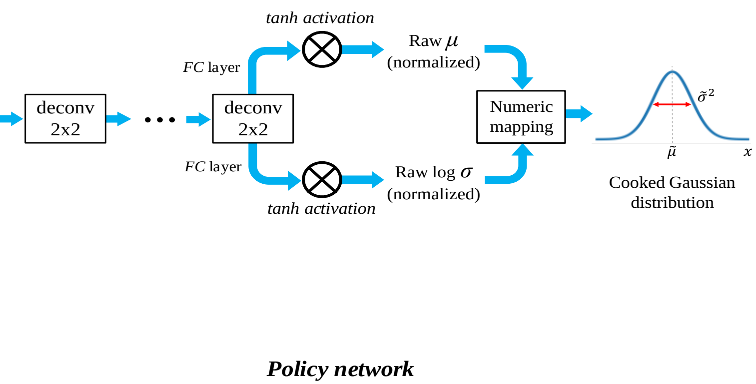
▪ Agent P design



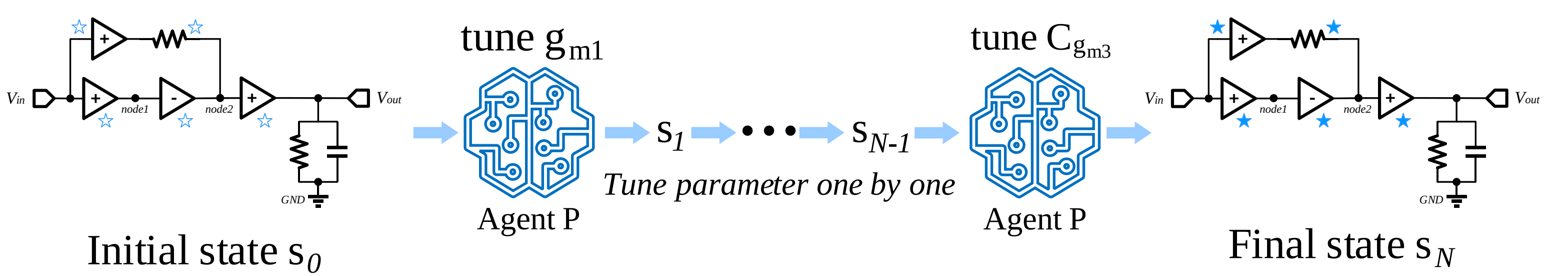
▪ State & action design

State: device type & device location

Action: $x \sim [x_{min}, x_{max}]$ for types



▪ PT process



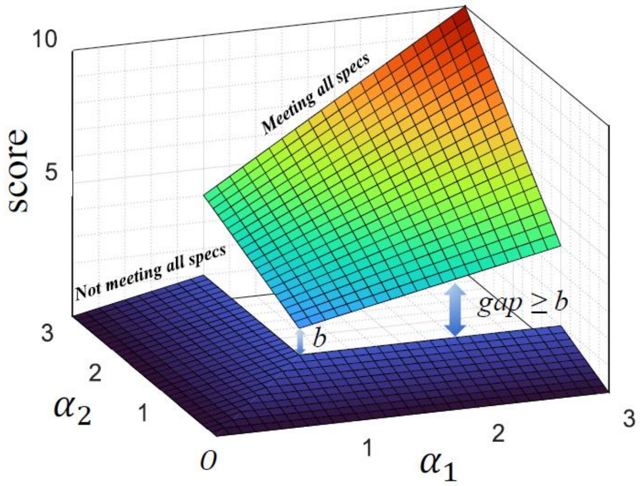
6 Reward Function Design

- **Our scoring function** [6]

$$\alpha_i = \frac{c_i}{c_{th}^i}, \forall i \in \{1, ..., N_c\}$$

$$\text{score} = \begin{cases} \prod_{i=1}^{N_c} {\alpha_i}^{\gamma_i} + b & \forall i \in \{1, ..., N_c\} : \alpha_i > 1 \\ \min_{i \in \{1, ..., N_c\}} (\alpha_i), & \exists i \in \{1, ..., N_c\} : \alpha_i \leq 1 \end{cases}$$

$$f(g, \mathbf{x}) = \begin{cases} \text{penalty}, & \text{if simulation fails} \\ \text{score}(g, \mathbf{x}), & \text{otherwise} \end{cases}$$



Guidance: find short board if not meet all specs yet

Distinction: meeting specs > not meeting specs > simulation failure

Redundancy: greater redundancy, higher score

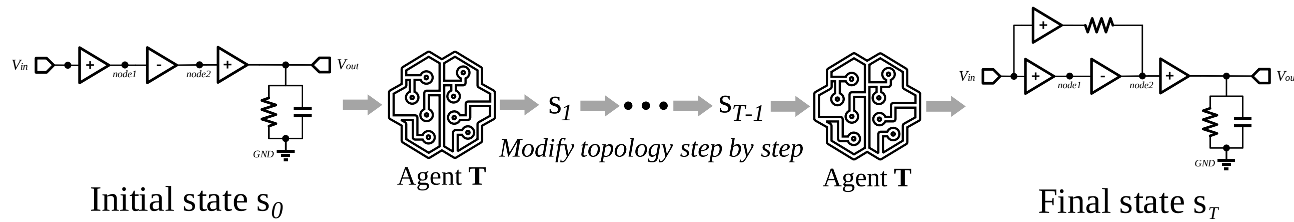
Flexibility: tune attention to each spec via gamma

7 Co-evolution of Agents

- **Single design trajectory**

Topology design

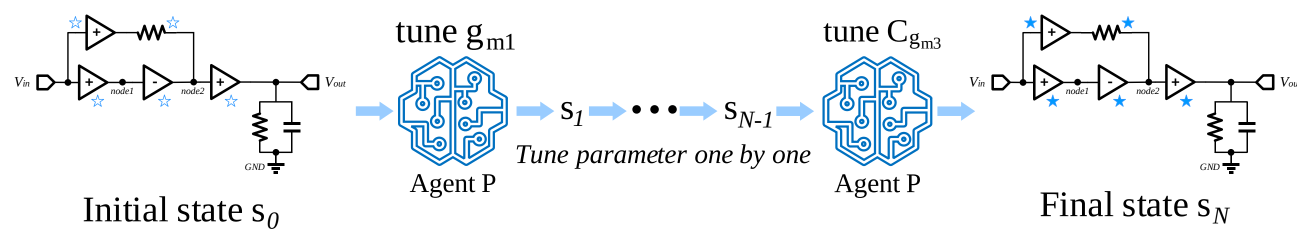
probability $p_{\mathrm{T}i}$



Parameter tuning

reward R_i

probability $p_{\mathrm{P}i}$



- **Training method**

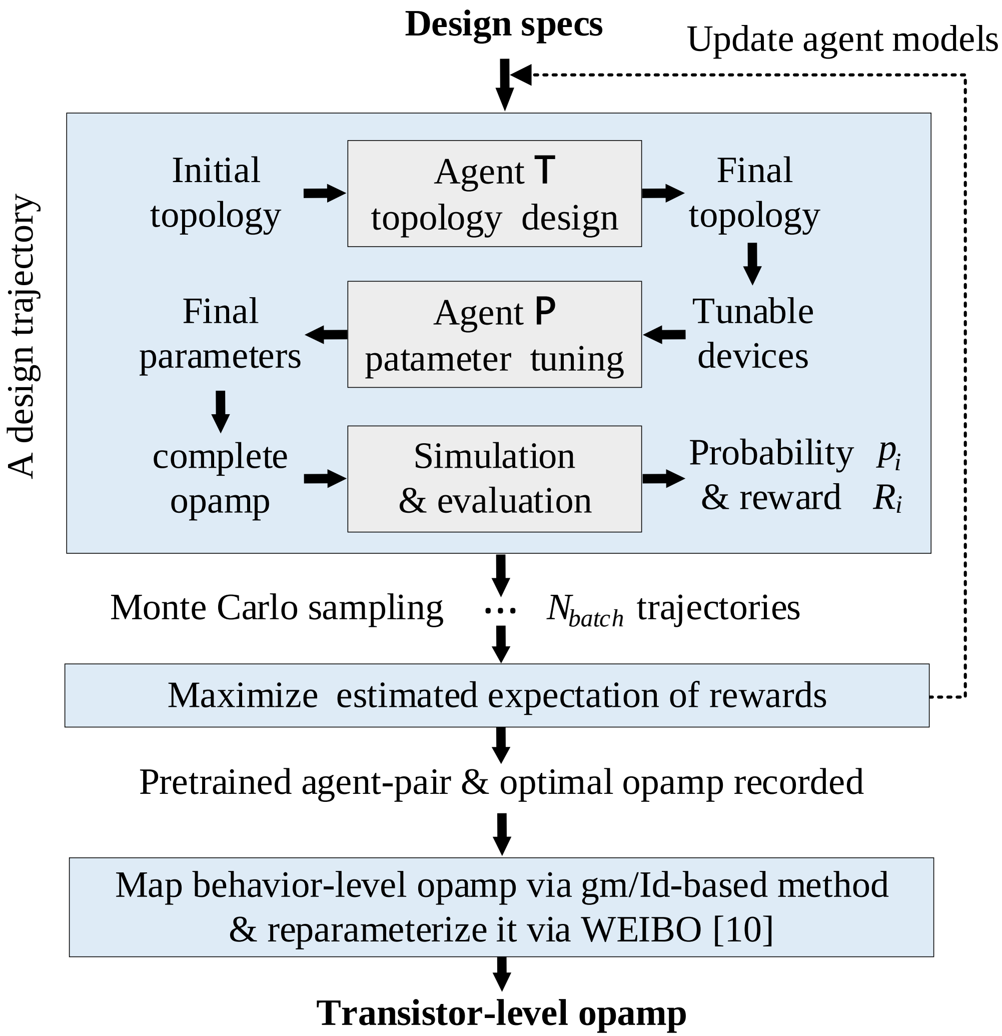
Monte Carlo sampling N-times

Maximize **reward expectation** by gradient method

$$\bar{R} = \sum_{i=1}^{N} R_i \, p_{\mathrm{T}i} p_{\mathrm{P}i}$$

Learn to design opamp

8 Overall Workflow



We use the mapping and re-optimization tool in [7] open sourced at

https://github.com/jialinlu/OPAMP-Generator.

[7] J. Lu, et al. "Automatic op-amp generation from specification to layout," IEEE TCAD, 2023.

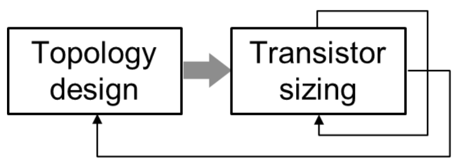
9 Experimental Setups

- **Experiment platforms**

Intel Xeon Gold 6226R CPU	for Cadence Spectre simulator
WEIBO [1]	for transistor sizing
NVIDIA RTX 2080Ti GPU	for agents deployment

- **Experiment cases**

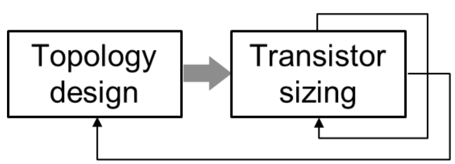
BOBO [5]



Inner loop: BO

Outer loop: BO

RLBO [6]

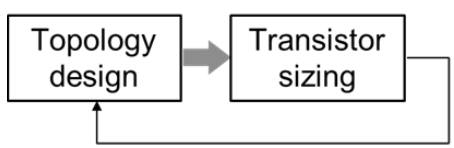


Inner loop: BO

Outer loop: RL

Gain	>85dB
PM	>55deg
GBW	>0.7MHz
Power	<250uW

MACRO



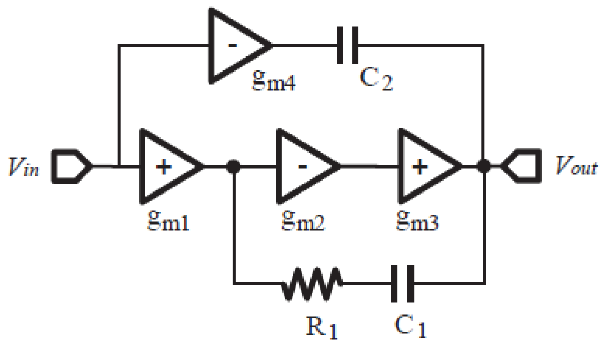
Inner loop canceled

Outer loop generates the feedback

10 Experimental Results

BEHAVIOR-LEVEL SEARCH RESULTS

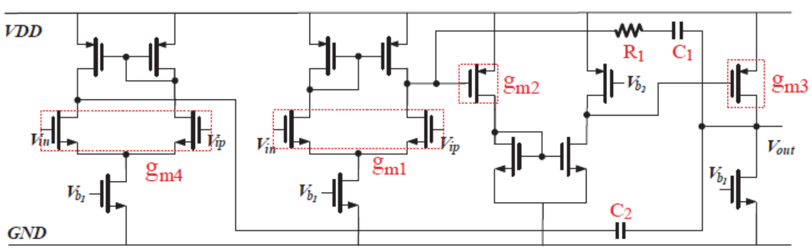
Methods		FoM	Gain (dB)	PM (degree)	GBW (MHz)	Power (μW)	Time* (h)
BOBO [6]	exp1	573497	85.1	73.5	0.8	13.1	3.04
	exp2	235292	86.2	55.9	2.3	97.2	0.65
	exp3	160779	86.4	60.5	2.5	154.0	4.15
	avg	**323189**	**85.9**	**63.3**	**1.9**	**88.1**	**2.61**
RLBO [9]	exp1	561382	86.0	57.3	2.6	46.2	3.43
	exp2	413630	90.1	56.2	3.1	75.5	2.27
	exp3	726207	86.8	57.9	2.4	33.3	2.77
	avg	**567073**	**87.6**	**57.1**	**2.7**	**51.7**	**2.82**
MACRO	exp1	676001	85.9	55.6	1.4	20.9	2.66
	exp2	785408	85.4	55.5	1.6	20.6	3.34
	exp3	691094	87.0	55.2	1.8	26.0	1.78
	avg	**717501**	**86.1**	**55.4**	**1.6**	**22.5**	**2.59**



Search result in exp1 of MACRO

TRANSISTOR-LEVEL MAPPING* RESULTS

Methods		FoM	Gain (dB)	PM (degree)	GBW (MHz)	Power (μW)	C_L (nF)	Process (nm)
BOBO [6]	exp1	244062	114.0	47.4	0.5	21.2	10	180
	exp2	112886	102.9	55.0	1.7	152.1	10	180
	exp3	184706	105.4	69.9	1.1	59.5	10	180
	avg	**180551**	**107.4**	**57.4**	**1.1**	**77.6**	-	-
RLBO [9]	exp1	309569	98.1	61.9	1.1	36.9	10	180
	exp2	260901	90.5	55.2	1.8	69.7	10	180
	exp3	237871	89.4	55.0	1.6	66.0	10	180
	avg	**269447**	**92.7**	**57.4**	**1.5**	**57.5**	-	-
MACRO	exp1	563391	98.1	56.7	2.1	37.9	10	180
	exp2	503255	101.0	61.2	2.3	46.1	10	180
	exp3	613469	98.8	55.2	3.1	50.2	10	180
	avg	**560038**	**99.3**	**57.7**	**2.5**	**44.7**	-	-



Mapping result in exp1 of MACRO

11 Result Analysis

- **Search results comparison**

MACRO's FoM is **2.22×** and **1.27×** that of BOBO and RLBO.

High-dimensional & heterogeneous space exploration capability

- **Mapping results comparison**

MACRO's FoM is **3.1×** and **2.08×** that of BOBO and RLBO.

FoM degradation is **0.78×**, better than BOBO (**0.56×**) and RLBO (**0.48×**).

Co-evolution could lead to **easier topology** and **universal parameters**.

Parametric space simplicity could maintain and ease resizing.

12 Conclusion

- **Design space is explored:**

  The multi-agent & multi-step scheme decompose the tasks.

- **Efficiency is maintained:**

  The inner-loop BO-based sizing is canceled.

- **Mapping degradation is lower:**

  Co-evolution could lead to smooth parametric space.

Thank you.

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